The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

The Linear Control Circuits Data Book for Design Engineers

First Edition

TEXAS INSTRUMENTS
INCORPORATED

LIMA TECHNICAL COLLEGE
OSU LIMA CAMPUS
4240 Campus Drive
LIMA, OHIO 45804

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INTRODUCTION

In this 368-page data book, Texas Instruments is pleased to present important technical information on a broad line of Linear Control Integrated Circuits.

You will find complete specifications on TI's TL series and second source Linear Control circuits including operational amplifiers, comparators, voltage regulators, analog switches, and special functions.

The functional indexes, selection guides and cross-references are designed for ease of circuit selection. There are margin tabs to guide you quickly to general circuit categories, and the alphanumeric index will let you locate specific type numbers quickly.

A military products section covers process screening requirements for JAN, JAN-processed, 883 Class B, and standard products. Test conditions and environmental levels are detailed for the product categories.

Although this volume offers design and specification data only for Linear Control Integrated Circuits, complete technical data for any TI semiconductor/component product is available from your nearest TI field sales office, local authorized TI distributor, or by writing directly to: Marketing and Information Services, Texas Instruments Incorporated, P.O. Box 5012, MS 308, Dallas, Texas 75222.

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*Future product, to be announced

CROSS-REFERENCE
Old TI Type Numbers to New TI Type Numbers

OLD NUMBER	NEW NUMBER
SN52L022	TL022M
SN52L044	TL044M
SN52101A	LM101A
SN52104	LM104
SN52105	LM105
SN52106	LM106
SN52107	LM107
SN52108*	TL081M†
SN52108A*	TL801M†
SN52109	LM109
SN52110*	
SN52111	LM111
SN52118	LM118
SN52506	TL506M
SN52510	TL510M
SN52514	TL514M
SN52555	SE555
SN52558	MC1558
SN52660*	TL081†
SN52702	TL702M
SN52702A	uA702M
SN52709	uA709M
SN52709A	uA709AM
SN52710	TL710M
SN52711	uA711M
SN52723	uA723M
SN52733	uA733M
SN52741	uA741M
SN52747	uA747M
SN52748	uA748M
SN52770*	TL081M†
SN52771*	TL081M†
SN52777	uA777M
SN52810	TL810M
SN52811	TL811M
SN52820	TL820M
SN5510*	
SN5511*	
SN5512*	
SN5514*	
SN56502	TL441M
SN56514*	
SN62088*	TL089I†
SN72L022	TL022C
SN72L044	TL044C
SN72088*	TL089C†
SN72301A	LM301A
SN72304	LM304
SN72305	LM305
SN72305A	LM305A
SN72306	LM306
SN72307	LM307
SN72308*	TL081C†
SN72308A*	TL081C†
SN72309	LM309
SN72310*	
SN72311	LM311
SN72318	LM318
SN72376	LM376
SN72440	TL440C
SN72506	TL506C
SN72510	TL510C
SN72514	TL514C
SN72555	NE555
SN72558	MC1458
SN72560	TL560C
SN72660*	TL081C†
SN72702	TL702C
SN72709	uA709C
SN72710	TL710C
SN72711	uA711C
SN72720	TL720C
SN72723	uA723C
SN72733	uA733C
SN72741	uA741C
SN72747	uA747C
SN72748	uA748C
SN72770*	TL081C†
SN72771*	TL081C†
SN72777	uA777C
SN72810	TL810C
SN72811	TL811C
SN72820	TL820C
SN7510*	
SN7511*	
SN7512*	
SN7514*	
SN76502	TL441C
SN76514*	

*Not recommended for new design.

† Recommended as replacement

FUNCTIONAL INDEX

OPERATIONAL AMPLIFIERS

FUNCTION		OPERATING FREE-AIR TEMPERATURE RANGE				PACKAGE TYPES	PAGE
		−55°C to 125°C	−40°C to 85°C	−25°C to 85°C	0°C to 70°C		
General-Purpose Operational Amplifiers	Single	TL702M				J, L, U	113
					TL702C	J, L, N, U	
		uA702M				J, L	118
		uA709AM				J, JG, L, U	123
		uA709M				J, JG, L, U	
					uA709C	J, JG, L, N, P,U	
		uA741M				J, JG, L, U	129
					uA741C	J, JG, L, N, P, U	
		uA748M				J, JG, L, U	137
					uA748C	J, JG, L, N, P, U	
	Dual	LM158				JG, L	85
				LM258		JG, L, P	
					LM358	JG, L, P	
			LM2904			JG, L, P	89
		MC1558				JG, L	91
					MC1458	JG, L, P	
		uA747M				J, L, W	133
					uA747C	J, L, N, W	
	Quad	LM124				J	83
				LM224		J, N	
					LM324	J, N	
			LM2902			J, N	87
JFET-Input Operational Amplifiers	Single	LF155				JG, L	63
		LF155A				JG, L	
				LF255		JG, L, P	
					LF355	JG, L, P	
					LF355A	JG, L, P	
		LF156				JG, L	63
		LF156A				JG, L	
				LF256		JG, L, P	
					LF356	JG, L, P	
					LF356A	JG, L, P	
		LF157				JG, L	63
		LF157A				JG, L	
				LF257		JG, L, P	
					LF357	JG, L, P	
					LF357A	JG, L, P	
					TL081AC*	JG, L, P	105
					TL081C*	JG, L, P	
	Dual	LF2155				JG, L	69
		LF2155A				JG, L	
				LF2255		JG, L, P	
					LF2355	JG, L, P	
					LF2355A	JG, L, P	
		LF2156				JG, L	69
		LF2156A				JG, L	
				LF2256		JG, L, P	
					LF2356	JG, L, P	
					LF2356A	JG, L, P	
	Quad				TL084C*	J, N	107

*Future product, to be announced.

OPERATIONAL AMPLIFIERS

FUNCTION		OPERATING FREE-AIR TEMPERATURE RANGE			PACKAGE TYPES	PAGE
		−55°C to 125°C	−25°C to 85°C	0°C to 70°C		
Wide-Band Operational Amplifiers	Single	LM118			JG, L, U	80
			LM218		JG, L, P, U	
				LM318	JG, L, P, U	
High-Performance Operational Amplifiers	Single	LM101A			J, JG, L, U	74
			LM201A		J, JG, L, N, P, U	
				LM301A	J, JG, L, N, P, U	
		LM107			J, JG, L, U	77
			LM207		J, JG, L, N, P, U	
				LM307	J, JG, L, N, P, U	
		uA777M			J, JG, L, U	141
				uA777C	J, JG, L, N, P, U	
	Dual	RM4558			JG, L	97
				RC4558	JG, L, P	
	Quad	RM4136			J	95
				RC4136	J, N	
Low-Power Operational Amplifiers	Dual	TL022M			JG, L	99
				TL022C	JG, L, P	
	Quad	TL044M			J	102
				TL044C	J, N	
Chopper-Stabilized Operational Amplifiers	Single		TL089I		L	108
				TL089C	L	

FUNCTIONAL INDEX

DIFFERENTIAL COMPARATORS

FUNCTION		OPERATING FREE-AIR TEMPERATURE RANGE				PACKAGE TYPES	PAGE
		−55°C to 125°C	−40°C to 85°C	−25°C to 85°C	0°C to 70°C		
Differential Comparators	Single	TL710M				J, JG, L, U	185
					TL710C	J, JG, L, N, P, U	
		uA710M				J, JG, L, U	203
		TL810M				J, JG, L, U	191
					TL810C	J, JG, L, N, P, U	
	Dual	LM193				JG, L	167
				LM293		JG, L, P	
					LM393	JG, L, P	
			LM2903			JG, L, P	171
					TL720C	J, N	189
		TL820M				J	201
					TL820C	J, N	
	Quad	LM139				J	165
				LM239		J, N	
					LM339	J, N	
			LM2901			J, N	169
Differential Comparators with Strobes	Single	LM106				J, JG, L, U	151
				LM206		J, JG, L, N, P, U	
					LM306	J, JG, L, N, P, U	
		LM111				J, JG, L, U	157
					LM311	J, JG, L, N, P, U	
		TL510M				J, JG, L, U	179
					TL510C	J, JG, L, N, P, U	
	Dual	TL506M				J, W	173
					TL506C	J, N, W	
		TL514M				J	183
					TL514C	J, N	
Dual-Channel Differential Comparators with Strobes		uA711M				J, L, U	207
					uA711C	J, L, N, U	
		TL811M				J, L, U	195
					TL811C	J, L, N, U	

VOLTAGE REGULATORS

FUNCTION		OPERATING VIRTUAL-JUNCTION TEMPERATURE RANGE			PACKAGE TYPES	PAGE
		−55°C to 150°C	−25°C to 125°C	0°C to 125°C		
Adjustable Positive-Voltage Regulators		LM117*			KA	229
			LM217*		KA, KC	
				LM317*	KA, KC	
Positive Fixed-Voltage Regulators	2.6 Volts			uA78L02C	JG, LP	255
				uA78L02AC	JG, LP	
	5 Volts	LM109			LA	225
			LM209		LA	
				LM309	LA	
		uA7805M			KA	245
				uA7805C	KA, KC	
				uA78L05C	JG, LP	255
				uA78L05AC	JG, LP	
		uA78M05M			LA	261
				uA78M05C	KC, KD, LA	
	6 Volts	uA7806M			KA	245
				uA7806C	KA, KC	
		uA78M06M			LA	261
				uA78M06C	KC, KD, LA	
	6.2 Volts			uA78L06C	JG, LP	255
				uA78L06AC	JG, LP	
	8 Volts	uA7808M			KA	245
				uA7808C	KA, KC	
				uA78L08C	JG, LP	255
				uA78L08AC	JG, LP	
		uA78M08M			LA	261
				uA78M08C	KC, KD, LA	
	8.5 Volts	uA7885M			KA	245
				uA7885C	KA, KC	
	12 Volts	uA7812M			KA, KA	245
				uA7812C	KA, KC	
				uA78L12C	JG, LP	255
				uA78L12AC	JG, LP	
		uA78M12M			LA	261
				uA78M12C	KC, KD, LA	
	15 Volts	uA7815M			KA	245
				uA7815C	KA, KC	
				uA78L15C	JG, LP	255
				uA78L15AC	JG, LP	
		uA78M15M			LA	261
				uA78M15C	KC, KD, LA	
	18 Volts	uA7818M			KA	245
				uA7818C	KA, KC	
	20 Volts	uA78M20M			LA	261
				uA78M20C	KC, KD, LA	
	24 Volts	uA7824M			KA	245
				uA7824C	KA, KC	
		uA78M24M			LA	261
				uA78M24C	KC, KD, LA	

*Future product, to be announced.

FUNCTIONAL INDEX

VOLTAGE REGULATORS

FUNCTION		OPERATING VIRTUAL-JUNCTION TEMPERATURE RANGE			PACKAGE TYPES	PAGE
		−55°C to 150°C	−25°C to 125°C	0°C to 125°C		
Negative Fixed-Voltage Regulators	5 Volts	uA7905M			KA	271
				uA7905C	KA, KC	
		uA79M05M			LA	281
				uA79M05C	KC, KD, LA	
	6 Volts	uA7906M			KA	271
				uA7906C	KA, KC	
		uA79M06M			LA	281
				uA79M06C	KC, KD, LA	
	8 Volts	uA7908M			KA	271
				uA7908C	KA, KC	
		uA79M08M			LA	281
				uA79M08C	KC, KD, LA	
	12 Volts	uA7912M			KA	271
				uA7912C	KA, KC	
		uA79M12M			LA	281
				uA79M12C	KC, KD, LA	
	15 Volts	uA7915M			KA	271
				uA7915C	KA, KC	
		uA79M15M			LA	281
				uA79M15C	KC, KD, LA	
	18 Volts	uA7918M			KA	271
				uA7918C	KA, KC	
	20 Volts	uA79M20M			LA	281
				uA79M20C	KC, KD, LA	
	24 Volts	uA7924M			KA	271
				uA7924C	KA, KC	
		uA79M24M			LA	281
				uA79M24C	KC, KD, LA	

FUNCTION	OPERATING FREE-AIR TEMPERATURE RANGE			PACKAGE TYPES	PAGE
	−55°C to 125°C	−25°C to 85°C	0°C to 70°C		
Precision Voltage Regulators	uA723M			J, L, U	239
			uA723C	J, L, N, U	
Positive-Voltage Regulators	LM105			JG, L	221
		LM205		JG, L, P	
			LM305	JG, L, P	
			LM305A	JG, L, P	
			LM376	JG, L, P	
Negative-Voltage Regulators	LM104			J, L	217
		LM204		J, L, N	
			LM304	J, L, N	
Shunt Regulator			TL430C	JG, LP	233
Switching Voltage Regulators	TL497M			J	236
		TL497I		J, N	
			TL497C	J, N	

SPECIAL FUNCTIONS

FUNCTION		OPERATING FREE-AIR TEMPERATURE RANGE			PACKAGE TYPES	PAGE
		−55°C to 125°C	−25°C to 85°C	0°C to 70°C		
Analog Switches	SPST	TL610M			JG	339
			TL610I		JG, P	
				TL610C	JG, P	
	Dual SPST	TL182M			L	305
			TL182I		L, N	
				TL182C	L, N	
		TL604M			JG	339
			TL604I		JG, P	
				TL604C	JG, P	
	SPDT	TL188M			L	311
			TL188I		L, N	
				TL188C	L, N	
		TL601M			JG	339
			TL601I		JG, P	
				TL601C	JG, P	
		TL607M			JG	339
			TL607I		JG, P	
				TL607C	JG, P	
	Dual SPDT	TL191M			J	314
			TL191I		J, N	
				TL191C	J, N	
	Dual DPST	TL185M			J	308
			TL185I		J, N	
				TL185C	J, N	
Precision Timers		SE555			JG, L	295
				NE555	JG, L, P	
Precision Level Detector				TL560C	JG, L, P	333
Zero-Voltage Switch				TL440C	J, N	317
Logarithmic Amplifiers		TL441M			J	323
				TL441C	J, N	
Differential Video Amplifiers with Gain Select		uA733M			J, L, U	345
				uA733C	J, L, N, U	
Analog Processor				TL500C*	N	330
Digital Panel Meter Logic Control Device				TL502C*	N	331

*Future product, to be announced.

INTERCHANGEABILITY GUIDE

(ALPHABETICALLY BY MANUFACTURERS)

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Several of the popular Linear Interface circuits, not included in this book, are included in the interchangeability guides for your reference.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

FAIRCHILD ORDER INFORMATION

EXAMPLE OF ORDER CODE:

XXX — Device Type

D — Package Type
- D = C-DIP
- F = FLAT PACK
- P = PLASTIC DIP
- T = MINI DIP
- H = METAL CAN

C — Temperature Range
- C = Commercial/Inductrial Consumer 0°C to 70°C or 75°C
- M = Military –55°C to 125°C

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
µA101A	LM101A	
µA104	LM104	
µA105	LM105	
µA107	LM107	
µA109	LM109	
µA111	LM111	
µA139	LM139	
µA201A	LM201A	
µA204	LM204	
µA205	LM205	
µA207	LM207	
µA209	LM209	
µA301A	LM301A	
µA304	LM304	
µA305	LM305	
µA305A	LM305A	
µA307	LM307	
µA309	LM309	
µA311	LM311	
µA376	LM376	
µA555	SE555	
µA702	uA702	
µA709	uA709	
µA709A	uA709A	
µA710	uA710	
µA711	uA711	
µA715		LM118
µA723	uA723	
µA733	uA733	
µA734		LM111
µA741	uA741	
µA742		TL440
µA747	uA747	
µA748	uA748	
µA776		uA777
µA777	uA777	
8T13	SN55121	
8T14	SN55122	
8T23	SN75123	
8T24	SN75124	
1458	MC1458	
1558	MC1558	
7524	SN7524	
7525	SN7525	
µA7805	uA7805	
µA7806	uA7806	
µA7808	uA7808	
µA7812	uA7812	
µA7815	uA7815	
µA7818	uA7818	
µA7824	uA7824	
µA78L05	uA78L05	
µA78L06	uA78L06	
µA78L08	uA78L08	
µA78L12	uA78L12	
µA78L15	uA78L15	
µA78L26	uA78L26	
µA78L05A	uA78L05A	
µA78L06A	uA78L06A	
µA78L08A	uA78L08A	
µA78L12A	uA78L12A	
µA78L15A	uA78L15A	
µA78L26A	uA78L26A	
µA78M05	uA78M05	

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
µA78M06	uA78M06	
µA78M08	uA78M08	
µA78M12	uA78M12	
µA78M15	uA78M15	
µA78M20	uA78M20	
µA78M24	uA78M24	
µA7905	uA7905	
µA7906	uA7906	
µA7908	uA7908	
µA7912	uA7912	
µA7915	uA7915	
µA7924	uA7924	
µA79M05	uA79M05	
µA79M06	uA79M06	
µA79M08	uA79M08	
µA79M12	uA79M12	
µA79M15	uA79M15	
µA79M20	uA79M20	
µA79M24	uA79M24	
9614	SN75114	
9615	SN75115	
9616		SN75150
		SN75188
9617		SN75189
		SN75189A
		SN75152
		SN75154
9627		SN75152
55107	SN55107A	
55108	SN55108A	
55109	SN55109	
55110	SN55110	
75325	SN75325	
75450	SN75450	
75451	SN75451	
75452	SN75452	
75453	SN75453	
75454	SN75454	
75460	SN75460	
75461	SN75461	
75462	SN75462	
75463	SN75463	
75491	SN75491	
75492	SN75492	

MOTOROLA ORDER INFORMATION

EXAMPLE OF ORDER CODE:

MC

Prefix

XXX

Type Number

Different Numbers
Are Used For Variations
In Operating Temperatures

P

Package

F = Flat Package
G = Metal Can
L = C-DIP
P = Plastic

MOTOROLA	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
MLM101A	LM101A	
MLM107	LM107	
MLM109	LM109	
MLM111	LM111	
MLM201A	LM201A	
MLM207	LM207	
MLM209	LM209	
MLM211	LM211	
MLM301A	LM301A	
MLM304	LM304	
MLM305	LM305	
MLM307	LM307	
MLM309	LM309	
MLM311	LM311	
MC1414	TL514	
MC1420		uA733
MC1430		uA702
MC1431		uA702
MC1433		LM301A
MC1439		LM301A
MC1455	NE555	
MC1458	MC1458	
MC1460		uA723
MC1461		uA723
MC1463		uA723
MC1466		uA723
MC1469		uA723
MC1510	SN5510	
MC1514	SN52514	
MC1520		SN5511
MC1530		uA702
MC1531		uA702
MC1533		LM101A
MC1539		LM101A
MC1555	SE555	
MC1558	MC1558	

MOTOROLA	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
MC1560		uA723
MC1561		uA723
MC1563		uA723
MC1566		uA723
MC1569		uA723
MC1709	uA709	
MC1710	uA710	
MC1711	uA711	
MC1712	uA702	
MC1723	uA723	
MC1733	uA733	
MC1741	uA741	
MC1747	uA747	
MC1748	uA748	
MC3302P	LM339	
MC3302	LM3302	
MC7705	uA78M05	
MC7706	uA78M06	
MC7708	uA78M08	
MC7712	uA78M12	
MC7715	uA78M15	
MC7720	uA78M20	
MC7724	uA78M24	
MC7805	uA7805	
MC7806	uA7806	
MC7808	uA7808	
MC7812	uA7812	
MC7815	uA7815	
MC7818	uA7818	
MC7824	uA7824	

NATIONAL ORDER INFORMATION

EXAMPLE OF ORDER CODE:

LM — Prefix: LM, LH = Linear; DM = Line Ckts

1 — Temperature Range: 1 or 7 = 55°C to 125°C; 3 or 8 = 0°C to 70°C or 75°C

XXXX — Type Number

N — Package:
D = C-DIP
N = Plastic DIP
F = Flat Pack
H = Metal Can
N = Mini-DIP

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
LF155	LF155	
LF155A	LF155A	
LF255	LF255	
LF355	LF355	
LF355A	LF355A	
LF2155	LF2155	
LF2155A	LF2155A	
LF2156	LF2156	
LF2156A	LF2156A	
LF2255	LF2255	
LF2256	LF2256	
LF2355	LF2355	
LF2356	LF2356	
LM101A	LM101A	
LM102	LM102	
LM104	LM104	
LM105	LM105	
LM106	LM106	
LM107	LM107	
LM109	LM109	
LM110	LM110	
LM111	LM111	
LM112	LM112	
LM117	LM117	
LM118	LM118	
LM120-5	uA7905M	
LM120-6	uA7906M	
LM120-8	uA7908M	
LM120-12	uA7912M	
LM120-15	uA7915M	
LM120-24	uA7924M	
LM122	LM122	
LM123	LM123	
LM124	LM124	
LM139	LM139	
LM158	LM158	
LM193	LM193	
LM201A	LM201A	
LM205	LM205	
LM206	LM206	
LM207	LM207	
LM209	LM209	
LM211	LM211	
LM217	LM217	
LM218	LM218	
LM224	LM224	
LM239	LM239	
LM258	LM258	
LM293	LM293	
LM301A	LM301A	

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
LM304	LM304	
LM305	LM305	
LM306	LM306	
LM307	LM307	
LM309	LM309	
LM311	LM311	
LM317	LM317	
LM318	LM318	
LM320T-5	uA7905C	
LM320T-6	uA7906C	
LM320T-8	uA7908C	
LM320T-12	uA7912C	
LM320T-15	uA7915C	
LM320T-24	uA7924C	
LM324	LM324	
LM339	LM339	
LM340T-5	uA7805C	
LM340T-6	uA7806C	
LM340T-8	uA7808C	
LM340T-12	uA7812C	
LM340T-15	uA7815C	
LM340T-18	uA7818C	
LM340T-24	uA7824C	
LM341-5	uA78M05C	
LM341-6	uA78M06C	
LM341-8	uA78M08C	
LM341-12	uA78M12C	
LM341-15	uA78M15C	
LM341-24	uA78M24C	
LM358	LM358	
LM376	LM376	
LM393	LM393	
LM555M	SE555	
LM555C	NE555	
LM709	uA709	
LM709A	uA709A	
LM709C	uA709C	
LM710	uA710	
LM710C	uA710C	
LM711	uA711	
LM711C	uA711C	
LM723	uA723	
LM723C	uA723C	
LM733	uA733	
LM733C	uA733C	
LM741	uA741	
LM741C	uA741C	
LM747	uA747	
LM747C	uA747C	
LM748	uA748	
LM748C	uA748C	
LM1414N	TL514C	
LM1458	SN72558	
LM1514	TL514M	
LM1558	MC1558	
LM2901	LM2901	
LM2902	LM2902	
LM2903	LM2903	
LM2904	LM2904	
LM3302	LM3302	
LM3900		TL044
LM3905		NE555
LM5520	SN5520	
LM5521	SN5521	
LM5522	SN5522	
LM5523	SN5523	
LM5524	SN5524	
LM5525	SN5525	
LM5528	SN5528	
LM5529	SN5529	
LM78L05C	uA78L05C	
LM78L08C	uA78L08C	
LM78L12C	uA78L12C	
LM78L15C	uA78L15C	

RAYTHEON ORDER INFORMATION

EXAMPLE OF ORDER CODE:

R	M	XXX	L
Prefix	Temperature Range	Type Number	Package
	M = Military C = Consumer		DC = C-DIP DP, ND = Plastic DIP Q, J = Flat Pack TO = Metal Can

RAYTHEON	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
LM101A	LM101A	
LM106	LM106	
LM107	LM107	
LM109	LM109	
LM111	LM111	
LM118	LM118	
LM124	LM124	
LM139	LM139	
LM158	LM158	
LM201A	LM201A	
LM206	LM206	
LM207	LM207	
LM209	LM209	
LM211	LM211	
LM218	LM218	
LM224	LM224	
LM239	LM239	
LM258	LM258	
LM301A	LM301A	
LM304	LM304	
LM305	LM305	
LM306	LM306	
LM307	LM307	
LM309	LM309	
LM311	LM311	
LM318	LM318	
LM324	LM324	
LM339	LM339	
LM358	LM358	
RC7805	uA7805C	
RC7806	uA7806C	
RC7808	uA7808C	
RC7812	uA7812C	
RC7815	uA7815C	
RC7818	uA7818C	
RC7824	uA7824C	
RC555	NE555	
RC702	uA702C	
RC709	uA709C	
RC710	uA710C	
RC711	uA711C	
RC723	uA723C	
RC733	uA733C	
RC741	uA741C	
RC747	uA747C	
RC748	uA748C	
RC1458	MC1458	
RC3302	LM3302	
RC4136	RC4136	
RC4558	RC4558	
RC78XX	uA78XXC	
RM555	SE555	
RM702	uA702M	
RM709	uA709M	
RM710	uA710M	
RM711	uA711M	
RM723	uA723M	
RM733	uA733M	
RM741	uA741M	
RM747	uA747M	
RM748	uA748M	
RM1514	TL514M	
RM1558	MC1558	
RM4136	RM4136	
RM4558	RM4558	

SIGNETICS ORDER INFORMATION

EXAMPLE OF ORDER CODE:

NE — Temperature Range

NE = 0°C to 70°C or 75°C
SE = −55°C to 125°C

XXXX — Type Number

B — Package

F, I = C-DIP
A, B, N, V = Plastic DIP
Q, W = Flat Pack

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
LM101A	LM101A	
LM107	LM107	
LM109	LM109	
LM111	LM111	
LM124	LM124	
LM139	LM139	
LM201A	LM201A	
LM207	LM207	
LM209	LM209	
LM211	LM211	
LM224	LM224	
LM239	LM239	
LM301A	LM301A	
LM307	LM307	
LM309	LM309	
LM311	LM311	
LM324	LM324	
LM339	LM339	
NE532	LM358	
NE555	NE555	
NE5733	uA733C	
NE7805	uA7805C	
NE7806	uA7806C	
NE7808	uA7808C	
NE7812	uA7812C	
NE7815	uA7815C	
NE7824	uA7824C	
NE78L05	uA78L05C	
NE78L06	uA78L06C	
NE78L08	uA78L08C	
NE78L12	uA78L12C	
NE78L15	uA78L15C	
NE78M05	uA78M05C	
NE78M20	uA78M20C	
NE78M24	uA78M24C	
SE532	LM158	
SE555	SE555	
SE5733	uA733M	
SE7805	uA7805M	
SE7806	uA7806M	
SE7808	uA7808M	
SE7812	uA7812M	
SE7815	uA7815M	
SE7824	uA7824M	
SE78M05	uA78M05M	
uA709	uA709	
uA709A	uA709A	
uA710	uA710M	
uA710C	uA710C	
uA711	uA711M	
uA711C	uA711C	
uA723	uA723M	
uA741	uA741M	
uA741C	uA741C	
uA747C	uA747C	
uA748	uA748M	
uA748C	uA748C	

Thermal Information

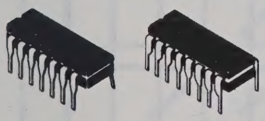
THERMAL RESISTANCES FOR LINEAR INTEGRATED CIRCUITS

PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$ (°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)
J ceramic dual-in-line	14	56	122
	16	60	116
J ceramic dual-in-line[†]	14	25[†]	91[†]
	16	29[†]	85[†]
JG ceramic dual-in-line	8	45	135
JG ceramic dual-in-line[†]	8	20[†]	110[†]
L plug-in	8, 10	51	195
LA plug-in, steel header	3	15	210
LP plastic plug-in	3	35	160
N plastic dual-in-line	14	45	108
	16	42	102
P plastic dual-in-line	8	45	125
U ceramic flat	10, 14	55	185
W ceramic flat	14	60	126
	16	59	124

[†] These ratings apply only for devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883."

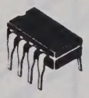
For thermal resistances of KA, KC, and KD power packages, see individual product data sheets.

J PACKAGES

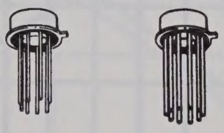


14-PIN 16-PIN

JG PACKAGE

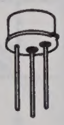


L PACKAGES

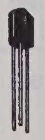


8-PIN 10-PIN

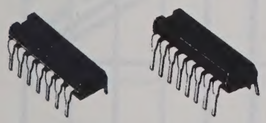
LA PACKAGE



LP PACKAGE

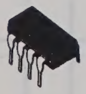


N PACKAGES

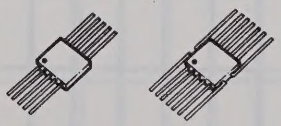


14-PIN 16-PIN

P PACKAGE

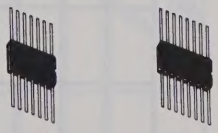


U PACKAGES



10-PIN 14-PIN

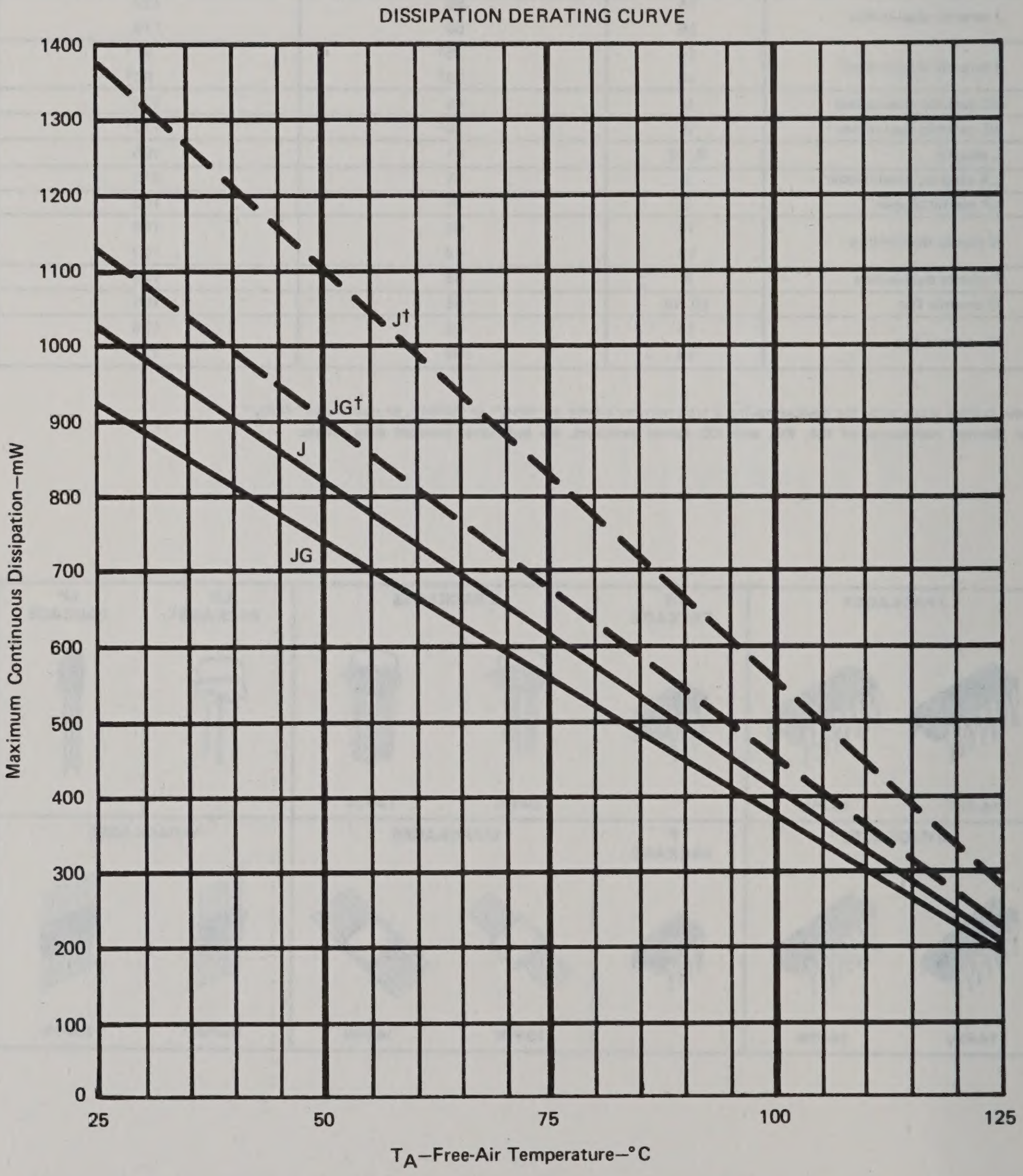
W PACKAGES



14-PIN 16-PIN

CERAMIC DUAL-IN-LINE PACKAGES

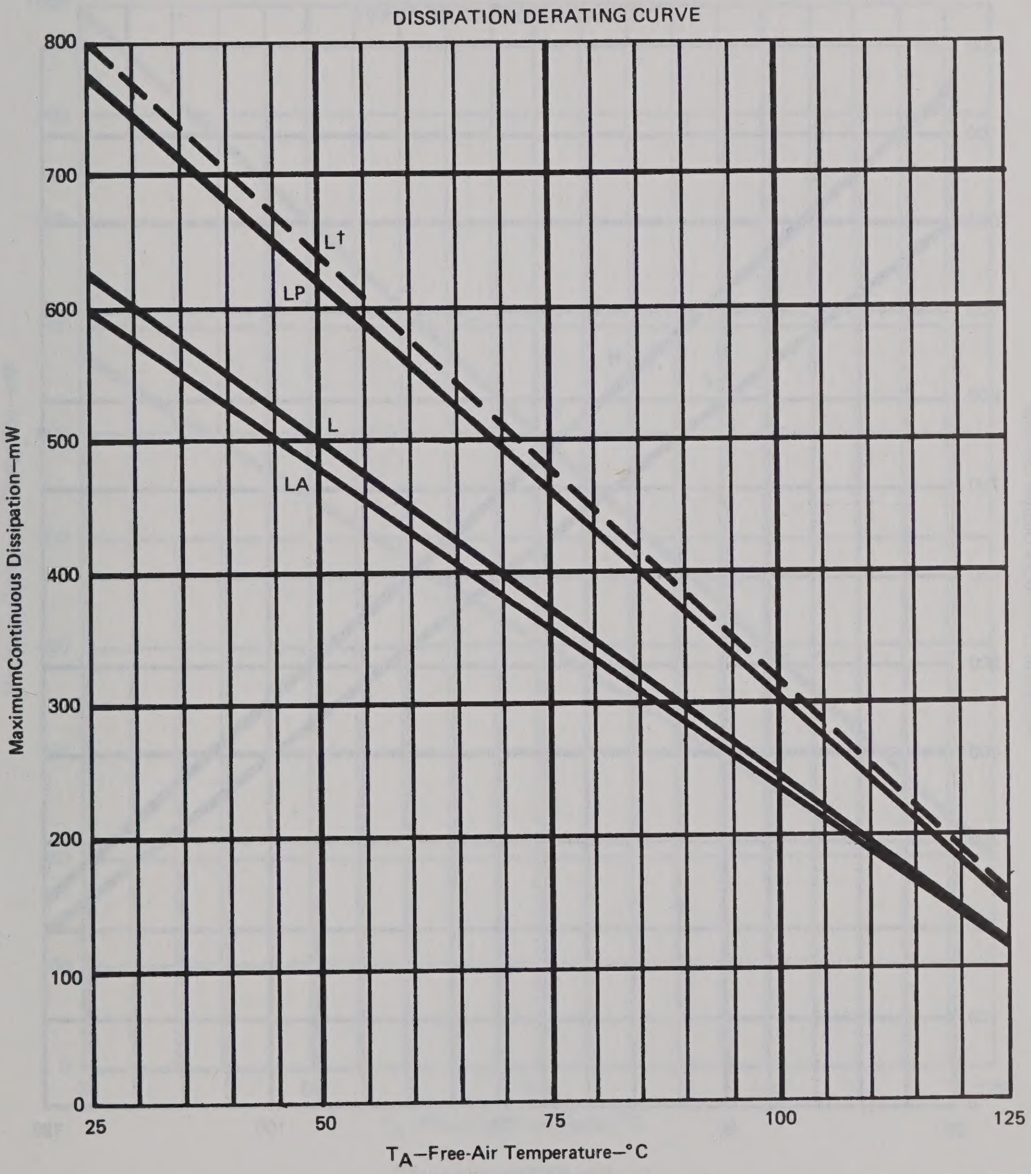
These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.



†The dashed lines apply only for devices having a type number prefix of "SNC" or "SNM", or a suffix of "/833."

AXIAL-LEAD PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

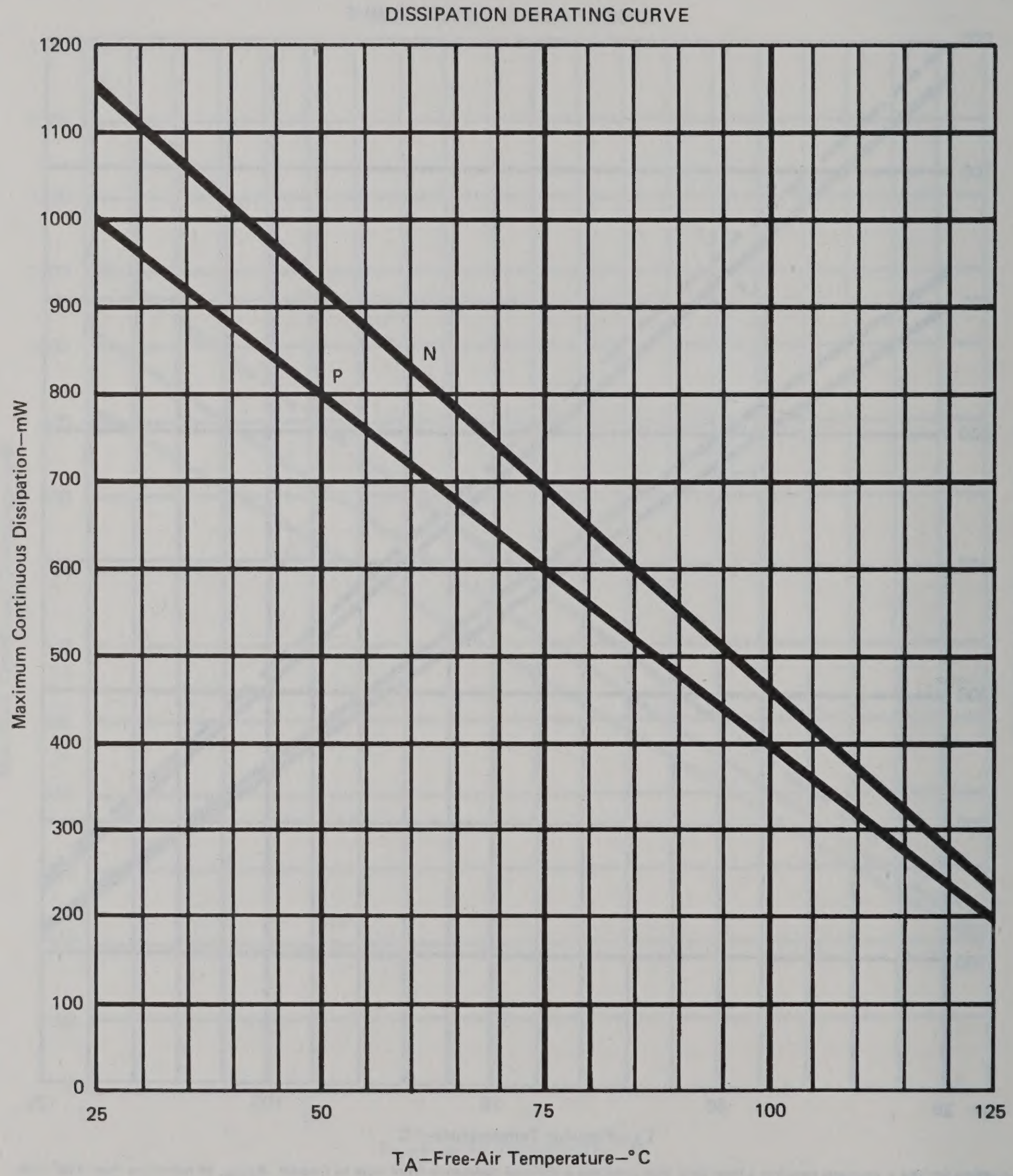


†This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

THERMAL INFORMATION

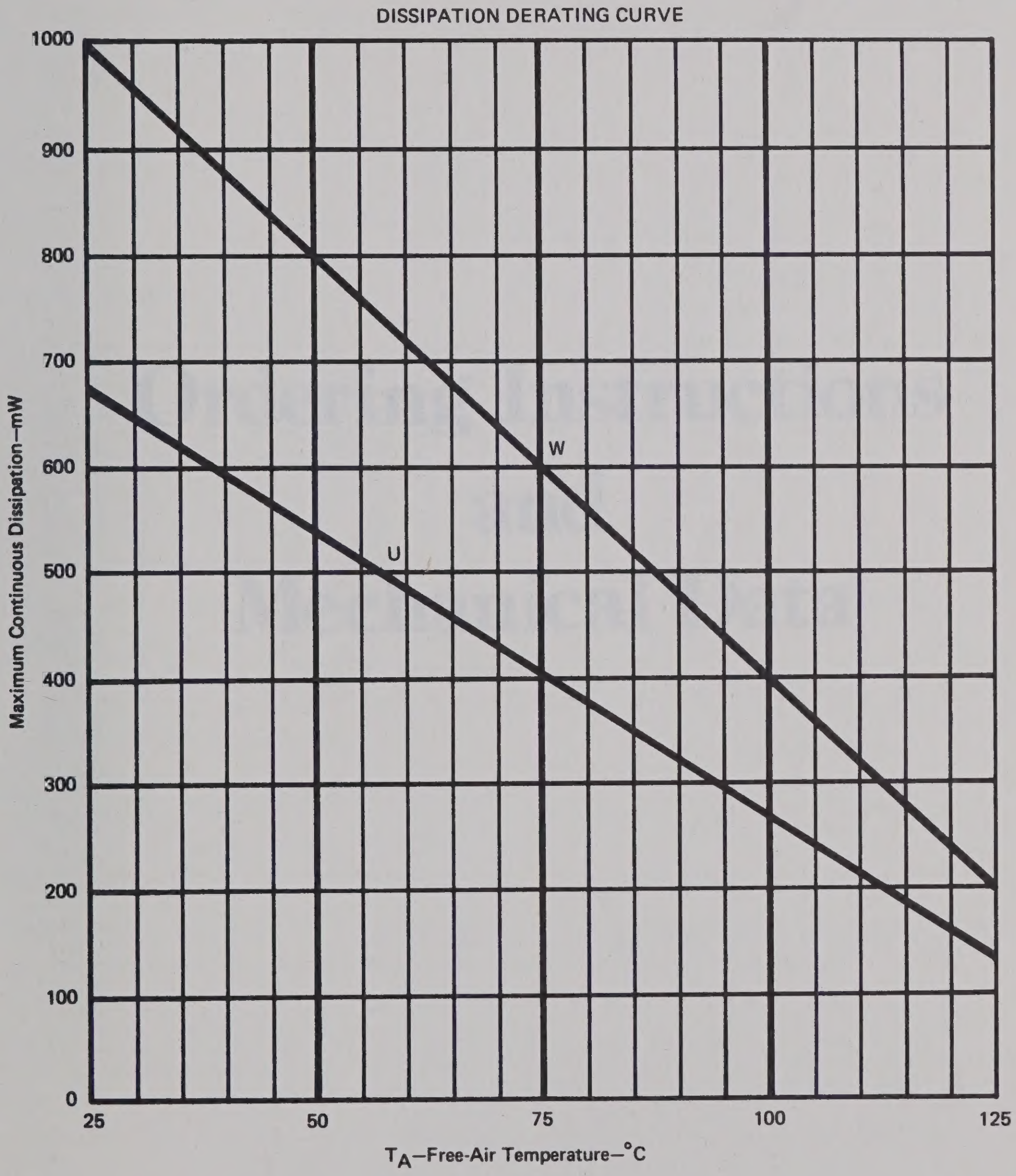
PLASTIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.



FLAT PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.



Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawing shown in this section.

Factory orders for ciricuits described in this data book should include a five-part type number as explained in the following example.

EXAMPLE: TL 022M JG /883B –00

1. Prefix

MUST CONTAIN TWO OR THREE LETTERS

TL	TI Linear Control Products
SN	TI Interface Products
SNM	Mach IV, Level I
SNC	Mach IV, Level III

STANDARD SECOND-SOURCE PREFIXES

LF or LM	National	MC	Motorola
NE or SE	Signetics	uA	Fairchild
RM or RC	Raytheon		

2. Unique Circuit Designator Including Temperature Range

MUST CONTAIN THREE TO SEVEN CHARACTERS

(From Individual Data Sheets)

Examples:

022M	1414
101A	75450B
107	78L05AC

3. Package

MUST CONTAIN ONE OR TWO LETTERS

J, JG, KA, KC, KD, L, LA, LP, ND, P, U, or W
(From Pin-Connection Diagram on Individual Data Sheet)

4. MIL-STD-883B Method 5004, Class B

NOT USED WITH PART NUMBERS HAVING AN SN PREFIX

5. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

(From Dash No. Column of Following Table)

PACKAGES	SOLDER-DIPPED LEADS	INSULATOR	ORDER DASH NO
DUAL-IN-LINE PACKAGES			
J, JG, N, ND, P	No	No	00
J, N, P, JG	Yes	No	10
CERAMIC FLAT PACKAGES			
U, W	No	No	00
U, W	Yes	No	10
PLUG-IN PACKAGES			
L, LA, LP	No	No	00
L, LA, LP	Yes	No	10
POWER PACKAGES			
KA	No	No	N/A
KC	No	No	N/A
KD	No	No	N/A

Circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

Flat (U, W)
- Barnes Carrier
- Milton Ross Carrier

Dual-In-Line (J, JG, N, ND, P)
- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier
- Sectioned Cardboard Box
- Individual Plastic Box

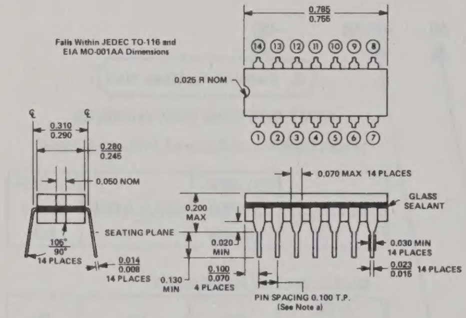
Plug-In (L, LA, LP)
- Barnes Carrier
- Sectioned Cardboard Box
- Individual Cardboard Box

LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

J ceramic dual-in-line package (inch dimensions, see page 46 for metric dimensions)

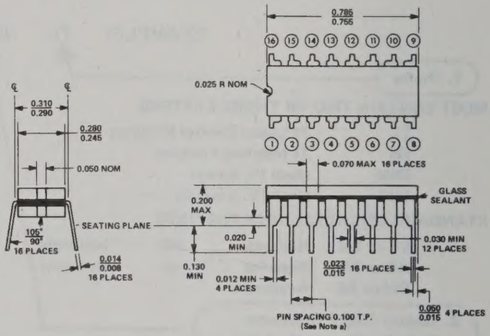
These hermetically sealed dual-in-line packages consist of a ceramic, ceramic cap, and a 14-or 16-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (—00) require no additonal cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC (INCH)


Falls Within JEDEC TO-116 and
EIA MO-001AA Dimensions
0.785
0.755
14 13 12 11 10 9 8
0.025 R NOM
1 2 3 4 5 6 7
℄ ℄
0.310
0.290
0.280
0.245
0.050 NOM
0.070 MAX 14 PLACES
GLASS SEALANT
0.200 MAX
SEATING PLANE
0.020 MIN
0.030 MIN 14 PLACES
105°
90°
14 PLACES
0.014
0.008
14 PLACES
0.130 MIN
0.100
0.070
4 PLACES
0.023
0.015
14 PLACES
PIN SPACING 0.100 T.P.
(See Note a)

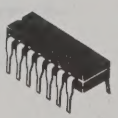
Falls Within JEDEC TO-116 and
MO-001 AA Dimensions

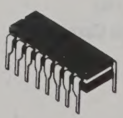
16- PIN J CERAMIC (INCH)


0.785
0.755
16 15 14 13 12 11 10 9
0.025 R NOM
1 2 3 4 5 6 7 8
℄ ℄
0.310
0.290
0.280
0.245
0.050 NOM
0.070 MAX 16 PLACES
GLASS SEALANT
0.200 MAX
SEATING PLANE
0.020 MIN
0.030 MIN 12 PLACES
105°
90°
16 PLACES
0.014
0.008
16 PLACES
0.130 MIN
0.012 MIN 4 PLACES
0.023
0.015
16 PLACES
0.050
0.015
4 PLACES
PIN SPACING 0.100 T.P.
(See Note a)

NOTES: a. Each pin center line is located within 0.010 of its true longitudinal position.

b. All dimensions are in inches unless otherwise noted.

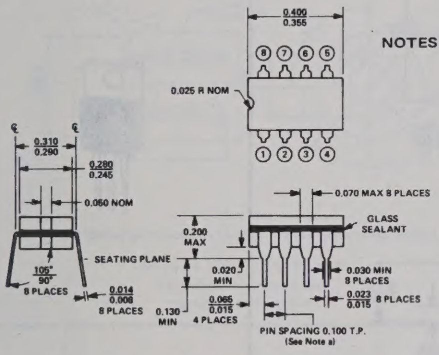




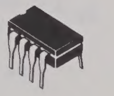
JG ceramic dual-in-line package (inch dimensions, see page 47 for metric dimensions)

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

8-PIN JG CERAMIC
(INCH)

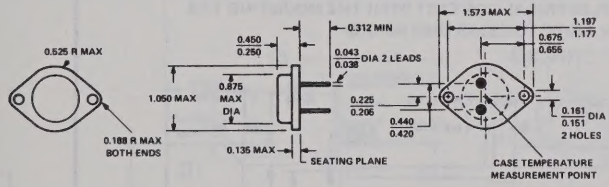

0.400
0.355
⑧ ⑦ ⑥ ⑤
① ② ③ ④
0.025 R NOM
℄ ℄
0.310
0.290
0.280
0.245
0.050 NOM
105°
90°
8 PLACES
0.014
0.008
8 PLACES
SEATING PLANE
0.070 MAX 8 PLACES
GLASS SEALANT
0.200 MAX
0.020 MIN
0.130 MIN
0.065
0.015
4 PLACES
0.030 MIN
8 PLACES
0.023
0.015
8 PLACES
PIN SPACING 0.100 T.P.
(See Note a)

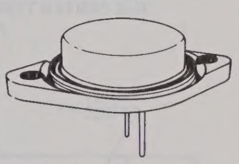
NOTES: a. Each center line is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



KA (TO-3) package (inch dimensions, see page 47 for metric dimensions)

ALL JEDEC TO-3 DIMENSIONS AND NOTES ARE APPLICABLE
(INCH)


0.525 R MAX
0.188 R MAX
BOTH ENDS
1.050 MAX
0.875
MAX
DIA
0.450
0.250
0.312 MIN
0.043
0.038
DIA 2 LEADS
0.135 MAX
SEATING PLANE
1.573 MAX
1.197
1.177
0.675
0.655
0.225
0.205
0.440
0.420
0.161
0.151
DIA
2 HOLES
CASE TEMPERATURE
MEASUREMENT POINT



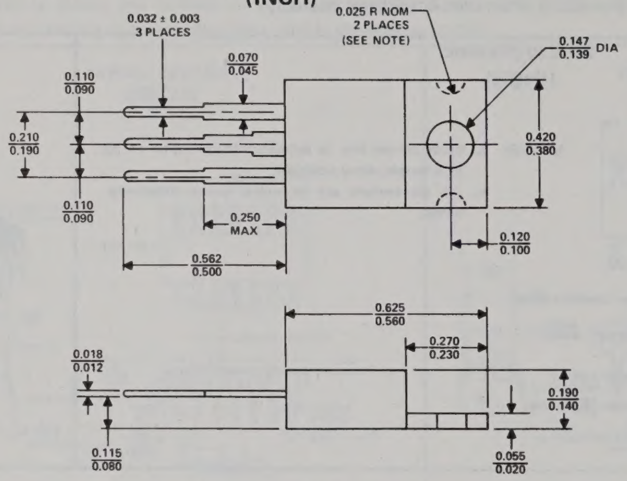
All dimensions are in inches

LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

KC (TO-220AB) package (inch dimensions, see page 48 for metric dimensions)

THE CENTER TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB
FALLS WITHIN JEDEC TO-220AB DIMENSIONS

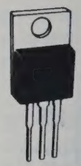
(INCH)



0.032 ± 0.003
3 PLACES
0.025 R NOM
2 PLACES
(SEE NOTE)
0.147
0.139
DIA
0.070
0.045
0.110
0.090
0.210
0.190
0.110
0.090
0.420
0.380
0.250
MAX
0.120
0.100
0.562
0.500
0.625
0.560
0.270
0.230
0.018
0.012
0.190
0.140
0.115
0.080
0.055
0.020

All dimensions are in inches

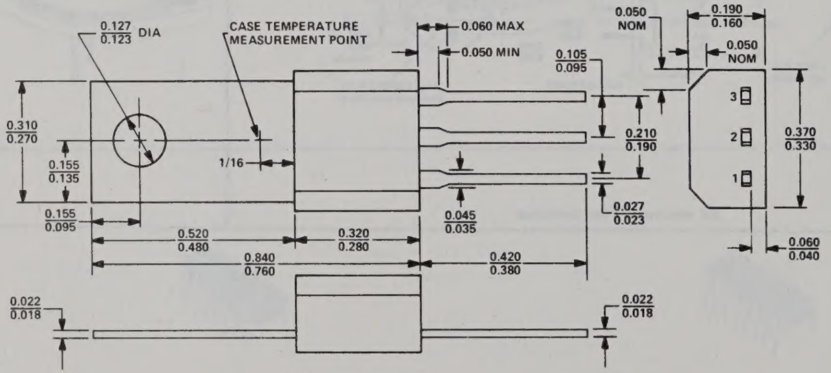
NOTE: Notches may or may not be present.



KD (TO-202AB) package (inch dimensions, see page 48 for metric dimensions)

THE CENTER TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB
FALLS WITHIN JEDEC TO-202AB DIMENSIONS

(INCH)



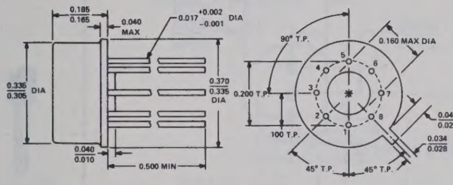
0.127
0.123
DIA
CASE TEMPERATURE
MEASUREMENT POINT
0.060 MAX
0.050 MIN
0.105
0.095
0.050
NOM
0.190
0.160
0.050
NOM
0.310
0.270
0.155
0.135
1/16
3
2
1
0.210
0.190
0.370
0.330
0.155
0.095
0.520
0.480
0.320
0.280
0.045
0.035
0.027
0.023
0.060
0.040
0.840
0.760
0.420
0.380
0.022
0.018
0.022
0.018

All dimensions are in inches

L and LA plug-in packages (inch dimensions, see page 49 for metric dimensions

These hermetically sealed plug-in packages each consist of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (—00) require no additional cleaning or processing when used in soldered assembly.

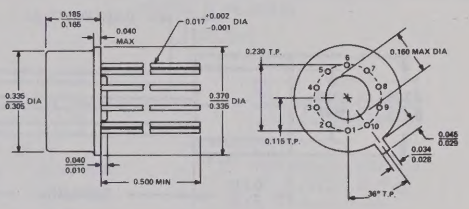
8-PIN L
(INCH)


0.185
0.165
0.040
MAX
0.017 +0.002 −0.001 DIA
0.335
0.305
DIA
0.370
0.335
DIA
0.040
0.010
0.500 MIN
90° T.P.
0.160 MAX DIA
0.200 T.P.
100 T.P.
1
2
3
4
5
6
7
8
0.045
0.029
0.034
0.028
45° T.P.
45° T.P.

All dimensions are in inches unless otherwise noted.

Same as JEDEC TO-99 and
MO-002AK except for
diameter of standoff

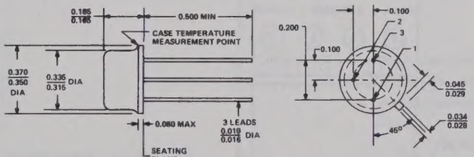
10-PIN L
(INCH)


0.185
0.165
0.040
MAX
0.017 +0.002 −0.001 DIA
0.335
0.305
DIA
0.370
0.335
DIA
0.040
0.010
0.500 MIN
0.230 T.P.
0.160 MAX DIA
0.115 T.P.
1
2
3
4
5
6
7
8
9
10
0.045
0.029
0.034
0.028
36° T.P.

All dimensions are in inches inless otherwise noted.

Same as JEDEC TO-100 and
MO-006AD except for
diameter of standoff

3-PIN LA
(INCH)


0.185
0.165
0.500 MIN
CASE TEMPERATURE
MEASUREMENT POINT
0.370
0.350
DIA
0.335
0.315
DIA
0.050 MAX
3 LEADS
0.019
0.016
DIA
SEATING
PLANE
0.200
0.100
0.100
1
2
3
0.045
0.029
0.034
0.028
45°

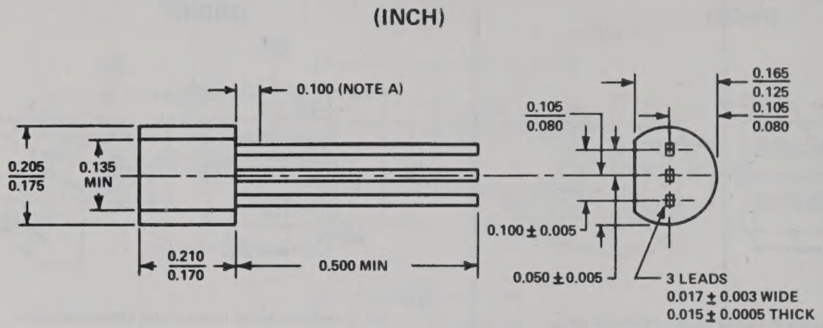
Same as JEDEC TO-39
except for reduced can height

All dimensions are in inches unless otherwise noted.

LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

LP silect plastic package (inch dimensions, see page 50 for metric dimensions)

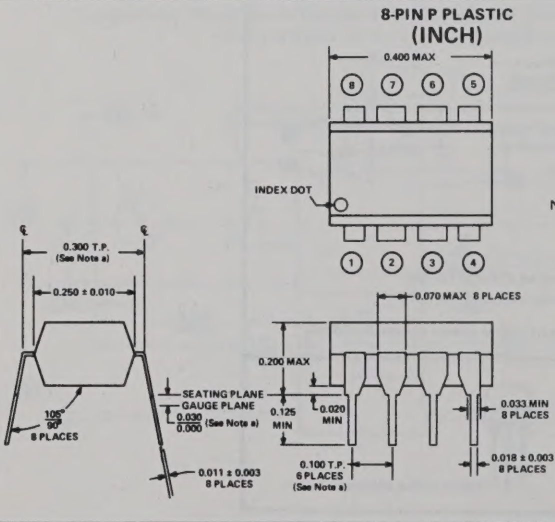
The silect package is an encapsulation in a plastic compound specifically designed for this purpose. The package will withstand soldering temperatures without deformation. The package exhibits stable characteristics under high-humidity conditions and is capable of meeting MIL-STD-202C, Method 106B.


(INCH)
0.100 (NOTE A)
0.205
0.175
0.135
MIN
0.210
0.170
0.500 MIN
0.105
0.080
0.165
0.125
0.105
0.080
0.100 ± 0.005
0.050 ± 0.005
3 LEADS
0.017 ± 0.003 WIDE
0.015 ± 0.0005 THICK

NOTES: A. Lead dimensions are not controlled in this area.
B. All dimensions are in inches.

P plastic dual-in-line package (inch dimensions, see page 50 for metric dimensions)

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

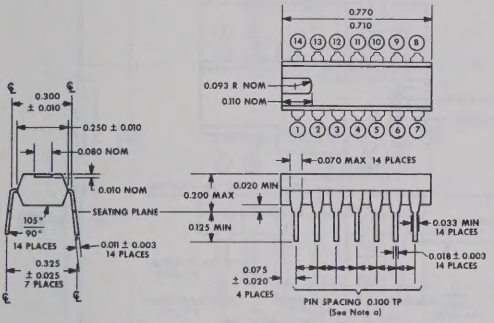

8-PIN P PLASTIC
(INCH)
0.400 MAX
⑧ ⑦ ⑥ ⑤
INDEX DOT
① ② ③ ④
℄
℄
0.300 T.P.
(See Note a)
0.250 ± 0.010
105°
90°
8 PLACES
SEATING PLANE
GAUGE PLANE
0.030
0.000 (See Note a)
0.011 ± 0.003
8 PLACES
0.070 MAX 8 PLACES
0.200 MAX
0.125
MIN
0.020
MIN
0.033 MIN
8 PLACES
0.100 T.P.
6 PLACES
(See Note a)
0.018 ± 0.003
8 PLACES

NOTES: a. Each pin is within 0.005 radius of true position (T.P.) at the guage plane with maximum material condition and unit installed.
b. All dimensions are in inches unless otherwise noted.

N plastic dual-in-line package (inch dimensions, see page 51 for metric dimensions)

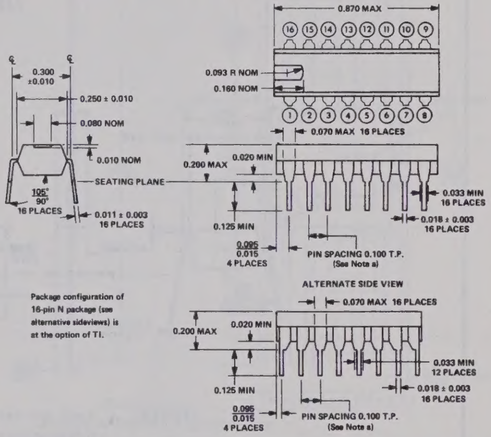
These dual-in-line packages consist of a circuit mounted on a 14-or 16-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (—00) require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC
(INCH)


0.770
0.710
14 13 12 11 10 9 8
1 2 3 4 5 6 7
0.093 R NOM
0.110 NOM
℄ ℄
0.300 ± 0.010
0.250 ± 0.010
0.080 NOM
0.010 NOM
SEATING PLANE
105°
90°
14 PLACES
0.011 ± 0.003
14 PLACES
0.325
± 0.025
7 PLACES
℄ ℄
0.070 MAX 14 PLACES
0.020 MIN
0.200 MAX
0.125 MIN
0.033 MIN
14 PLACES
0.018 ± 0.003
14 PLACES
0.075
± 0.020
4 PLACES
PIN SPACING 0.100 TP
(See Note a)

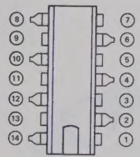
Falls Within JEDEC TO-116 and
MO-001AA Dimensions

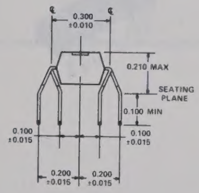
16-PIN N PLASTIC
(INCH)


0.870 MAX
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
0.093 R NOM
0.160 NOM
℄ ℄
0.300
±0.010
0.250 ± 0.010
0.080 NOM
0.010 NOM
SEATING PLANE
105°
90°
16 PLACES
0.011 ± 0.003
16 PLACES
0.070 MAX 16 PLACES
0.020 MIN
0.200 MAX
0.125 MIN
0.033 MIN
16 PLACES
0.018 ± 0.003
16 PLACES
0.095
0.015
4 PLACES
PIN SPACING 0.100 T.P.
(See Note a)
ALTERNATE SIDE VIEW
0.070 MAX 16 PLACES
0.200 MAX
0.020 MIN
0.125 MIN
0.033 MIN
12 PLACES
0.018 ± 0.003
16 PLACES
0.095
0.015
4 PLACES
PIN SPACING 0.100 T.P.
(See Note a)

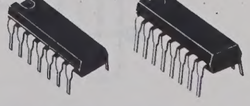
Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.

QUAD-IN-LINE LEAD CONFIGURATION


8 9 10 11 12 13 14
7 6 5 4 3 2 1


℄ ℄
0.300
±0.010
0.210 MAX
SEATING
PLANE
0.100 MIN
0.100
±0.015
0.100
±0.015
0.200
±0.015
0.200
±0.015

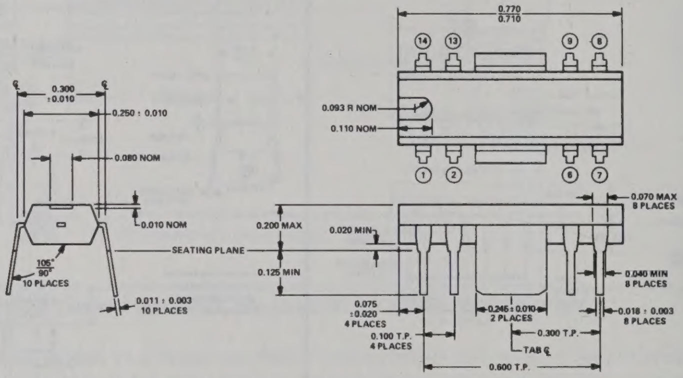
NOTES:
a. Each pin center line is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



ND plastic package (inch dimensions, see page 52 for metric dimensions)

This dual-in-line package consists of a circuit mounted on an 8-lead, 2-tab frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting rows on 0.300-inch centers. Once the leads are compressed to 0.300-inch separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Pin positions 3, 4, 5, 10, 11, and 12 are occupied by two tabs which facilitate attachment of heat sinks. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

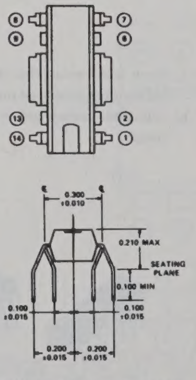
ND PLASTIC
(INCH)


0.770
0.710
⑭ ⑬ ⑨ ⑧
① ② ⑥ ⑦
0.093 R NOM
0.110 NOM
℄ 0.300 ±0.010 ℄
0.250 ± 0.010
0.080 NOM
0.010 NOM
105°
90°
10 PLACES
SEATING PLANE
0.011 ± 0.003
10 PLACES
0.200 MAX
0.125 MIN
0.020 MIN
0.070 MAX
8 PLACES
0.040 MIN
8 PLACES
0.075
±0.020
4 PLACES
0.245 ± 0.010
2 PLACES
0.018 ± 0.003
8 PLACES
0.100 T.P.
4 PLACES
0.300 T.P.
TAB ℄
0.600 T.P.

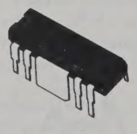
NOTES: a. Each pin (or tab) center line is located within 0.005 of its true longitudinal position (T.P.)

b. All dimensions are in inches unless otherwise noted.

QUAD-IN-LINE LEAD CONFIGURATION


⑧ ⑨ ⑬ ⑭
⑦ ⑥ ② ①
℄ 0.300 ±0.010 ℄
0.210 MAX
SEATING PLANE
0.100 MIN
0.100
±0.015
0.100
±0.015
0.200
±0.015
0.200
±0.015

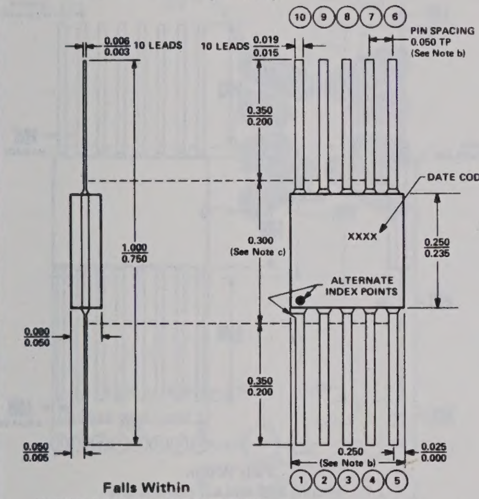
All dimensions are in inches



U ceramic flat packages (inch dimensions, see page 53 for metric dimensions)

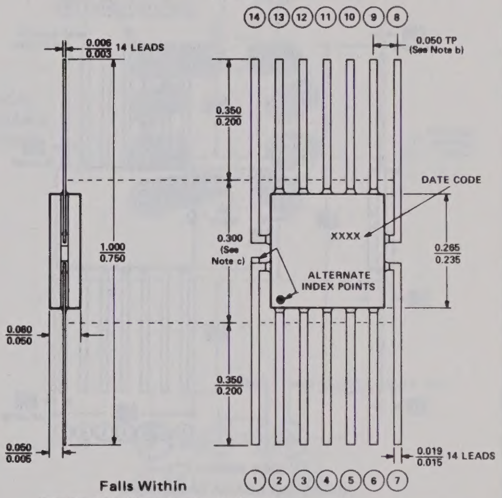
These flat packages consist of a ceramic base, ceramic cap, and 10- or 14-lead frame. Circuit bars are alloy-mounted. Hermetic sealing is accomplished with glass. Tin-plated leads require no additional cleaning or processing when used in soldered assembly.

10-PIN U (INCH)


10 9 8 7 6
0.006 / 0.003 10 LEADS
10 LEADS 0.019 / 0.015
PIN SPACING 0.050 TP (See Note b)
0.350 / 0.200
DATE CODE
XXXX
0.300 (See Note c)
0.250 / 0.235
1.000 / 0.750
ALTERNATE INDEX POINTS
0.080 / 0.050
0.350 / 0.200
0.050 / 0.005
0.250 (See Note b)
0.025 / 0.000
1 2 3 4 5

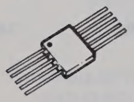
Falls Within
JEDEC MO-004AE Dimensions

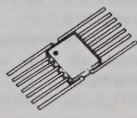
14-PIN U (INCH)


14 13 12 11 10 9 8
0.006 / 0.003 14 LEADS
0.050 TP (See Note b)
0.350 / 0.200
DATE CODE
XXXX
0.300 (See Note c)
1.000 / 0.750
ALTERNATE INDEX POINTS
0.265 / 0.235
0.080 / 0.050
0.350 / 0.200
0.050 / 0.005
0.019 / 0.015 14 LEADS
1 2 3 4 5 6 7

Falls Within
JEDEC MO-004AA Dimensions

NOTES:
a. All dimensions are in inches.
b. Leads are within 0.005 radius of true position (TP) at maximum material condition.
c. These dimensions determine a zone within which all body and lead irregularities lie.

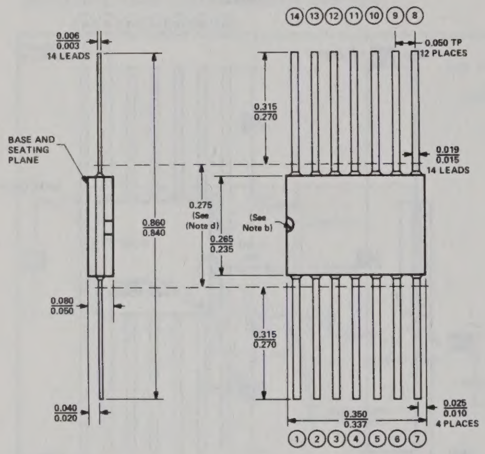




W ceramic flat packages (inch dimensions, see page 54 for metric dimensions)

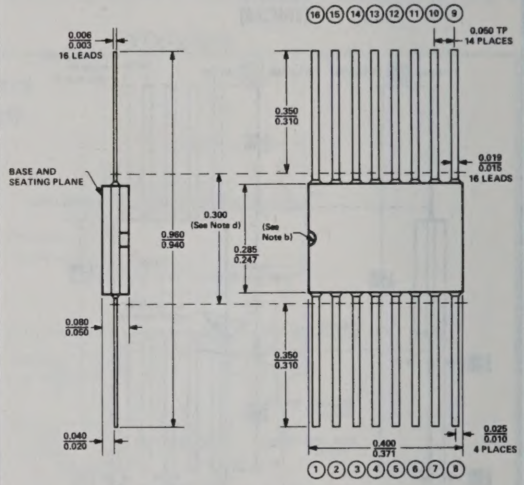
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14- or 16-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC
(INCH)


14 13 12 11 10 9 8
0.006
0.003
14 LEADS
0.050 TP
12 PLACES
0.315
0.270
BASE AND SEATING PLANE
0.019
0.015
14 LEADS
0.275 (See (Note d)
(See Note b)
0.860
0.840
0.265
0.235
0.080
0.050
0.315
0.270
0.040
0.020
0.350
0.337
0.025
0.010
4 PLACES
1 2 3 4 5 6 7

Falls Within
JEDEC MO-004AA Dimensions

16-PIN W CERAMIC
(INCH)


16 15 14 13 12 11 10 9
0.050 TP
14 PLACES
0.006
0.003
16 LEADS
0.350
0.310
BASE AND SEATING PLANE
0.019
0.015
16 LEADS
0.300 (See Note d)
(See Note b)
0.960
0.940
0.285
0.247
0.080
0.050
0.350
0.310
0.040
0.020
0.400
0.371
0.025
0.010
4 PLACES
1 2 3 4 5 6 7 8

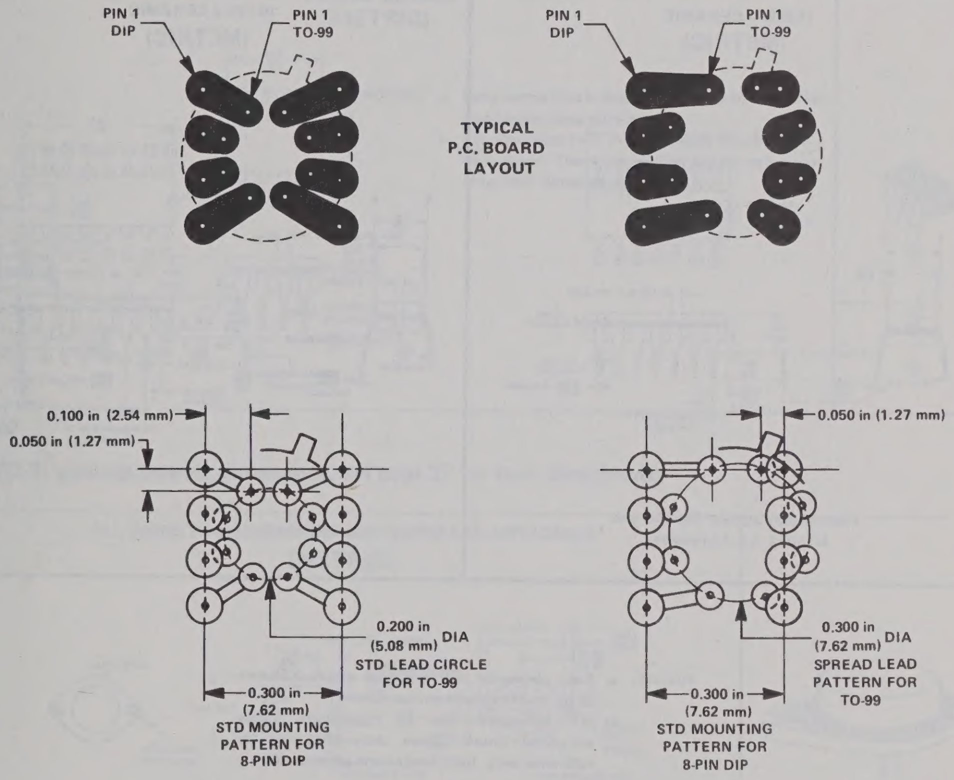
Falls Within
JEDEC MO-004AG Dimensions

NOTES:

a. All dimensions are in inches.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.

14 PIN

16 PIN


PIN 1
DIP
PIN 1
TO-99
TYPICAL
P.C. BOARD
LAYOUT
PIN 1
DIP
PIN 1
TO-99
0.100 in (2.54 mm)
0.050 in (1.27 mm)
0.200 in
(5.08 mm) DIA
STD LEAD CIRCLE
FOR TO-99
0.300 in
(7.62 mm)
STD MOUNTING
PATTERN FOR
8-PIN DIP
0.050 in (1.27 mm)
0.300 in
(7.62 mm) DIA
SPREAD LEAD
PATTERN FOR
TO-99
0.300 in
(7.62 mm)
STD MOUNTING
PATTERN FOR
8-PIN DIP

0.200-DIAMETER STANDARD LEAD CIRCLE FOR TO-99

0.300-DIAMETER SPREAD LEAD CIRCLE FOR TO-99

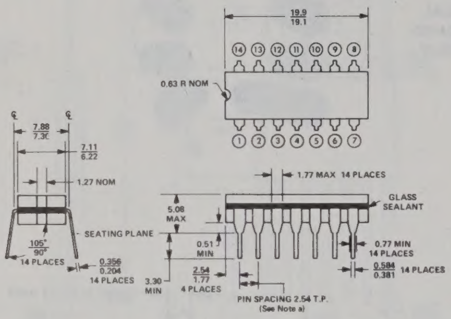
PRINTED CIRCUIT BOARD PATTERN THAT ALLOWS INTERCHANGEABILITY OF 8-PIN DUAL-IN-LINE PACKAGE WITH TO-99 PLUG-IN PACKAGE

LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

J ceramic dual-in-line packages (metric dimensions, see page 36 for inch dimensions)

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-or 16-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7.62-mm centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (—00) require no additional cleaning or processing when used in soldered assembly.

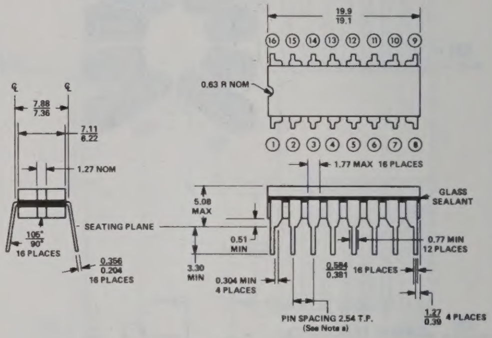
14-PIN J CERAMIC
(METRIC)



19.9 / 19.1
⑭ ⑬ ⑫ ⑪ ⑩ ⑨ ⑧
0.63 R NOM
① ② ③ ④ ⑤ ⑥ ⑦
℄ ℄
7.88 / 7.3C
7.11 / 6.22
1.27 NOM
SEATING PLANE
105° / 90° 14 PLACES
0.356 / 0.204 14 PLACES
1.77 MAX 14 PLACES
GLASS SEALANT
5.08 MAX
0.51 MIN
3.30 MIN
2.54 / 1.77 4 PLACES
0.77 MIN 14 PLACES
0.584 / 0.381 14 PLACES
PIN SPACING 2.54 T.P. (See Note a)

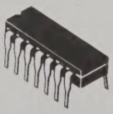
Falls Within JEDEC TO-116 and
MO-001 AA Dimensions

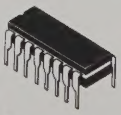
16-PIN J CERAMIC
(METRIC)



19.9 / 19.1
⑯ ⑮ ⑭ ⑬ ⑫ ⑪ ⑩ ⑨
0.63 R NOM
① ② ③ ④ ⑤ ⑥ ⑦ ⑧
℄ ℄
7.88 / 7.36
7.11 / 6.22
1.27 NOM
SEATING PLANE
105° / 90° 16 PLACES
0.356 / 0.204 16 PLACES
1.77 MAX 16 PLACES
GLASS SEALANT
5.08 MAX
0.51 MIN
3.30 MIN
0.304 MIN 4 PLACES
0.77 MIN 12 PLACES
0.584 / 0.381 16 PLACES
PIN SPACING 2.54 T.P. (See Note a)
1.27 / 0.39 4 PLACES

NOTES:
a. Each pin center line is located within 0.26 mm of its true longitudinal position.
b. All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.

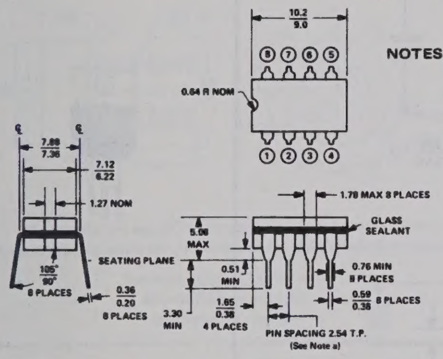




JG ceramic dual-in-line package (metric dimensions, see page 37 for inch dimensions)

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. The package is intended for insertion in mounting-hole rows on 7.62-mm centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

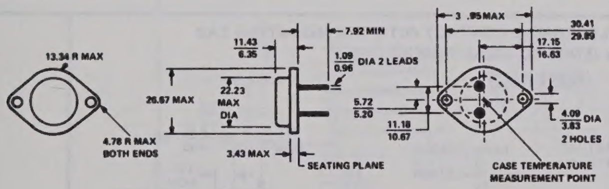
8-PIN JG CERAMIC
(METRIC)


10.2
9.0
⑧ ⑦ ⑥ ⑤
0.64 R NOM
① ② ③ ④
℄
℄
7.88
7.36
7.12
6.22
1.27 NOM
SEATING PLANE
105°
90°
8 PLACES
0.36
0.20
8 PLACES
1.78 MAX 8 PLACES
GLASS SEALANT
5.08 MAX
0.51 MIN
3.30 MIN
1.65
0.38
4 PLACES
0.76 MIN
8 PLACES
0.59
0.36
8 PLACES
PIN SPACING 2.54 T.P.
(See Note a)

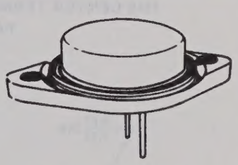
NOTES:
a. Each center line is located within 0.26-mm of its true longitudinal position
b. All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.

KA (TO-3) package (metric dimensions, see page 37 for inch dimensions)

ALL JEDEC TO-3 DIMENSIONS AND NOTES ARE APPLICABLE
(METRIC)


13.34 R MAX
4.78 R MAX
BOTH ENDS
11.43
6.35
7.92 MIN
1.09
0.96
DIA 2 LEADS
26.67 MAX
22.23
MAX
DIA
3.43 MAX
SEATING PLANE
3 .95MAX
30.41
29.89
17.15
16.63
5.72
5.20
11.18
10.67
4.09
3.83
DIA
2 HOLES
CASE TEMPERATURE
MEASUREMENT POINT

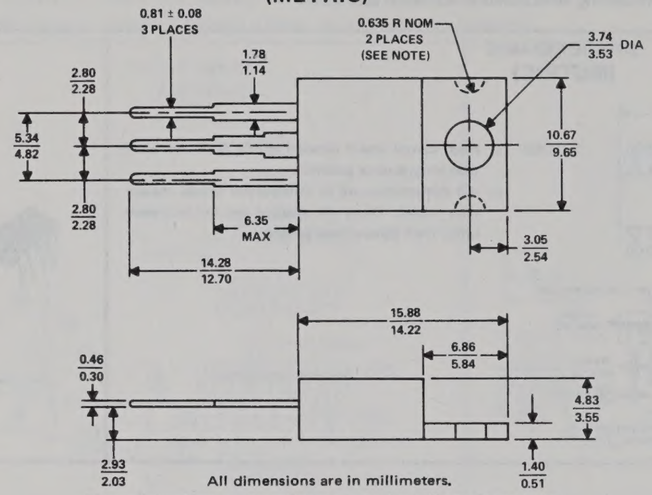
All dimensions are in millimeters
These dimensions are for reference only. Inch dimensions govern.



KC (TO-220AB) package (metric dimensions, see page 38 for inch dimensions)

THE CENTER TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB
FALLS WITHIN JEDEC TO-220AB DIMENSIONS

(METRIC)


0.81 ± 0.08
3 PLACES
0.635 R NOM
2 PLACES
(SEE NOTE)
3.74/3.53 DIA
1.78/1.14
2.80/2.28
5.34/4.82
10.67/9.65
2.80/2.28
6.35 MAX
3.05/2.54
14.28/12.70
15.88/14.22
6.86/5.84
0.46/0.30
4.83/3.55
2.93/2.03
1.40/0.51

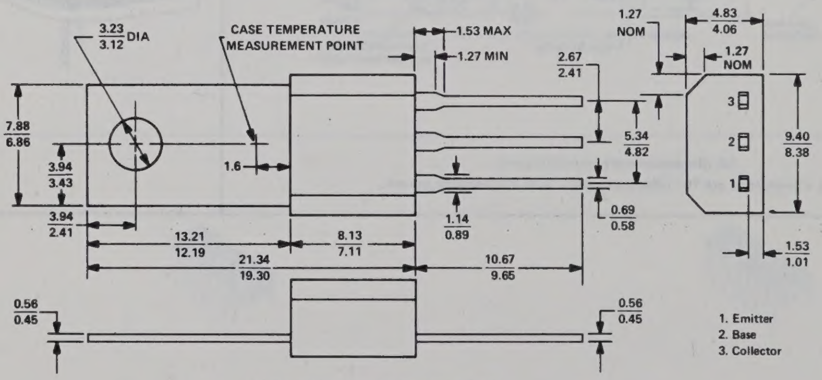
All dimensions are in millimeters.
These dimensions are for reference only. Inch dimensions govern.

NOTE: Notches may or may not be present.

KD (TO-202AB) package (metric dimensions, see page 38 for inch dimensions)

THE CENTER TERMINAL IS IN ELECTRICAL CONTACT WITH THE MOUNTING TAB
FALLS WITHIN JEDEC TO-202AB DIMENSIONS

(METRIC)


3.23/3.12 DIA
CASE TEMPERATURE
MEASUREMENT POINT
1.53 MAX
1.27 MIN
1.27 NOM
4.83/4.06
1.27 NOM
2.67/2.41
7.88/6.86
3.94/3.43
1.6
5.34/4.82
9.40/8.38
3
2
1
1.14/0.89
0.69/0.58
3.94/2.41
13.21/12.19
8.13/7.11
21.34/19.30
10.67/9.65
1.53/1.01
0.56/0.45
0.56/0.45

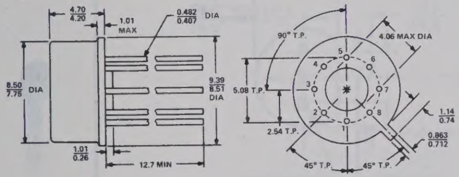
1. Emitter
2. Base
3. Collector

All dimensions are in millimeters
These dimensions are for reference only. Inch dimensions govern.

L and LA plug-in packages (metric dimensions, see page 39 for inch dimensions)

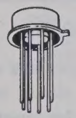
These hermetically sealed plug-in packages each consist of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

8-PIN L
(METRIC)

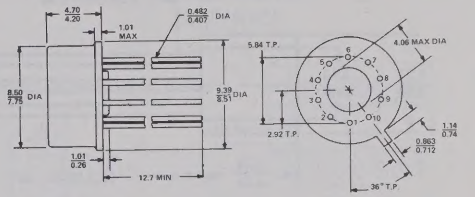

4.70
4.20
1.01
MAX
0.482
0.407
DIA
8.50
7.75
DIA
9.39
8.51
DIA
1.01
0.26
12.7 MIN
90° T.P.
4.06 MAX DIA
5.08 T.P.
2.54 T.P.
1
2
3
4
5
6
7
8
1.14
0.74
0.863
0.712
45° T.P.
45° T.P.

All dimensions are in millimeters unless otherwise noted.
These dimensions are for reference only. Inch dimensions govern.

Same as JEDEC TO-99 and
MO-002AK except for
diameter of standoff

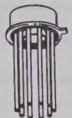


10-PIN L
(METRIC)

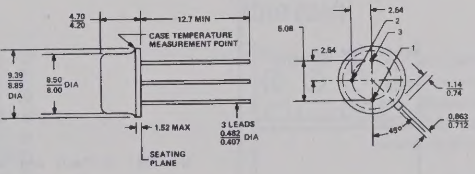

4.70
4.20
1.01
MAX
0.482
0.407
DIA
8.50
7.75
DIA
9.39
8.51
DIA
1.01
0.26
12.7 MIN
5.84 T.P.
2.92 T.P.
4.06 MAX DIA
1
2
3
4
5
6
7
8
9
10
1.14
0.74
0.863
0.712
36° T.P.

All dimensions are in millimeters unless otherwise noted.
These dimensions are for reference only. Inch dimensions govern.

Same as JEDEC TO-100 and
MO-006AD except for
diameter of standoff

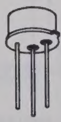


3-PIN LA
(METRIC)


4.70
4.20
12.7 MIN
CASE TEMPERATURE
MEASUREMENT POINT
9.39
8.89
DIA
8.50
8.00
DIA
1.52 MAX
SEATING
PLANE
3 LEADS
0.482
0.407
DIA
5.08
2.54
2.54
2
3
1
1.14
0.74
0.863
0.712
45°

Same as JEDEC TO-39
except for reduced can height

All dimensions are in millimeters unless otherwise noted.
These dimensions are for reference only. Inch dimensions govern.

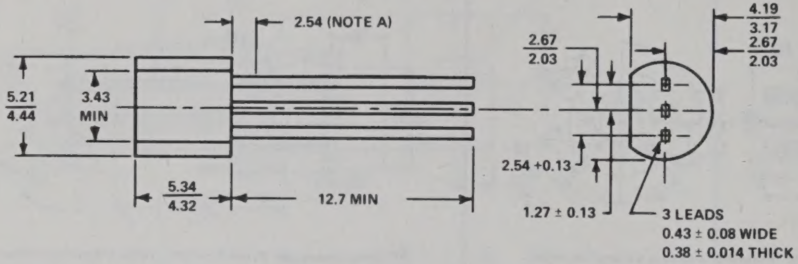


LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

LP silect plastic package (metric dimensions, see page 40 for inch dimensions)

The silect package is an encapsulation in a plastic compound specifically designed for this purpose. The package will withstand soldering temperatures without deformation. The package exhibits stable characteristics under high-humidity conditions and is capable of meeting MIL-STD-202C, Method 106B.

(METRIC)

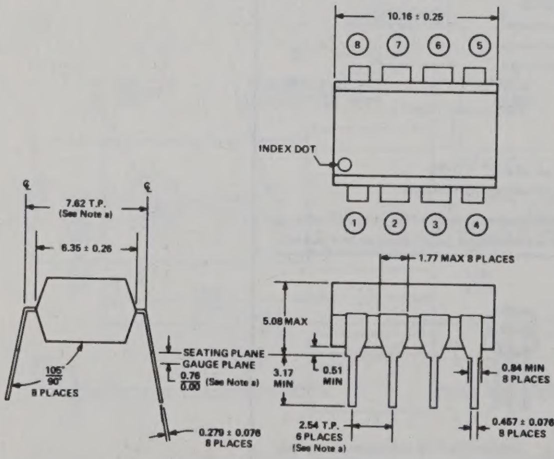

2.54 (NOTE A)
5.21
4.44
3.43
MIN
5.34
4.32
12.7 MIN
2.67
2.03
4.19
3.17
2.67
2.03
2.54 +0.13
1.27 ± 0.13
3 LEADS
0.43 ± 0.08 WIDE
0.38 ± 0.014 THICK

NOTES: A. Lead dimensionsare not controlled in this area.
B. All dimensions are in millimeters. These dimensions are for reference only. Inch dimensions govern.

P plastic dual-in-line package (metric dimensions, see page 40 for inch dimensions)

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7.62-mm centers. Once the leads are compressed to 7.62-mm separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC
(METRIC)

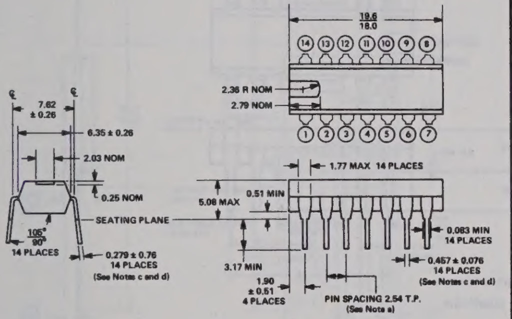

10.16 ± 0.25
8
7
6
5
INDEX DOT
1
2
3
4
7.62 T.P.
(See Note a)
6.35 ± 0.26
1.77 MAX 8 PLACES
5.08 MAX
SEATING PLANE
GAUGE PLANE
0.76
0.00
(See Note a)
3.17
MIN
0.51
MIN
0.84 MIN
8 PLACES
105°
90°
8 PLACES
0.279 ± 0.076
8 PLACES
2.54 T.P.
6 PLACES
(See Note a)
0.457 ± 0.076
8 PLACES

NOTES: a. Each pin is within 0.127 mm radius of true position (T.P.) at the guage plane with maximum material condition and unit installed.
b All dimension are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.

N plastic dual-in-line packages (metric dimensions, see page 41 for inch dimensions)

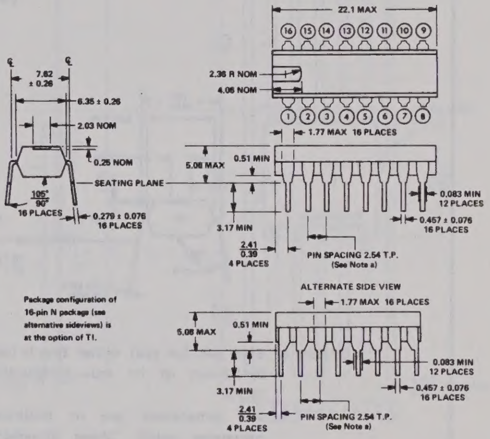
These dual-in-line packages consist of a circuit mounted on a 14- or 16-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7.62-mm centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (—00) require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC (METRIC)


19.6
18.0
⑭ ⑬ ⑫ ⑪ ⑩ ⑨ ⑧
① ② ③ ④ ⑤ ⑥ ⑦
2.36 R NOM
2.79 NOM
7.62 ± 0.26
6.35 ± 0.26
2.03 NOM
0.25 NOM
SEATING PLANE
105° 90°
14 PLACES
0.279 ± 0.76
14 PLACES
(See Notes c and d)
1.77 MAX 14 PLACES
5.08 MAX
0.51 MIN
3.17 MIN
1.90 ± 0.51
4 PLACES
0.083 MIN
14 PLACES
0.457 ± 0.076
14 PLACES
(See Notes c and d)
PIN SPACING 2.54 T.P.
(See Note a)

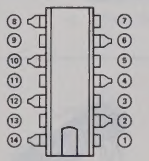
Falls Within JEDEC TO-116 and MO-001AA Dimensions

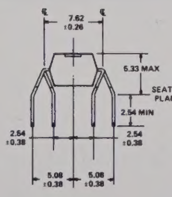
16-PIN N PLASTIC (METRIC)


22.1 MAX
⑯ ⑮ ⑭ ⑬ ⑫ ⑪ ⑩ ⑨
① ② ③ ④ ⑤ ⑥ ⑦ ⑧
2.36 R NOM
4.06 NOM
7.62 ± 0.26
6.35 ± 0.26
2.03 NOM
0.25 NOM
SEATING PLANE
105° 90°
16 PLACES
0.279 ± 0.076
16 PLACES
1.77 MAX 16 PLACES
5.08 MAX
0.51 MIN
3.17 MIN
2.41 0.39
4 PLACES
0.083 MIN
12 PLACES
0.457 ± 0.076
16 PLACES
PIN SPACING 2.54 T.P.
(See Note a)
ALTERNATE SIDE VIEW
1.77 MAX 16 PLACES
5.08 MAX
0.51 MIN
3.17 MIN
2.41 0.39
4 PLACES
0.083 MIN
12 PLACES
0.457 ± 0.076
16 PLACES
PIN SPACING 2.54 T.P.
(See Note a)

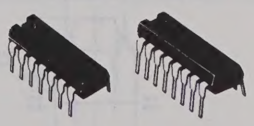
Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.

QUAD-IN-LINE LEAD CONFIGURATION


⑧ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭
⑦ ⑥ ⑤ ④ ③ ② ①


7.62 ±0.26
5.33 MAX
SEATING PLANE
2.54 MIN
2.54 ±0.38
2.54 ±0.38
5.08 ±0.38
5.08 ±0.38

NOTES:
- a. Each pin centerline is located within 0.26 mm of its true longitudinal position.
- b. All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.

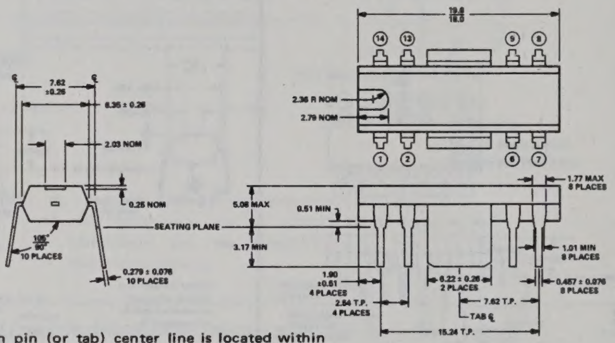


LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

ND-package (metric dimensions, see page 42 for inch dimensions)

This dual-in-line package consists of a circuit mounted onan 8-lead, 2-tab frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7.62-mm centers. Once the leads are compressed to 7.62-mm separation and inserted, sufficient tension is provided to secure the package in the board during soldering. Pin positions 3, 4, 5, 10, 11, and 12 are occupied by two tabs which facilitate attachment of heat sinks. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.

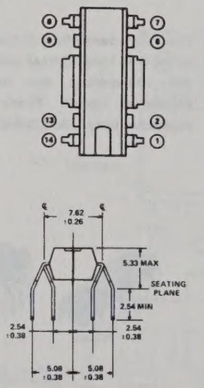
ND PLASTIC
(METRIC)



7.62 ±0.26
6.35 ± 0.26
2.03 NOM
0.25 NOM
SEATING PLANE
105°/90° 10 PLACES
0.279 ± 0.076 10 PLACES
19.8/18.0
14
13
9
8
1
2
6
7
2.36 R NOM
2.79 NOM
1.77 MAX 8 PLACES
5.08 MAX
0.51 MIN
3.17 MIN
1.01 MIN 8 PLACES
1.90 ±0.51 4 PLACES
6.22 ± 0.26 2 PLACES
0.457 ± 0.076 8 PLACES
2.54 T.P. 4 PLACES
7.62 T.P.
TAB ℄
15.24 T.P.

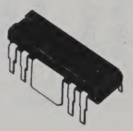
NOTES:
- a. Each pin (or tab) center line is located within 0.127 mm of its true longitudinal position (T.P.)
- b. All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.

QUAD-IN-LINE LEAD CONFIGURATION



8
9
13
14
7
6
2
1
7.62 ±0.26
5.33 MAX
SEATING PLANE
2.54 MIN
2.54 ±0.38
2.54 ±0.38
5.08 ±0.38
5.08 ±0.38

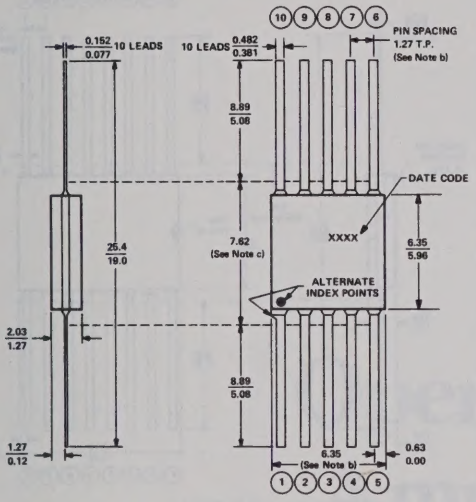
All dimensions are in millimeters.



U ceramic flat packages (metric dimensions, see page 43 for inch dimensions)

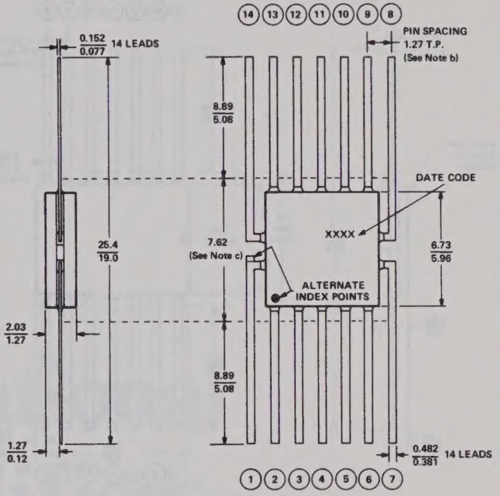
These flat packages consist of a ceramic base, ceramic cap, and 10- or 14-lead frame. Circuit bars are alloy-mounted. Hermetic sealing is accomplished with glass. Tin-plated leads require no additional cleaning or processing when used in soldered assembly.

10-PIN U
(METRIC)


10
9
8
7
6
0.152
0.077
10 LEADS
10 LEADS
0.482
0.381
PIN SPACING
1.27 T.P.
(See Note b)
8.89
5.08
DATE CODE
XXXX
25.4
19.0
7.62
(See Note c)
6.35
5.96
ALTERNATE
INDEX POINTS
2.03
1.27
8.89
5.08
1.27
0.12
6.35
(See Note b)
0.63
0.00
1
2
3
4
5

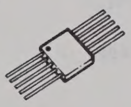
Falls Within
JEDEC MO-004AE Dimensions

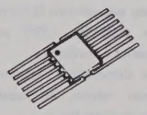
14-PIN U
(METRIC)


14
13
12
11
10
9
8
0.152
0.077
14 LEADS
PIN SPACING
1.27 T.P.
(See Note b)
8.89
5.08
DATE CODE
XXXX
25.4
19.0
7.62
(See Note c)
6.73
5.96
ALTERNATE
INDEX POINTS
2.03
1.27
8.89
5.08
1.27
0.12
0.482
0.381
14 LEADS
1
2
3
4
5
6
7

Falls Within
JEDEC MO-004AA Dimensions

NOTES:
- a. All dimensions are in millimeters. These dimensions are for reference only. Inch dimensions govern.
- b. Leads are within 0.13 mm radius of true position (TP) at maximum material condition.
- c. These dimensions determine a zone within which all body and lead irregularities lie.



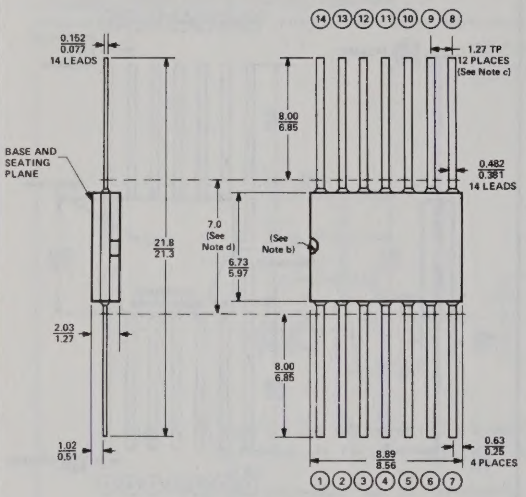


LINEAR CIRCUITS
ORDERING INSTRUCTIONS AND MECHANICAL DATA

W ceramic flat packages (metric dimensions, see page 44 for inch dimensions)

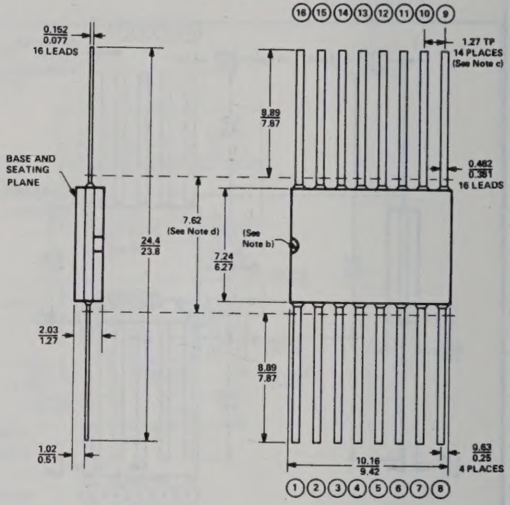
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14- or 16-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC
(METRIC)


⑭⑬⑫⑪⑩⑨⑧
0.152
0.077
14 LEADS
1.27 TP
12 PLACES
(See Note c)
8.00
6.85
BASE AND
SEATING
PLANE
0.482
0.381
14 LEADS
7.0
(See
Note d)
21.8
21.3
(See
Note b)
6.73
5.97
2.03
1.27
8.00
6.85
1.02
0.51
8.89
8.56
0.63
0.25
4 PLACES
①②③④⑤⑥⑦

Falls Within
JEDEC MO-004AA Dimensions

16-PIN W CERAMIC
(METRIC)


⑯⑮⑭⑬⑫⑪⑩⑨
0.152
0.077
16 LEADS
1.27 TP
14 PLACES
(See Note c)
8.89
7.87
BASE AND
SEATING
PLANE
0.482
0.381
16 LEADS
7.62
(See Note d)
(See
Note b)
24.4
23.8
7.24
6.27
2.03
1.27
8.89
7.87
1.02
0.51
10.16
9.42
0.63
0.25
4 PLACES
①②③④⑤⑥⑦⑧

Falls Within
JEDEC MO-004AG Dimensions

NOTES:

a. All dimensions are in millimeters. These dimensions are for reference only. Inch dimensions govern.

b. Index point is provided on cap for terminal identification only.

c. Leads are within 0.13 mm radius of true position (TP) at maximum material condition.

d. This dimension determines a zone within which all body and lead irregularities lie.

14 PIN

16 PIN

Operational Amplifiers

4

OPERATIONAL AMPLIFIER SELECTION GUIDE

OPERATIONAL AMPLIFIERS

		Input Offset Voltage MAX (mV)	Input Offset Current MAX (nA)	Input Bias Current MAX (nA)	Bandwidth TYP (MHz)	Slew Rate at Unity Gain TYP (V/μs)
Single	LM101A, LM301A	7.5	50	250	1	0.5
	LM107, LM307	7.5	50	250	1[†]	0.5[†]
	LM118, LM318	10	200	500	15	70
	LM2902	10	50	–500	1	0.5
	TL089	0.15	0.6	1	3	10
	TL702	10	5,000	15,000	30	1.7
	uA702	2	500	5,000	30	1.7
	uA709	7.5	500	1,500	10	0.3
	uA741	6	200	500	1	0.5
	uA748	6	200	500	1	0.5
	uA777	5	20	100	1	0.5
Dual	LM158, LM358	7	50	–250	1	0.5
	LM2904	10	50	–500	1	0.5
	MC1458	6	200	500	1	0.5
	RC4558	6	200	500	3	1
	TL022	5	80	250	0.8	0.5
	uA747	6	200	500	1	0.5
Quad	LM124, LM324	7	50	–250	1	0.5
	RC4136	6	200	500	3	1
	TL044	5	80	250	0.8	0.5

OPERATIONAL AMPLIFIERS WITH JFET INPUTS

		Input Offset Voltage MAX (mV)	Input Offset Current MAX (nA)	Input Bias Current MAX (nA)	Bandwidth TYP (Hz)	Slew Rate at Unity Gain TYP (V/μs)
Single	LF155, LF355	10	0.05	0.2	2.5	5
	LF155A, LF355A	2	0.01	0.05	2.5	5
	LF156, LF356	10	0.05	0.2	4.5	12
	LF156A, LF356A	2	0.01	0.05	4.5	12
	LF157, LF357	10	0.05	0.2	20	50
Dual	LF157A, LF357A	2	0.01	0.05	20	50
	LF2155, LF2355	10	0.05	0.2	2.5	5
	LF2155A, LF2355A	2	0.01	0.05	2.5	5
	LF2156, LF2356	10	0.05	0.2	4.5	12
	LF2156A, LF2356A	2	0.01	0.05	4.5	12

GLOSSARY
OPERATIONAL AMPLIFIER TERMS AND DEFINITIONS

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to zero. NOTE: The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right|$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at zero volts.

Input voltage Range (V_I)

The range of voltage that if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Maximum Peak Output Voltage Swing (V_{OM})

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP})

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

GLOSSARY
OPERATIONAL AMPLIFIER TERMS AND DEFINITIONS

Large-Signal Voltage Amplification (A_V)

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output voltage to the change in differential input voltage producing it.

Maximum-Output-Swing Bandwidth (B_{OM})

The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1)

The range of frequencies within which the open-loop voltage amplification is greater than unity.

Phase Margin (ϕ_m)

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

Gain Margin (A_m)

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Input Resistance (r_i)

The resistance between the input terminals with either input grounded.

Differential Input Resistance (r_{id})

The small-signal resistance between the two ungrounded input terminals.

Output Resistance (r_o)

The resistance between the output terminal and ground.

Input Capacitance (C_i)

The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic})

The parallel sum of the small-signal impedance between each input terminal and ground.

Output Impedance (z_o)

The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Sensitivity (k_{SVS}, $\Delta V_{IO}/\Delta V_{CC}$)

The absolute value of the ratio of the change in input offset voltage to the change in supply voltages producing it.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

Supply Voltage Rejection Ratio (k_{SVR}, $\Delta V_{CC}/\Delta V_{IO}$)

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage rejection ratio.

Equivalent Input Noise Voltage (V_n)

The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent Input Noise Current (I_n)

The current of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

Short-Circuit Output Current (I_{OS})

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.

Supply Current (I_{CC})

The current into the V_{CC} or V_{CC+} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Channel Separation (V_{o1}/V_{o2})

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

GLOSSARY
OPERATIONAL AMPLIFIER TERMS AND DEFINITIONS

Rise Time (t_r)

The time required for an output voltage step to change from 10% to 90% of its final value.

Total Response Time (Settling Time) (t_{tot})

The time between a step-function change of the input signal level and the instant at which the magnitude of the output signal reaches for the last time a specified level range (±ϵ) containing the final output signal level.

Overshoot Factor

The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal, to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

Slew Rate (SR)

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

LINEAR INTEGRATED CIRCUITS

TYPES LF155, LF155A, LF156, LF156A, LF157, LF157A, LF255, LF256, LF257, LF355, LF355A, LF356, LF356A, LF357, LF357A JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612387, JUNE 1976

- Rugged JFET's Allow Blow-Out-Free Handling Compared with MOSFET-Input Devices
- Offset Adjustment Does Not Degrade αV_{IO} or Common-Mode Rejection as in Most Bipolar Amplifiers
- Low Input Bias Current . . . 30 pA Typ
- Low Input Offset Current . . . 3 pA Typ
- Low Input Offset Voltage Temperature Coefficient . . . 5 µV/°C Typ
- High Input Impedance . . . 10^{12} Ω Typ
- High Common-Mode Rejection Ratio
- High DC Voltage Gain . . . 200 V/mV Typ
- No External Frequency Compensation Required
- Low Equivalent Input Noise Current

quick selection guides

TYPES	OPERATING FREE-AIR TEMPERATURE RANGE			MAX OFFSET VOLTAGE				
	−55°C to 125°C	−25°C to 85°C	0°C to 70°C	2.3 mV	2.5 mV	6.5 mV	7 mV	13 mV
LF1__A	●				●			
LF1__	●						●	
LF2__		●				●		
LF3__A			●	●				
LF3__			●					●

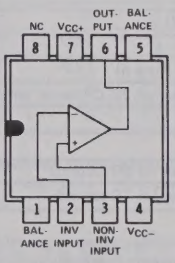
TYPES	TYP BANDWIDTH			TYP V_n		TYP		TYP SLEW RATE		
	$A_V = 5$	$A_V = 1$		f = 100 Hz		I_{CC}		$A_V = 5$	$A_V = 1$	
	20 MHz	4.5 MHz	2.5 MHz	15 nV/$\sqrt{Hz}$	25 nV/$\sqrt{Hz}$	2 mA	5 mA	50 V/µs	12 V/µs	5 V/µs
'55, '55A			●		●	●				●
'56, '56A		●		●			●		●	
'57, '57A	●			●			●	●		

description

These monolithic JFET-input operational amplifiers incorporate well-matched, high-voltage BI-FET technology (JFET's on the same chip with standard bipolar transistors). The devices feature low input bias and offset currents, low offset voltage and offset voltage temperature coefficient, coupled with offset adjustment that does not degrade temperature coefficient or common-mode rejection. The devices are also designed for wide bandwidths, high slew rate, extremely fast settling time, low equivalent input noise voltage and current, and a low 1/f corner.

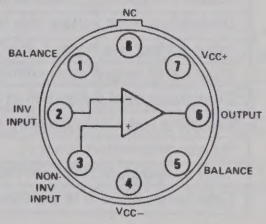
The LF155, LF155A, LF156, LF156A, LF157, and LF157A are characterized for operation over the full military temperature range of −55°C to 125°C; the LF255, LF256, and LF257 are characterized for operation from −25°C to 85°C; the LF355, LF355A, LF356, LF356A, LF357, and LF357A are characterized for operation from 0°C to 70°C.

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

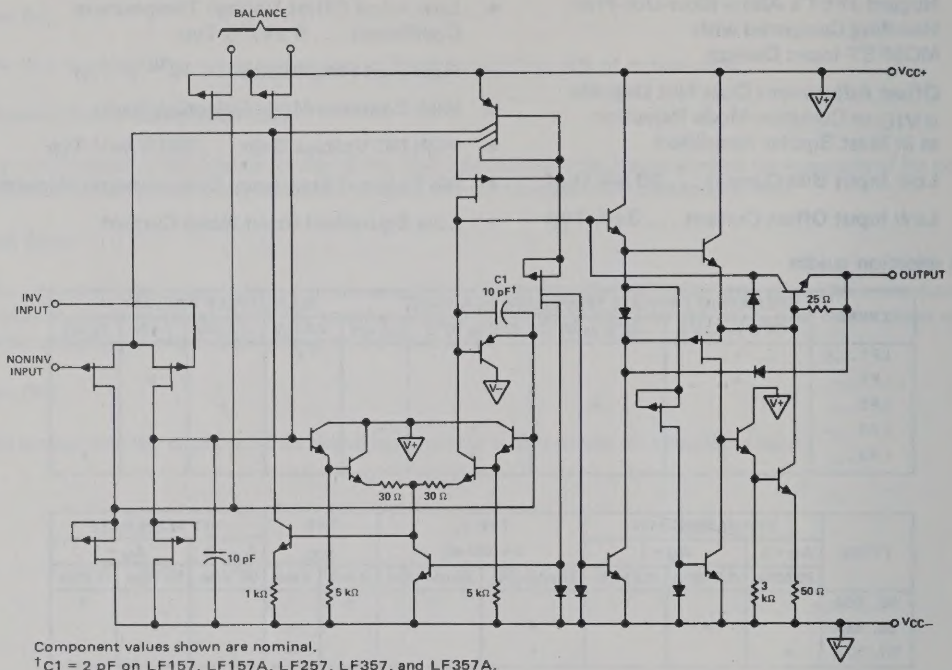
L
PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TYPES LF155, LF155A, LF156, LF156A, LF157, LF157A, LF255, LF256, LF257, LF355, LF355A, LF356, LF356A, LF357, LF357A JFET-INPUT OPERATIONAL AMPLIFIERS

schematic



Component values shown are nominal.

†C1 = 2 pF on LF157, LF157A, LF257, LF357, and LF357A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LF1−− LF1−−A	LF2−−	LF3−− LF3−−A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±40	±40	±30	V
Input voltage (see Notes 1 and 3)		±20	±20	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		670	670	670	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	JG or L package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P package	260	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.

2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.

4. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

5. For operation above 25°C, free-air temperature, refer to Dissipation Derating Curves, Section 2. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

TYPES LF155, LF156, LF157, LF255, LF256, LF257, LF355, LF356, LF357 JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LF1__			LF2__			LF3__			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω			3	5		3	5		3	10	mV
		R_S = 50 Ω,	T_A = full range			7			6.5			13	
αV_{IO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = full range		5			5			5		µV/°C
$\frac{\Delta \alpha V_{IO}}{\Delta V_{IO}}$	Change in temperature coefficient with offset voltage adjustment	R_S = 50 Ω			0.5			0.5			0.5		$\frac{\mu V/°C}{mV}$
I_{IO}	Input offset current				3	20		3	20		3	50	pA
		T_A = full range				20			1			2	nA
I_{IB}	Input bias current				30	100		30	100		30	200	pA
		T_A = full range				50			5			8	nA
V_{ICR}	Common-mode input voltage range			+11 to −11	+15 to −12		+11 to −11	+15 to −12		+10 to −10	+15 to −12		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V,	R_L = 10 kΩ	24	26		24	26		24	26		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ, V_O = ±10 V	T_A = 25°C	50	200		50	200		25	200		V/mV
			T_A = full range	25			25			15			
B_1	Unity-gain bandwidth		'55		2.5			2.5			2.5		MHz
			'56		4.5			4.5			4.5		
			'57		20			20			20		
r_i	Input resistance				10^{12}			10^{12}			10^{12}		Ω
C_i	Input capacitance				3			3			3		pF
CMRR	Common-mode rejection ratio	R_S = 50 Ω		85	100		85	100		80	100		dB
k_{SVR}*	Supply voltage rejection ratio			85	100		85	100		80	100		dB
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 100 Hz	'55		25			25			25		nV/$\sqrt{Hz}$
			'56, '57		15			15			15		
		R_S = 100 Ω, f = 1 kHz	'55		20			20			20		
			'56, '57		12			12			12		
I_n	Equivalent input noise current	f = 100 Hz			0.01			0.01			0.01		pA/$\sqrt{Hz}$
		f = 1 kHz			0.01			0.01			0.01		
I_{CC}	Supply current	No load, No signal	'55		2	4		2	4		2	4	mA
			'56, '57		5	7		5	7		5	10	

*$k_{SVR} = \Delta V_{CC\pm}/\Delta V_{IO}$.

†All characteristics are specified under open-loop operation, unless otherwise noted. Also unless otherwise noted, $V_{CC\pm}$ = ±15 V to ±20 V for LF1__ and LF2__, $V_{CC\pm}$ = ±15 V for LF3__. Full range for T_A is −55°C to 125°C for LF1__, −25°C to 85°C for LF2__, and 0°C to 70°C for LF3__.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			LF1__			LF2__			LF3__			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{tot}	Total response time (settling time)	ΔV_O = 10 V, ϵ = ±0.01%, See Figure 1	A_V = −1	'55		4			4			4		µs
				'56		1.5			1.5			1.5		
			A_V = −5	'57		1.5			1.5			1.5		
SR	Slew rate	ΔV_O = 10 V, See Figure 2	A_V = −1	'55		5			5			5		V/µs
				'56	7.5	12		7.5	12			12		
			A_V = −5	'57	30	50		30	50			50		

TYPES LF155A, LF156A, LF157A, LF355A, LF356A, LF357A JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LF1__A			LF3__A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$			1	2		1	2	mV
		$R_S = 50\ \Omega$,	T_A = full range			2.5			2.3	
α_{VIO}	Temperature coefficient of input offset voltage	$R_S = 50\ \Omega$,	T_A = full range		3	5		3	5	μV/°C
$\frac{\Delta\alpha_{VIO}}{\Delta V_{IO}}$	Change in temperature coefficient with offset voltage adjustment	$R_S = 50\ \Omega$			0.5			0.5		$\frac{\mu\text{V}/°\text{C}}{\text{mV}}$
I_{IO}	Input offset current				3	10		3	10	pA
		T_A = full range				10			1	nA
I_{IB}	Input bias current				30	50		30	50	pA
		T_A = full range				25			5	nA
V_{ICR}	Common-mode input voltage range			+11 to −11	+15 to −12		+11 to −11	+15 to −12		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V,	$R_L = 10\ k\Omega$	24	26		24	26		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $R_L = 2\ k\Omega$, $V_O = \pm 10$ V	$T_A = 25°C$	50	200		50	200		V/mV
			T_A = full range	25			25			
B_1	Unity-gain bandwidth		'55A		2.5			2.5		MHz
			'56A	4	4.5		4	4.5		
			'57A	15	20		15	20		
r_i	Input resistance				10^{12}			10^{12}		Ω
C_i	Input capacitance				3			3		pF
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$		85	100		85	100		dB
k_{SVR}*	Supply voltage rejection ratio			85	100		85	100		dB
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, f = 100 Hz	'55A		25			25		$nV/\sqrt{Hz}$
			'56A, '57A		15			15		
		$R_S = 100\ \Omega$, f = 1 kHz	'55A		20			20		
			'56A, '57A		12			12		
I_n	Equivalent input noise current	f = 100 Hz			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1 kHz			0.01			0.01		
I_{CC}	Supply current	No load, No signal	'55A		2	4		2	4	mA
			'56A, '57A		5	7		5	10	

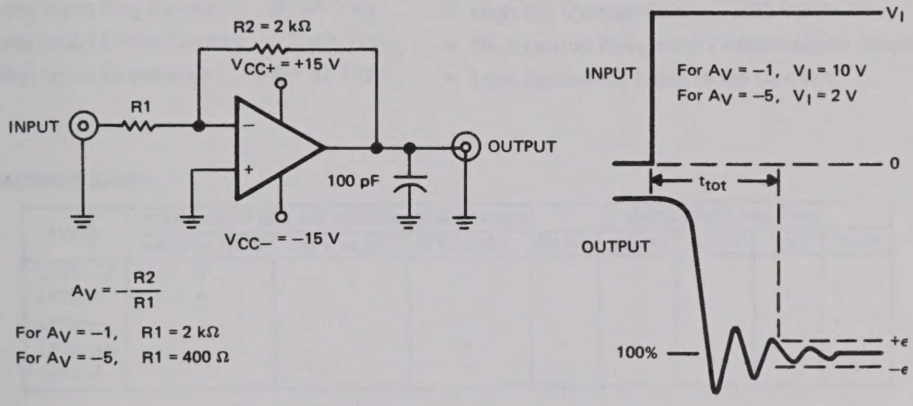
*$k_{SVR} = \Delta V_{CC\pm}/\Delta V_{IO}$.

†All characteristics are specified under open-loop operation, unless otherwise noted. Also unless otherwise noted, $V_{CC\pm} = \pm 15$ V to 20 V for LF1−−A and LF3−−A. Full range for T_A is −55°C to 125°C for LF1−−A and 0°C to 70°C for LF3—A.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			LF1__A			LF3__A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{tot}	Total response time (settling time)	$\Delta V_O = 10$ V, $\epsilon = \pm 0.01\%$, See Figure 1	$A_V = -1$	'55A		4			4		μs
				'56A		1.5			1.5		
			$A_V = -5$	'57A		1.5			1.5		
SR	Slew rate	$\Delta V_O = 10$ V, See Figure 2	$A_V = -1$	'55A	3	5		3	5		V/μs
				'56A	10	12		10	12		
			$A_V = -5$	'57A	40	50		40	50		

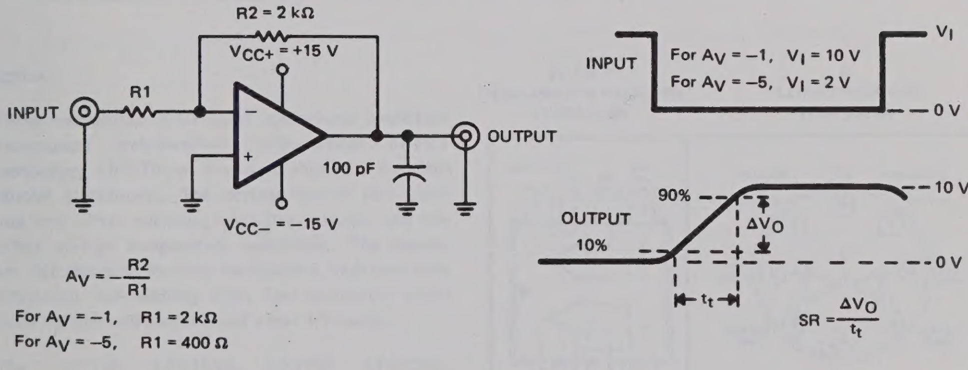
PARAMETER MEASUREMENT INFORMATION


R2 = 2 kΩ
VCC+ = +15 V
R1
INPUT
OUTPUT
100 pF
VCC– = –15 V
AV = –R2/R1
For AV = –1, R1 = 2 kΩ
For AV = –5, R1 = 400 Ω
VI
INPUT
For AV = –1, VI = 10 V
For AV = –5, VI = 2 V
0
ttot
OUTPUT
100%
+ε
–ε

TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 1—TOTAL RESPONSE TIME


R2 = 2 kΩ
VCC+ = +15 V
R1
INPUT
OUTPUT
100 pF
VCC– = –15 V
AV = –R2/R1
For AV = –1, R1 = 2 kΩ
For AV = –5, R1 = 400 Ω
VI
INPUT
For AV = –1, VI = 10 V
For AV = –5, VI = 2 V
0 V
10 V
90%
OUTPUT
10%
ΔVO
0 V
tt
SR = ΔVO/tt

TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 2—SLEW RATE

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TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME
IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

LINEAR INTEGRATED CIRCUIT

TYPES LF2155, LF2155A, LF2156, LF2156A, LF2157, LF2157A, LF2255, LF2256, LF2257, LF2355, LF2355A, LF2356, LF2356A, LF2357, LF2357A DUAL JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612420, JUNE 1976

- Rugged JFET's Allow Blow-Out-Free Handling Compared with MOSFET-Input Devices
- Low Input Bias Current . . . 30 pA Typ
- Low Input Offset Current . . . 3 pA Typ
- High Input Impedance . . . 10^{12} Ω Typ
- Low Input Offset Voltage Temperature Coefficient . . . 5 μV/°C Typ
- High Common-Mode Rejection Ratio
- High DC Voltage Gain . . . 200 V/mV Typ
- No External Frequency Compensation Required
- Low Equivalent Input Noise Current

quick selection guides

TYPES	OPERATING FREE-AIR TEMPERATURE RANGE			MAX OFFSET VOLTAGE				
	−55°C to 125°C	−25°C to 85°C	0°C to 70°C	2.3 mV	2.5 mV	6.5 mV	7 mV	13 mV
LF21––A	●				●			
LF21––	●						●	
LF22––		●				●		
LF23––A			●	●				
LF23––			●					●

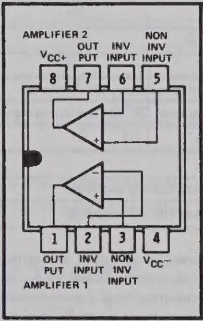
TYPES	TYP BANDWIDTH			TYP V_n f = 100 Hz		TYP I_{CC}		TYP SLEW RATE		
	$A_V = 5$	$A_V = 1$						$A_V = 5$	$A_V = 1$	
	20 MHz	4.5 MHz	2.5 MHz	15 nV/√Hz	25 nV/√Hz	2 mA	5 mA	50 V/μs	12 V/μs	5 V/μs
'55, '55A			●		●	●				●
'56, '56A		●		●			●		●	
'57, '57A	●			●			●	●		

description

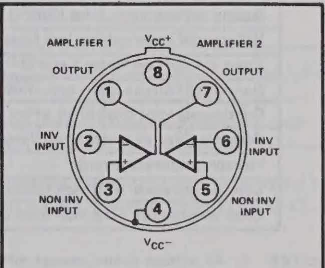
These monolithic JFET-input operational amplifiers incorporate well-matched, high-voltage BI-FET technology (JFET's on the same chip with standard bipolar transistors). The devices feature low input bias and offset currents, low offset voltage, and low offset voltage temperature coefficient. The devices are also designed for wide bandwidths, high slew rate, extremely fast settling time, low equivalent input noise voltage and current, and a low 1/f corner.

The LF2155, LF2155A, LF2156, LF2156A, LF2157, and LF2157A are characterized for operation over the full military temperature range of −55°C to 125°C; the LF2255, LF2256, and LF2257 are characterized for operation from −25°C to 85°C; the LF2355, LF2355A, LF2356, LF2356A, LF2357, and LF2357A are characterized for operation from 0°C to 70°C.

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



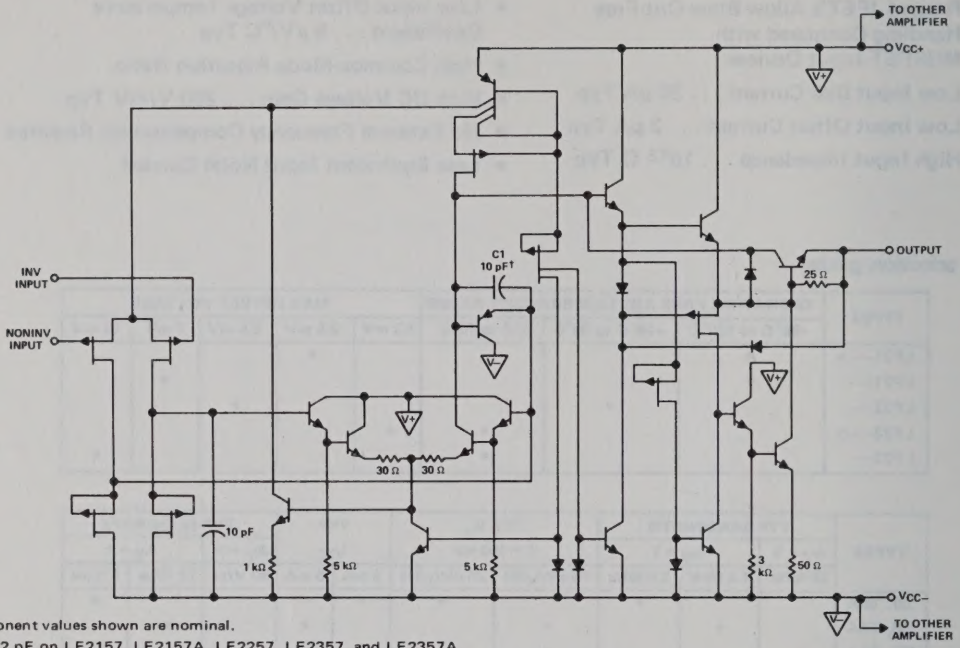
L
PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TYPES LF2155, LF2155A, LF2156, LF2156A, LF2157, LF2157A, LF2255, LF2256, LF2257, LF2355, LF2355A, LF2356, LF2356A, LF2357, LF2357A DUAL JFET-INPUT OPERATIONAL AMPLIFIERS

schematic (each amplifier)



Component values shown are nominal.
†C1 = 2 pF on LF2157, LF2157A, LF2257, LF2357, and LF2357A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LF21-- LF21--A	LF22--	LF23-- LF23--A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±40	±40	±30	V
Input voltage (see Notes 1 and 3)		±20	±20	±15	V
Duration of output short-circuit (one amplifier, see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		670	670	670	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	JG or L package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P package	260	260	260	°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves, Section 2. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

electrical characteristics, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LF21--			LF22--			LF23--			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$			3	5		3	5		3	10	mV
		$R_S = 50\ \Omega$,	T_A = full range			7			6.5			13	
αV_{IO}	Temperature coefficient of input offset voltage	$R_S = 50\ \Omega$,	T_A = full range		5			5			5		μV/°C
$\frac{\Delta\alpha V_{IO}}{\Delta V_{IO}}$	Change in temperature coefficient with offset voltage adjustment	$R_S = 50\ \Omega$			0.5			0.5			0.5		$\frac{\mu V/°C}{mV}$
I_{IO}	Input offset current				3	20		3	20		3	50	pA
		T_A = full range				20			1			2	nA
I_{IB}	Input bias current				30	100		30	100		30	200	pA
		T_A = full range				50			5			8	nA
V_{ICR}	Common-mode input voltage range			+11 to −11	+15 to −12		+11 to −11	+15 to −12		+10 to −10	+15 to −12		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm15$ V,	$R_L = 10\ k\Omega$	24	26		24	26		24	26		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm15$ V, $R_L = 2\ k\Omega$, $V_O = \pm10$ V	$T_A = 25°C$	50	200		50	200		25	200		V/mV
			T_A = full range	25			25			15			
B_1	Unity-gain bandwidth		'55		2.5			2.5			2.5		MHz
			'56		4.5			4.5			4.5		
			'57		20			20			20		
r_i	Input resistance				10^{12}			10^{12}			10^{12}		Ω
C_i	Input capacitance				3			3			3		pF
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$		85	100		85	100		80	100		dB
k_{SVR}*	Supply voltage rejection ratio			85	100		85	100		80	100		dB
V_n	Equivalent input noise voltage	$R_S = 100\ \Omega$, $f = 100$ Hz	'55		25			25			25		nV/$\sqrt{Hz}$
			'56, '57		15			15			15		
		$R_S = 100\ \Omega$, $f = 1$ kHz	'55		20			20			20		
			'56, '57		12			12			12		
I_n	Equivalent input noise current	$f = 100$ Hz			0.01			0.01			0.01		pA/$\sqrt{Hz}$
		$f = 1$ kHz			0.01			0.01			0.01		
I_{CC}	Supply current	No load, No signal	'55		4	8		4	8		4	8	mA
			'56, '57		10	14		10	14		10	20	

*$k_{SVR} = \Delta V_{CC\pm}/\Delta V_{IO}$.

†All characteristics are specified under open-loop operation, unless otherwise noted. Also unless otherwise noted, $V_{CC\pm} = \pm15$ V to ±20 V for LF21__ and LF22__, $V_{CC\pm} = \pm15$ V for LF23__. Full range for T_A is −55°C to 125°C for LF21__, −25°C to 85°C for LF22__, and 0°C to 70°C for LF23__.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			LF21--			LF22--			LF23--			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{tot}	Total response time (settling time)	$\Delta V_O = 10$ V, $\epsilon = \pm0.01\%$, See Figure 1	$A_V = -1$	'55		4			4			4		μs
				'56		1.5			1.5			1.5		
			$A_V = -5$	'57		1.5			1.5			1.5		
SR	Slew rate	$\Delta V_O = 10$ V, See Figure 2	$A_V = -1$	'55		5			5			5		V/μs
				'56	7.5	12		7.5	12			12		
			$A_V = -5$	'57	30	50		30	50			50		

TYPES LF2155, LF2155A, LF2156, LF2156A, LF2157, LF2157A, LF2255, LF2256, LF2257, LF2355, LF2355A, LF2356, LF2356A, LF2357, LF2357A DUAL JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LF1__A			LF3__A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω			1	2		1	2	mV
		R_S = 50 Ω,	T_A = full range			2.5			2.3	
αV_{IO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = full range		3	5		3	5	µV/°C
$\frac{\Delta\alpha V_{IO}}{\Delta V_{IO}}$	Change in temperature coefficient with offset voltage adjustment	R_S = 50 Ω			0.5			0.5		$\frac{\mu V/°C}{mV}$
I_{IO}	Input offset current				3	10		3	10	pA
		T_A = full range				10			1	nA
I_{IB}	Input bias current				30	50		30	50	pA
		T_A = full range				25			5	nA
V_{ICR}	Common-mode input voltage range			+11 to −11	+15 to −12		+11 to −11	+15 to −12		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V,	R_L = 10 kΩ	24	26		24	26		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ, V_O = ±10 V	T_A = 25°C	50	200		50	200		V/mV
			T_A = full range	25			25			
B_1	Unity-gain bandwidth		'55A		2.5			2.5		MHz
			'56A	4	4.5		4	4.5		
			'57A	15	20		15	20		
r_i	Input resistance				10^{12}			10^{12}		Ω
C_i	Input capacitance				3			3		pF
CMRR	Common-mode rejection ratio	R_S = 50 Ω		85	100		85	100		dB
k_{SVR}*	Supply voltage rejection ratio			85	100		85	100		dB
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 100 Hz	'55A		25			25		nV/√Hz
			'56A, '57A		15			15		
		R_S = 100 Ω, f = 1 kHz	'55A		20			20		
			'56A, '57A		12			12		
I_n	Equivalent input noise current	f = 100 Hz			0.01			0.01		pA/√Hz
		f = 1 kHz			0.01			0.01		
I_{CC}	Supply current	No load, No signal	'55A		4	8		4	8	mA
			'56A, '57A		10	14		10	14	

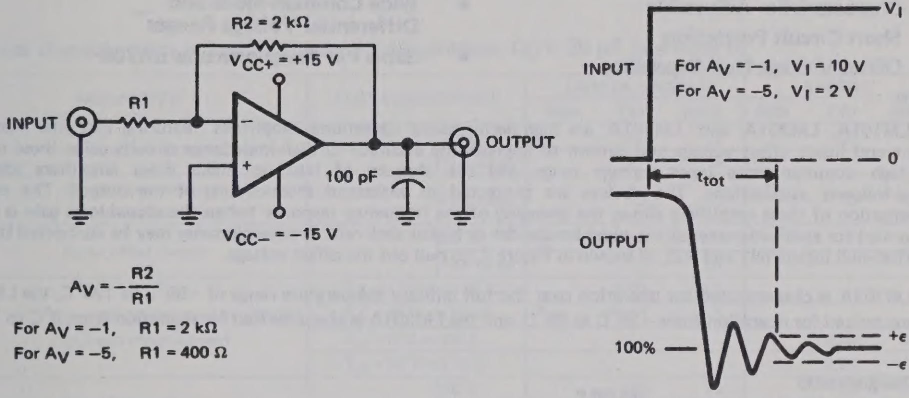
*$k_{SVR} = \Delta V_{CC\pm}/\Delta V_{IO}$.

†All characteristics are specified under open-loop operation, unless otherwise noted. Also unless otherwise noted, $V_{CC\pm}$ = ±15 V to 20 V for LF21––A and LF23––A. Full range for T_A is −55°C to 125°C for LF21––A and 0° to 70°C for LF23––A.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			LF21––A			LF23––A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{tot}	Total response time (settling time)	ΔV_O = 10 V, ε = ±0.01%, See Figure 1	A_V = −1	'55A		4			4		µs
				'56A		1.5			1.5		
			A_V = −5	'57A		1.5			1.5		
SR	Slew rate	ΔV_O = 10 V, See Figure 2	A_V = −1	'55A	3	5		3	5		V/µs
				'56A	10	12		10	12		
			A_V = −5	'57A	40	50		40	50		

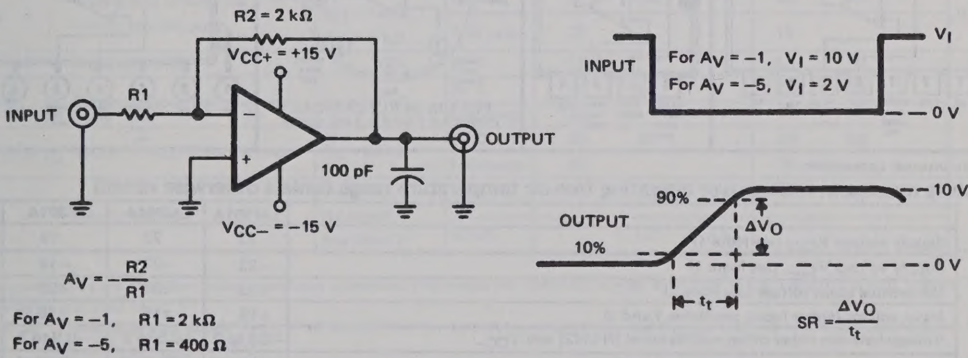
PARAMETER MEASUREMENT INFORMATION


R2 = 2 kΩ
VCC+ = +15 V
R1
INPUT
OUTPUT
100 pF
VCC– = –15 V
$A_V = -\frac{R2}{R1}$
For $A_V = -1$, R1 = 2 kΩ
For $A_V = -5$, R1 = 400 Ω
V_I
INPUT
For $A_V = -1$, $V_I = 10$ V
For $A_V = -5$, $V_I = 2$ V
0
t_{tot}
OUTPUT
100%
$+\epsilon$
$-\epsilon$

TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 1–TOTAL RESPONSE TIME


R2 = 2 kΩ
VCC+ = +15 V
R1
INPUT
OUTPUT
100 pF
VCC– = –15 V
$A_V = -\frac{R2}{R1}$
For $A_V = -1$, R1 = 2 kΩ
For $A_V = -5$, R1 = 400 Ω
V_I
INPUT
For $A_V = -1$, $V_I = 10$ V
For $A_V = -5$, $V_I = 2$ V
0 V
90%
10 V
OUTPUT
ΔV_O
10%
0 V
t_t
$SR = \frac{\Delta V_O}{t_t}$

TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 2–SLEW RATE

TI cannot assume any responsibility for any circuits shown
or represent that they are free from patent infringement.

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IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

TYPES LM101A, LM201A, LM301A HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611432, JANUARY 1971–REVISED JUNE 1976

FORMERLY SN52101A, SN72301A

- Low Input Currents
- Low Input Offset Parameters
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Designed to be Interchangeable with National Semiconductor LM101A and LM301A
- No Latch-Up
- Wide Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as uA709

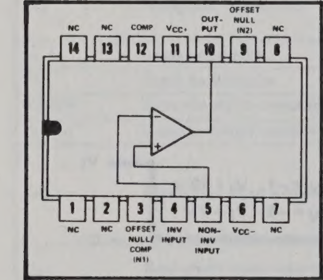
description

The LM101A, LM201A, and LM301A are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices. The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are protected to withstand short-circuits at the output. The external compensation of these amplifiers allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 7, to null out the offset voltage.

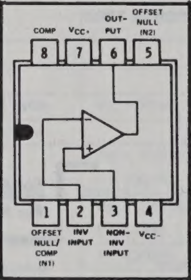
The LM101A is characterized for operation over the full military temperature range of −55°C to 125°C, the LM201A is characterized for operation from −25°C to 85°C, and the LM301A is characterized for operation from 0°C to 70°C.

terminal assignments

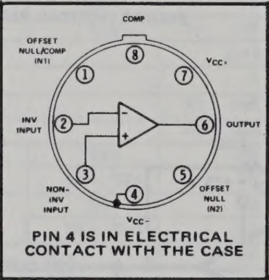
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
NC
COMP
VCC+
OUT-PUT
OFFSET NULL (N2)
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL/COMP (N1)
INV INPUT
NON-INV INPUT
VCC−
NC

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

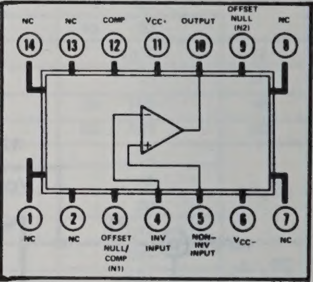

COMP
VCC+
OUT-PUT
OFFSET NULL (N2)
8
7
6
5
1
2
3
4
OFFSET NULL/COMP (N1)
INV INPUT
NON-INV INPUT
VCC−

L PLUG-IN PACKAGE (TOP VIEW)


COMP
OFFSET NULL/COMP (N1)
VCC+
INV INPUT
OUTPUT
NON-INV INPUT
OFFSET NULL (N2)
VCC−
1
2
3
4
5
6
7
8

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)


NC
NC
COMP
VCC+
OUTPUT
OFFSET NULL (N2)
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL/COMP (N1)
INV INPUT
NON-INV INPUT
VCC−
NC

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM101A	LM201A	LM301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	500	mW
Operating free-air temperature range		−55 to125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L, or U package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM201A only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature, C_C = 30 pF (see note 6)

PARAMETER		TEST CONDITIONS†		LM101A, LM201A			LM301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2.0	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	μV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for LM101A is −55°C to 125°C, for LM201A is −25°C to 85°C, and for LM301A is 0°C to 70°C.

NOTES: 6. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for LM101A and LM201A, and $V_{CC\pm}$ = ±5 V to ±15 V for LM301A. All typical values are at $V_{CC\pm}$ = ±15 V.

7. For LM101A and LM201A, $V_{CC\pm}$ = ±20 V. For LM301A, $V_{CC\pm}$ = ±15 V.

TYPES LM101A, LM201A, LM301A
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

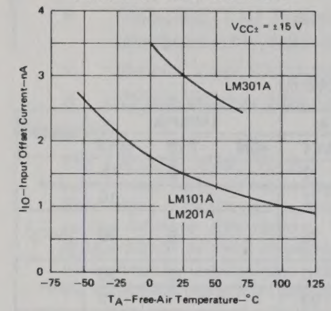


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

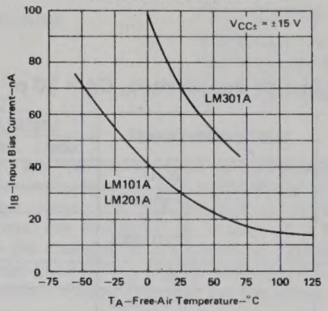


FIGURE 2

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

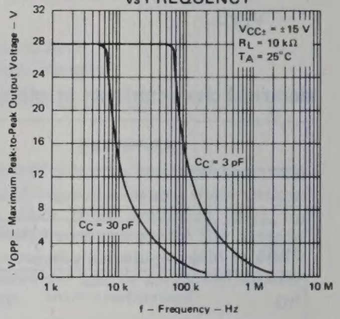


FIGURE 3

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

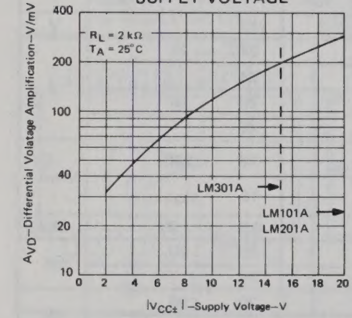


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

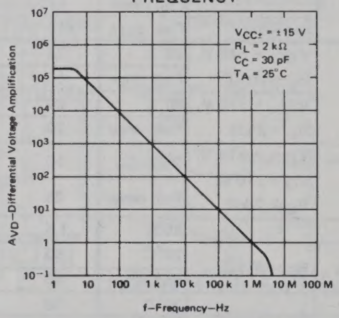


FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

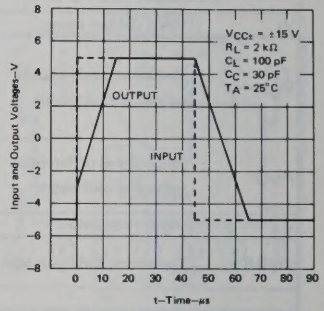
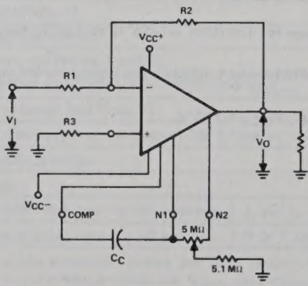


FIGURE 6

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geqslant \frac{R1 \cdot 30\ \text{pF}}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 7—INVERTING CIRCUIT WITH ADJUSTABLE GAIN,
SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

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LINEAR INTEGRATED CIRCUITS

TYPES LM107, LM207, LM307 HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611426, DECEMBER 1970—REVISED JUNE 1976

FORMERLY SN52107, SN72307

- Low Input Currents
- No Frequency Compensation Required
- Low Input Offset Parameters
- Short-Circuit Protection
- No Latch-Up
- Wide Common-Mode and Differential Voltage Ranges

description

The LM107, LM207, and LM307 are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The LM107 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM207 is characterized for operation from −25°C to 85°C, and the LM307 is characterized for operation from 0°C to 70°C.

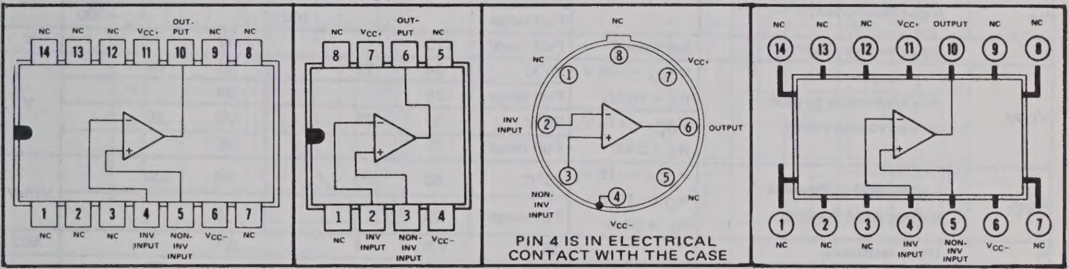
terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

JG OR P DUAL-IN-LINE PAKCAGE (TOP VIEW)

L PLUG-IN PACKAGE (TOP VIEW)

U FLAT PACKAGE (TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM107	LM207	LM307	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	500	mW
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L or U package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM207 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES LM107, LM207, LM307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

electrical characteristics at specified free-air temperature (see note 6)

	PARAMETER	TEST CONDITIONS†		LM107, LM207 MIN	LM107, LM207 TYP	LM107, LM207 MAX	LM307 MIN	LM307 TYP	LM307 MAX	UNIT
V_{IO}	Input offset voltage	R_S = 50 kΩ	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		3	15		6	30	µV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_I	Input voltage range	See Note 7	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	R_S = 50 kΩ	25°C	80	98		70	90		dB
			Full range	80			70			
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	R_S = 50 kΩ	25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, No signal, See Note 7	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

†All characteristics are specified under open-loop operation. Full range for LM107 is −55°C to 125°C, for LM207 is −25°C to 85°C, and for LM307 is 0°C to 70°C.

NOTES: 6. Unless otherwise noted $V_{CC\pm}$ = ±5 V to ±20 V for LM107 and LM207, and $V_{CC\pm}$ = ±5 V to ±15 V for LM307. All typical values are at $V_{CC\pm}$ = ±15 V.

7. For LM107 and LM207, $V_{CC\pm}$ = ±20 V. For LM307, $V_{CC\pm}$ = ±15 V.

TYPES LM107, LM207, LM307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

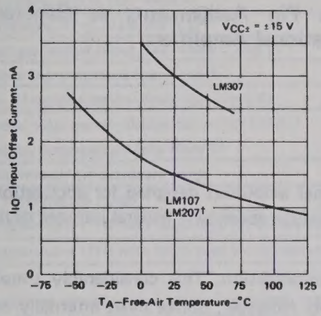


FIGURE 1

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

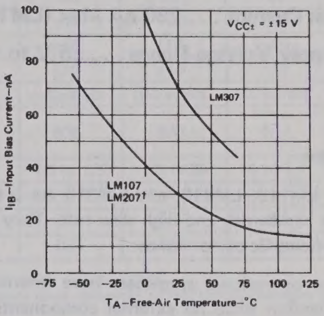


FIGURE 2

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

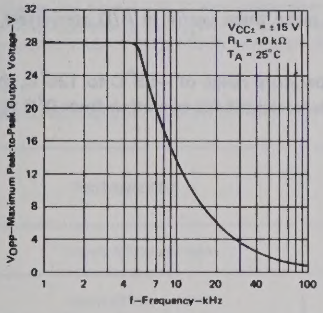


FIGURE 3

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

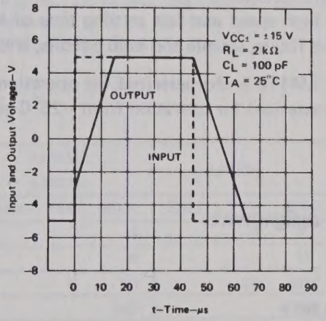


FIGURE 4

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

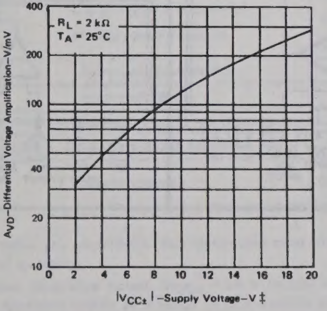


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

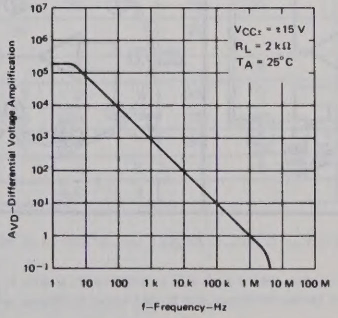


FIGURE 6

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† Data for free-air temperatures below –25°C and above 85°C is applicable for LM107 only.

‡ Data for supply voltages greater than 15 V is applicable to LM107 and LM207 circuits only.

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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

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TYPES LM118, LM218, LM318
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612410, JUNE 1976

- Small-Signal Bandwidth . . . 15 MHz Typ
- Slew Rate . . . 50 V/μs Min
- Bias Current . . . 250 nA Max (LM118, LM218)
- Supply Voltage Range . . . ±5 V to ±20 V
- Internal Frequency Compensation
- Input and Output Overload Protection
- Same Pin Assignments as General Purpose Operational Amplifiers

description

The LM118, LM218, and LM318 are precision high-speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing dc performance.

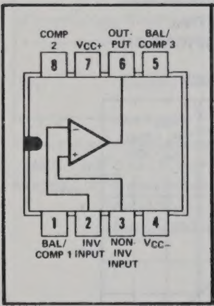
These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 150 V/μs and almost double the bandwidth. Overcompensation may be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor may be added to reduce the settling time for $\epsilon < 0.1\%$ to under 1 μs.

The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample and hold circuits, and general purpose amplifiers.

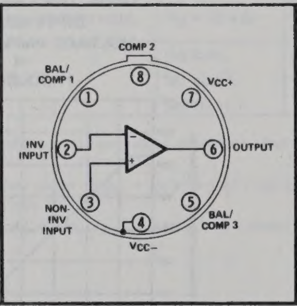
The LM118 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM218 is characterized for operation from −25°C to 85°C, and the LM318 is characterized for operation from 0°C to 70°C.

terminal assignments

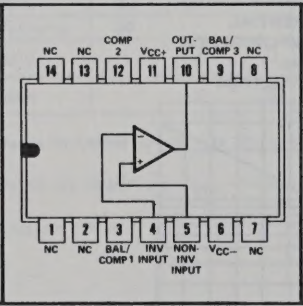
JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)


COMP 2
V_{CC+}
OUT-PUT
BAL/ COMP 3
8
7
6
5
1
2
3
4
BAL/ COMP 1
INV INPUT
NON-INV INPUT
V_{CC-}

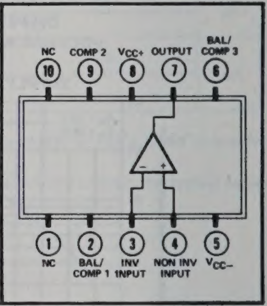
L PLUG-IN PACKAGE
(TOP VIEW)


COMP 2
8
BAL/ COMP 1
1
V_{CC+}
7
INV INPUT
2
6
OUTPUT
NON-INV INPUT
3
5
BAL/ COMP 3
4
V_{CC-}

N DUAL-IN-LINE
PACKAGE (TOP VIEW)


NC
NC
COMP 2
V_{CC+}
OUT-PUT
BAL/ COMP 3
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
BAL/ COMP 1
INV INPUT
NON-INV INPUT
V_{CC-}
NC

U FLAT PACKAGE
(TOP VIEW)


NC
COMP 2
V_{CC+}
OUTPUT
BAL/ COMP 3
10
9
8
7
6
1
2
3
4
5
NC
BAL/ COMP 1
INV INPUT
NON INV INPUT
V_{CC-}

TYPES LM118, LM218, LM318
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM118	LM218	LM318	UNIT
Supply voltage, V_{CC+} (see Note 1)	20	20	20	V
Supply voltage, V_{CC-} (see Note 1)	−20	−20	−20	V
Input voltage (either input, see Notes 1 and 2)	±15	±15	±15	V
Differential input current (see Note 3)	±10	±10	±10	mA
Duration of output short-circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)	500	500	500	mW
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J, JG, L, or U package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. For the LM118 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM218 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature (see note 6)

PARAMETER		TEST CONDITIONS†		LM118 LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current		25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current		25°C		120	250		150	500	nA
			Full range			500			750	
V_I	Input voltage range	$V_{CC\pm} = \pm 15$ V	Full range	±11.5			±11.5			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L = 2$ kΩ	Full range	24	26		24	26		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $V_O = \pm 10$ V, $R_L \geqslant 2$ kΩ	25°C	50	20		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm} = \pm 15$ V	25°C		15			15		MHz
r_i	Input resistance		25°C	1	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio		Full range	80	100		70	100		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio		Full range	70	80		65	80		dB
I_{CC}	Supply current	No load	25°C		5	8		5	10	mA
			MAX		4.5	7				

†All characteristics are specified under open-loop operation. Full range for LM118 is −55°C to 125°C, for LM218 is −25°C to 85°C and for LM318 is 0°C to 70°C.

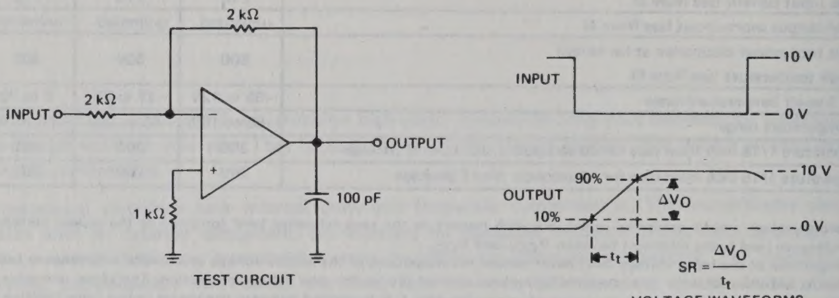
NOTE 6: Unless otherwise noted, $V_{CC\pm} = \pm 5$ V to ±20 V. All typical values are at $V_{CC\pm} = \pm 15$ V. Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

TYPES LM118, LM218, LM318
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$\Delta V_I = 10$ V,	$C_L = 100$ pF,	See Figure 1	50	70		V/µs

parameter measurement information

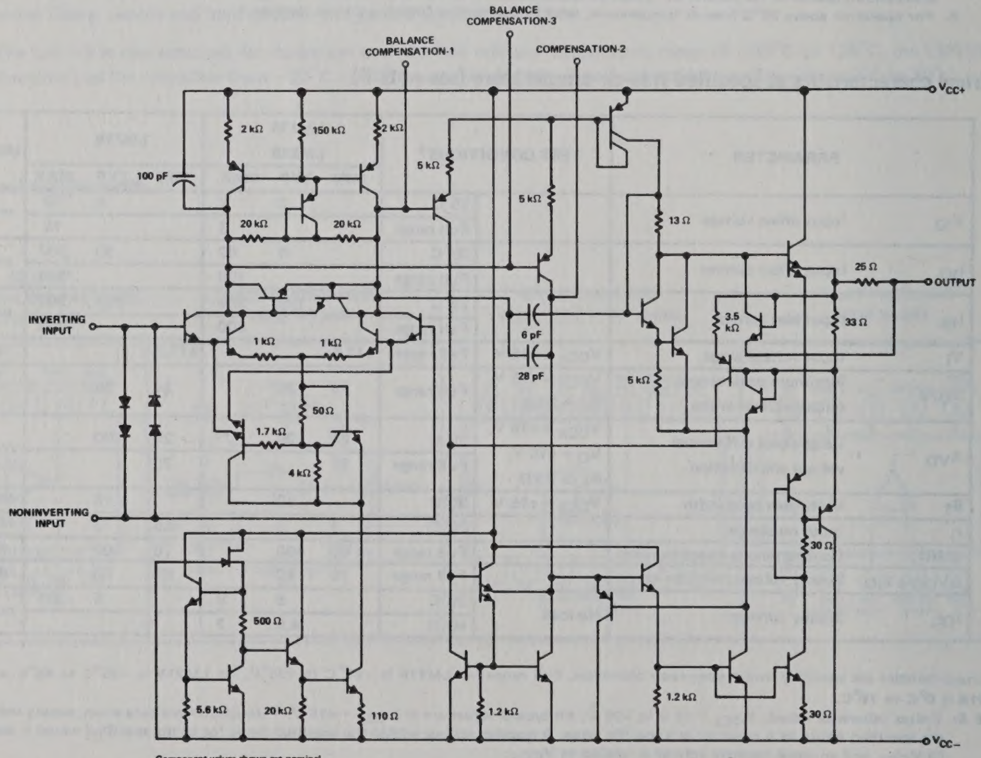

2 kΩ
2 kΩ
INPUT
–
+
OUTPUT
100 pF
1 kΩ
INPUT
10 V
0 V
OUTPUT
90%
10%
10 V
0 V
ΔV_O
t_t
$SR = \frac{\Delta V_O}{t_t}$

TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 1—SLEW RATE

schematic


BALANCE COMPENSATION-3
BALANCE COMPENSATION-1
COMPENSATION-2
V_{CC+}
2 kΩ
150 kΩ
2 kΩ
100 pF
5 kΩ
5 kΩ
20 kΩ
20 kΩ
13 Ω
25 Ω
OUTPUT
INVERTING INPUT
3.5 kΩ
33 Ω
1 kΩ
1 kΩ
6 pF
28 pF
5 kΩ
50 Ω
1.7 kΩ
4 kΩ
NONINVERTING INPUT
30 Ω
500 Ω
5.6 kΩ
20 kΩ
110 Ω
1.2 kΩ
1.2 kΩ
30 Ω
V_{CC-}

Component values shown are nominal.

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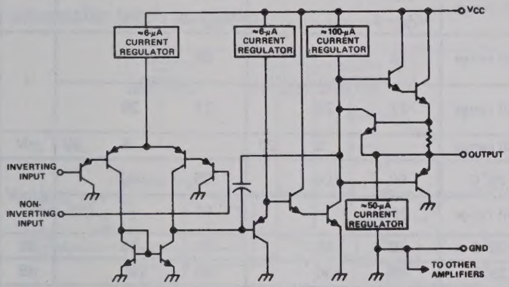
IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

TYPES LM124, LM224, LM324
QUADRUPLE OPERATIONAL AMPLIFIERS

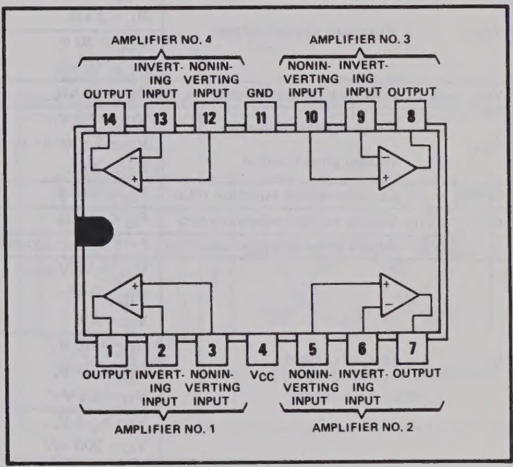
BULLETIN NO. DL-S 7612248, SEPTEMBER 1975—REVISED JUNE 1976

- Wide Range of Supply Voltages
  Single Supply . . . 3 V to 30 V
  or Dual Supplies
- Low Supply Current Drain
  Independent of Supply Voltage
  . . . 0.8 mA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Low Input Bias and Offset Parameters
  Input Offset Voltage . . . 2 mV Typ
  Input Offset Current . . . 3 nA Typ (LM124)
  Input Bias Current . . . 45 nA Typ
- Differential Input Voltage Range
  Equal to Maximum-Rated
  Supply Voltage . . . ±32 V
- Open-Loop Differential Voltage
  Amplification . . . 100 V/mV Typ
- Internal Frequency Compensation

schematic (each amplifier)


VCC
≈6-μA CURRENT REGULATOR
≈6-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
INVERTING INPUT
NON-INVERTING INPUT
OUTPUT
≈50-μA CURRENT REGULATOR
GND
TO OTHER AMPLIFIERS

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


AMPLIFIER NO. 4
AMPLIFIER NO. 3
OUTPUT
INVERT-ING INPUT
NONIN-VERTING INPUT
GND
NONIN-VERTING INPUT
INVERT-ING INPUT
OUTPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT
INVERT-ING INPUT
NONIN-VERTING INPUT
VCC
NONIN-VERTING INPUT
INVERT-ING INPUT
OUTPUT
AMPLIFIER NO. 1
AMPLIFIER NO. 2

description

These devices consist of four independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 30 volts and Pin 4 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ± 15-volt supplies.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		32 V
Differential input voltage (see Note 2)		±32 V
Input voltage range (either input)		−0.3 V to 32 V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leqslant 15$ V) (see Note 3)		unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)		900 mW
Operating free-air temperature range:	LM124	−55°C to 125°C
	LM224	−25°C to 85°C
	LM324	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES LM124, LM224, LM324
QUADRUPLE OPERATIONAL AMPLIFIERS

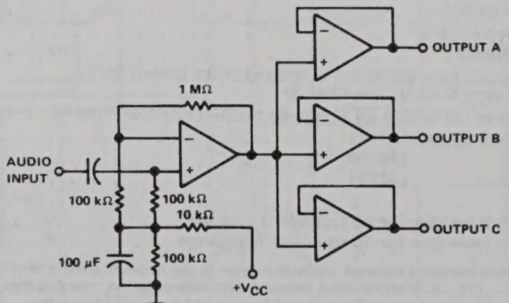
electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM124			LM224, LM324			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{CC} = 5 V to 30 V	25°C		2	5		2	7	mV
			Full range			7			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	30		5	50	nA
			Full range			100			150	
I_{IB}	Input bias current	V_O = 1.4 V, See Note 5	25°C		−45	−150		−45	−250	nA
			Full range			−300			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			V
		V_{CC} = 30 V, $R_L \geq$ 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_L \leq$ 10 kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \geq$ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ	25°C	70	85		65	85		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	$R_S \leq$ 10 kΩ	25°C	65	100		65	100		dB
	Amplifier-to-amplifier coupling	f = 1 kHz to 20 kHz	25°C		−120			−120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0 V	25°C	−20	−40		−20	−40		mA
			Full range	−10	−20		−10	−20		
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 2.5 V	25°C	10	20		10	20		
			Full range	5	8		5	8		
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	50		12	50		μA
I_{CC}	Supply current (four amplifiers)	No load, No signal	25°C		0.8			0.8		mA
			Full range			2			2	

†All characteristics are specified under open-loop conditions. Full range is −55°C to 125°C for LM124, −25°C to 85°C for LM224, and 0°C to 70°C for LM324.

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

TYPICAL APPLICATION DATA



AUDIO DISTRIBUTION AMPLIFIER

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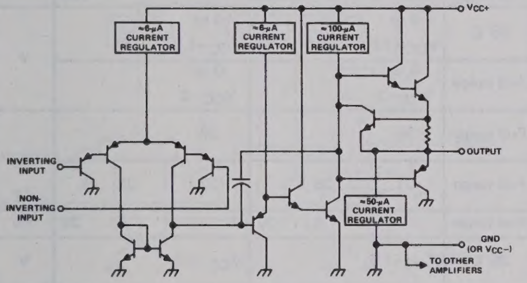
TYPES LM158, LM258, LM358
DUAL OPERATIONAL AMPLIFIERS

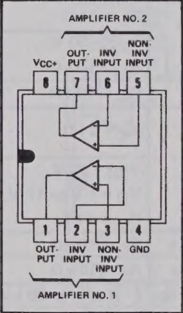
BULLETIN NO. DL-S 7612413, JUNE 1976

- Wide Range of Supply Voltages
  Single Supply . . . 3 V to 30 V
  or Dual Supplies
- Low Supply Current Drain
  Independent of Supply Voltage
  . . . 0.5 mA Typ
- Common-Mode Input Voltage
  Range Includes Ground Allowing
  Direct Sensing near Ground
- Low Input Bias and Offset Parameters
  Input Offset Voltage . . . 2 mV Typ
  Input Offset Current . . . 3 nA Typ (LM158)
  Input Bias Current . . . 45 nA Typ
- Differential Input Voltage Range
  Equal to Maximum-Rated
  Supply Voltage . . . ±32 V
- Open-Loop Differential Voltage
  Amplification . . . 100 V/mV Typ
- Internal Frequency Compensation

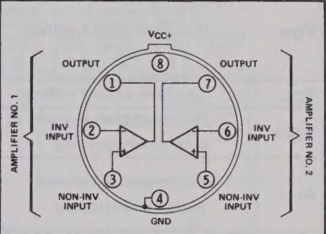
schematic (each amplifier)


≈6-μA CURRENT REGULATOR
≈6-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
VCC+
OUTPUT
INVERTING INPUT
NON-INVERTING INPUT
≈50-μA CURRENT REGULATOR
GND (OR VCC−)
TO OTHER AMPLIFIERS

JG OR P
DUAL-IN-LINE
PACKAGE (TOP VIEW)


AMPLIFIER NO. 2
VCC+
OUT-PUT
INV INPUT
NON-INV INPUT
8
7
6
5
1
2
3
4
OUT-PUT
INV INPUT
NON-INV INPUT
GND
AMPLIFIER NO. 1

L
PLUG-IN
PACKAGE (TOP VIEW)


VCC+
8
OUTPUT
1
OUTPUT
7
AMPLIFIER NO. 1
INV INPUT
2
6
INV INPUT
AMPLIFIER NO. 2
3
5
NON-INV INPUT
4
NON-INV INPUT
GND

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 30 volts and Pin 4 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM158 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-volt supplies.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		32 V
Differential input voltage (see Note 2)		±32 V
Input voltage range (either input)		−0.3 V to 32 V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)		unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4): JG or P package		900 mW
L package		625 mW
Operating free-air temperature range:	LM158	−55°C to 125°C
	LM258	−25°C to 85°C
	LM358	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds:	JG or P package	300°C
Lead temperature 1/16 inch from case for 10 seconds:	N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES LM158, LM258, LM358
DUAL OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM158			LM258, LM358			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{CC} = 5 V to 30 V	25°C		2	5		2	7	mV
			Full range			7			9	
αV_{IO}	Average temperature coefficient of input offset voltage		Full range		7			7		μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	30		5	50	nA
			Full range			100			150	
αI_{IO}	Average temperature coefficient of input offset current		Full range		10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V, See Note 5	25°C		−45	−150		−45	−250	nA
			Full range			−300			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
			Full range	0 to V_{CC}−2			0 to V_{CC}−2			
V_{OH}	High-level output voltage	V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			V
		V_{CC} = 30 V, $R_L \geqslant$ 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_L \leqslant$ 10 kΩ	Full range		5	20		5	20	mV
V_{OPP}	Maximum peak-to peak output voltage swing	R_L = 2 kΩ	25°C	V_{CC}−1.5			V_{CC}−1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \geqslant$ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	$R_S \leqslant$ 10 kΩ	25°C	70	85		70	85		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	$R_S \leqslant$ 10 kΩ	25°C	65	100		65	100		dB
	Amplifier-to-amplifier coupling	f = 1 kHz to 20 kHz	25°C		−120			−120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0 V	25°C	−20	−40		−20	−40		mA
			Full range	−10	−20		−10	−20		
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 200 mV	25°C	10	20		10	20		
			Full range	5	8		5	8		
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	50		12	50		μA
I_{CC}	Supply current (two amplifiers)	No load, No signal	25°C		0.5			0.5		mA
			Full range			1.2			1.2	

† All characteristics are specified under open-loop conditions. Full range is −55°C to 125°C for LM158, −25°C to 85°C for LM258, and 0°C to 70°C for LM358.

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

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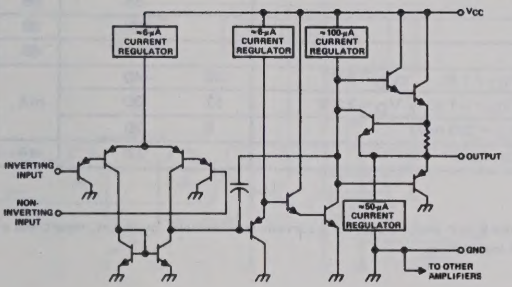
LINEAR INTEGRATED CIRCUITS

TYPE LM2902
QUADRUPLE OPERATIONAL AMPLIFIER

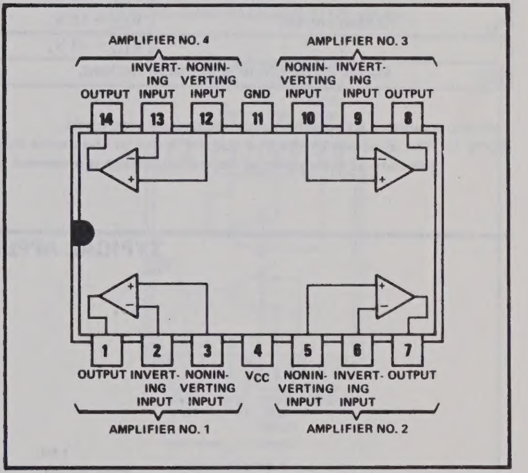
BULLETIN NO. DL-S 7612291, MARCH 1976—REVISED JUNE 1976

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 26 V or Dual Supplies**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters**
  - **Input Offset Voltage . . . 2 mV Typ**
  - **Input Offset Current . . . 5 nA Typ**
  - **Input Bias Current . . . 45 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±26 V**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Maximum Peak-to-Peak Output Voltage Swing . . . V_{CC}−1.5 V Typ**
- **Internal Frequency Compensation**

schematic (each amplifier)


VCC
≈6-μA CURRENT REGULATOR
≈6-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
OUTPUT
INVERTING INPUT
NON-INVERTING INPUT
≈50-μA CURRENT REGULATOR
GND
TO OTHER AMPLIFIERS

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


AMPLIFIER NO. 4
AMPLIFIER NO. 3
OUTPUT
INVERTING INPUT
NONINVERTING INPUT
GND
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT
INVERTING INPUT
NONINVERTING INPUT
VCC
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
AMPLIFIER NO. 1
AMPLIFIER NO. 2

description

This device consists of four independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply as in automotive systems. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 26 volts and Pin 4 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM2902 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ± 15-volt supplies.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	26 V
Differential input voltage (see Note 2)	±26 V
Input voltage range (either input)	−0.3 V to 26 V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leqslant 15$ V) (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	900 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPE LM2902
QUADRUPLE OPERATIONAL AMPLIFIER

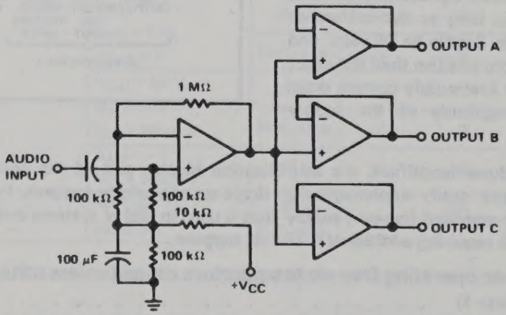
electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V		2	10	mV
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V, See Note 5		−45	−500	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 24 V	0 to V_{CC}−1.5			V
V_{OH}	High-level output voltage	V_{CC} = 24 V, R_L = 2 kΩ	20			V
		V_{CC} = 24 V, $R_L \geq$ 10 kΩ	21			
V_{OL}	Low-level output voltage	$R_L \leq$ 10 kΩ		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq$ 2 kΩ, V_O = 1 V to 11 V		100		V/mV
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ		85		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	$R_S \leq$ 10 kΩ		100		dB
	Amplifier-to-amplfiier coupling	f = 1 kHz to 20 kHz		−120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0 V	−20	−40		mA
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 2.5 V	12	30		
		V_{ID} = −1 V, V_O = 200 mV	8	20		
I_{CC}	Supply current (four amplifiers)	No load, No signal		0.8	2	mA

† All characteristics are specified under open-loop conditions.

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

TYPICAL APPLICATION DATA



AUDIO DISTRIBUTION AMPLIFIER

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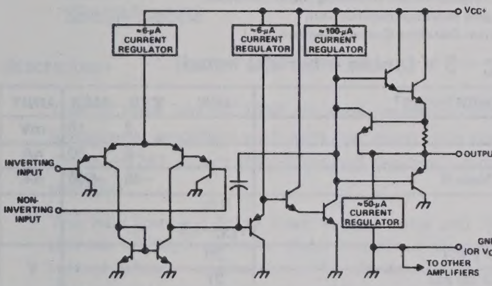
LINEAR INTEGRATED CIRCUITS

TYPE LM2904 DUAL OPERATIONAL AMPLIFIER

BULLETIN NO. DL-S 7612402, JUNE 1976

- Wide Range of Supply Voltages
  Single Supply . . . 3 V to 26 V
  or Dual Supplies
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Low Input Bias and Offset Parameters
  Input Offset Voltage . . . 2 mV Typ
  Input Offset Current . . . 5 nA Typ
  Input Bias Current . . . 45 nA Typ
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±26 V
- Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ
- Maximum Peak-to-Peak Output Voltage Swing . . . $V_{CC}-1.5$ V Typ
- Internal Frequency Compensation

schematic (each amplifier)

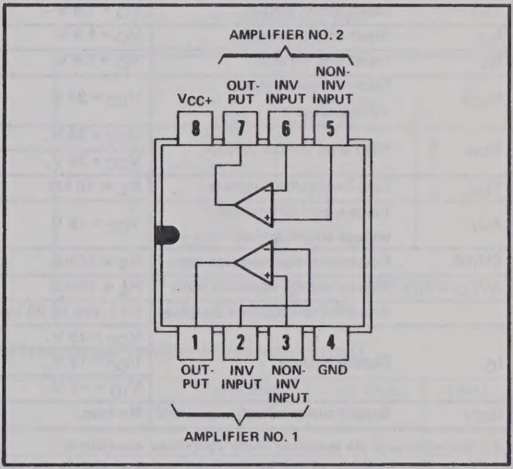

≈6-μA CURRENT REGULATOR
≈6-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
VCC+
OUTPUT
INVERTING INPUT
NON-INVERTING INPUT
≈50-μA CURRENT REGULATOR
GND (OR VCC−)
TO OTHER AMPLIFIERS

description

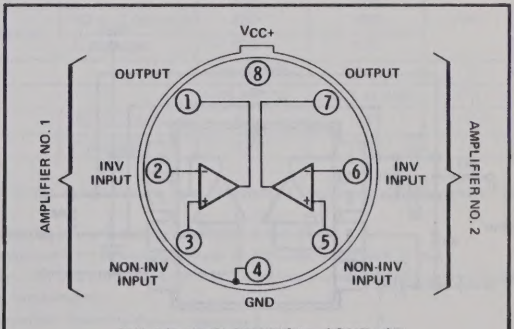
This device consists of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply as in automotive systems. Operation from split supplies is also possible so long as the difference between the two supplies is 3 volts to 26 volts and Pin 8 is at least 1.5 volts more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM2904 can be operated directly off of the standard five-volt supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-volt supplies.

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)


AMPLIFIER NO. 2
VCC+
OUT-PUT
INV INPUT
NON-INV INPUT
8
7
6
5
1
2
3
4
OUT-PUT
INV INPUT
NON-INV INPUT
GND
AMPLIFIER NO. 1

L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
OUTPUT
OUTPUT
8
1
7
AMPLIFIER NO. 1
AMPLIFIER NO. 2
INV INPUT
INV INPUT
2
6
3
5
4
NON-INV INPUT
NON-INV INPUT
GND

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

TYPE LM2904
OPERATIONAL AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	26 V
Differential input voltage (see Note 2)	±26 V
Input voltage range (either input)	−0.3 V to 26 V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \leq 15$ V) (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4): JG or P package	680 mW
L package	625 mW
Operating free-air temperature range	−40°C to 85°C
Lead temperature 1/16 inch from case for 60 seconds: JG or L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

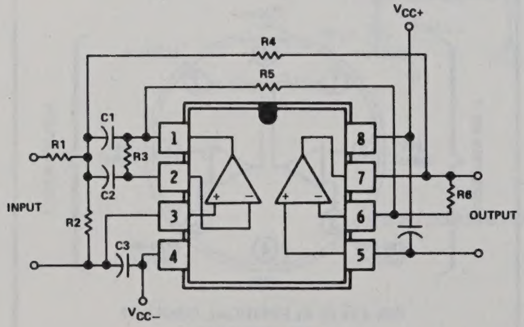
electrical characteristics at 25°C free-air temperature, $V_{CC} = 5$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 1.4$ V				2	10	mV
I_{IO}	Input offset current	$V_O = 1.4$ V				5	50	nA
I_{IB}	Input bias current	$V_O = 1.4$ V	See Note 5			−45	−500	nA
V_{ICR}	Common-mode input voltage range	$V_{CC} = 24$ V			0 to $V_{CC}-1.5$			V
V_{OH}	High-level output voltage	$V_{CC} = 24$ V,	$R_L = 2$ kΩ		20			V
		$V_{CC} = 24$ V,	$R_L \geq 10$ kΩ		21			
V_{OL}	Low-level output voltage	$R_L \leq 10$ kΩ				5	20	mV
A_{VD}	Large-signal differential voltage amplification	$V_{CC} = 15$ V,	$R_L \geq 2$ kΩ,	$V_O = 1$ V to 11 V		100		V/mV
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ				85		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	$R_S \leq 10$ kΩ				100		dB
	Amplifier-to-amplfiier coupling	f = 1 kHz to 20 kHz				−120		dB
I_O	Output current	$V_{CC} = 15$ V,	$V_{ID} = 1$ V,	$V_O = 0$ V	−20	−40		mA
		$V_{CC} = 15$ V,	$V_{ID} = -1$ V,	$V_O = 2.5$ V	12	30		
		$V_{ID} = -1$ V,	$V_O = 200$ mV		8	20		
I_{CC}	Supply current (both amplifiers)	No load,	No signal			0.5	1.2	mA

† All characteristics are specified under open-loop conditions.

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

TYPICAL APPLICATION DATA



SELECT VALUES FOR:

Q

C1 and C2

where C1 = C2

$\omega_0 = 2\pi f_0$

K

K is selected to optimize sensitivity and is typically between 1 and 10.

CALCULATE:

$$R1 = R3 = R5 = \frac{Q}{\omega_0 C}$$

$$R2 = \frac{R1}{Q - 1 - \frac{2}{K} + \frac{1}{K \cdot Q}}$$

$$R4 = \frac{R1 \cdot K \cdot Q}{2Q - 1}$$

$$R6 = K \cdot R1$$

MULTIPLE-FEEDBACK ACTIVE BANDPASS FILTER

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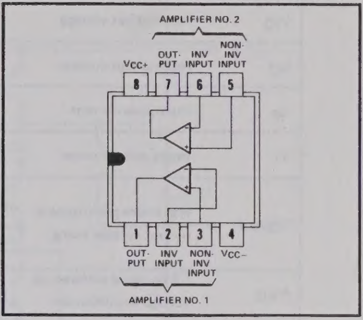
TYPES MC1558, MC1458
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611457, FEBRUARY 1971—REVISED JUNE 1976

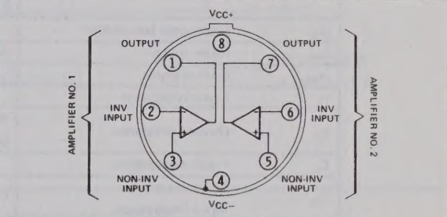
FORMERLY SN52558, SN72558

- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558

JG OR P
DUAL-IN-LINE
PACKAGE
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

description

The MC1558 and MC1458 are dual general-purpose operational amplifiers with each half electrically similar to uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The MC1558 is characterized for operation over the full military temperature range of −55°C to 125°C; the MC1458 is characterized for operation from 0°C to 75°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			MC1558	MC1458	UNIT
Supply voltage V_{CC+} (see Note 1)			22	18	V
Supply voltage V_{CC-} (see Note 1)			−22	−18	V
Differential input voltage (see Note 2)			±30	±30	V
Input voltage (any input, see Notes 1 and 3)			±15	±15	V
Duration of output short-circuit (see Note 4)			unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	Each amplifier		500	500	mW
	Total package	JG or P package	680	680	
		L package	625	625	
Operating free-air temperature range			−55 to 125	0 to 75	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds		JG or L package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds		P package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES MC1558, MC1458
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		MC1558			MC1458			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	25°C	24	28		24	28		V
		$R_L \geq 10$ kΩ	Full range	24			24			
		$R_L = 2$ kΩ	25°C	20	26		20	26		
		$R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	50	200		20	200		V/mV
			Full range	25			15			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	$R_L = 2$ kΩ, $V_O \geq \pm 10$ V, $A_{VD} = 1$, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	$A_{VD} = 1$	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	150	µV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed-loop)	$A_{VD} = 100$, $R_S = 0$, f = 1 kHz, BW = 1 Hz	25°C		45			45		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (Both amplifiers)	No load, No signal	25°C		3.4	5		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (Both amplifiers)	No load, No signal	25°C		100	150		100	170	mW
			Full range			200			200	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

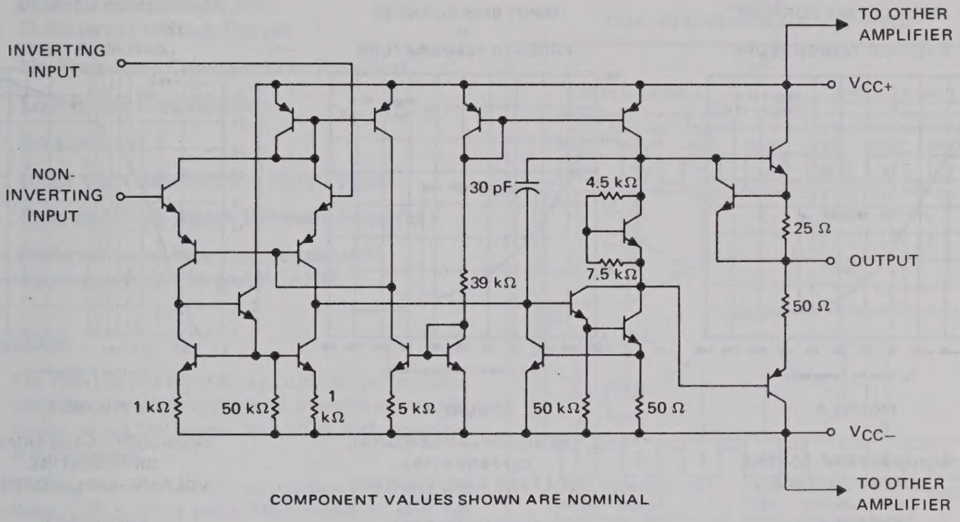
† All characteristics are specified under open-loop operation, unless otherwise noted. Full range for MC1558 is −55°C to 125°C and for MC1458 is 0°C to 75°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

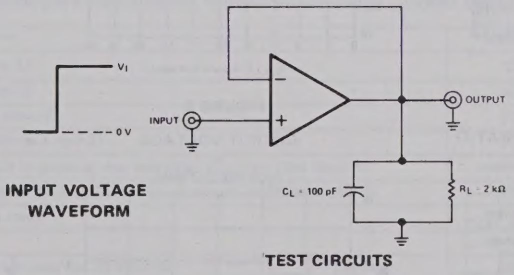
PARAMETER		TEST CONDITIONS	MC1558			MC1458			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/µs

schematic (each amplifier)


TO OTHER AMPLIFIER
INVERTING INPUT
V_{CC+}
NON-INVERTING INPUT
30 pF
4.5 kΩ
25 Ω
OUTPUT
7.5 kΩ
39 kΩ
50 Ω
1 kΩ
50 kΩ
1 kΩ
5 kΩ
50 kΩ
50 Ω
V_{CC-}
TO OTHER AMPLIFIER

COMPONENT VALUES SHOWN ARE NOMINAL

PARAMETER MEASUREMENT INFORMATION


V_I
0 V
INPUT
OUTPUT
−
+
$C_L = 100$ pF
$R_L = 2$ kΩ

INPUT VOLTAGE WAVEFORM

TEST CIRCUITS

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

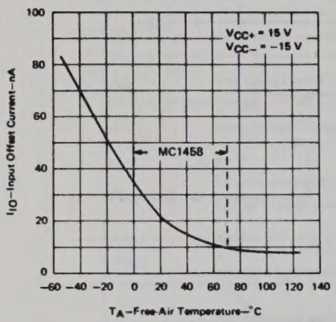


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

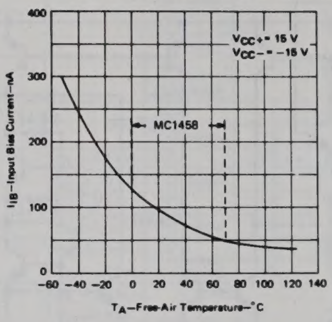


FIGURE 3

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

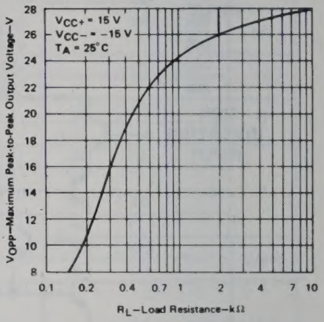


FIGURE 4

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

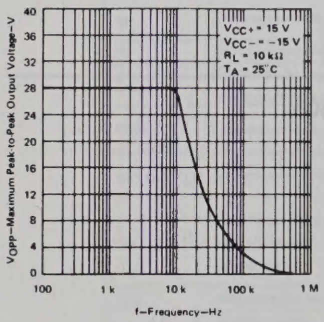


FIGURE 5

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

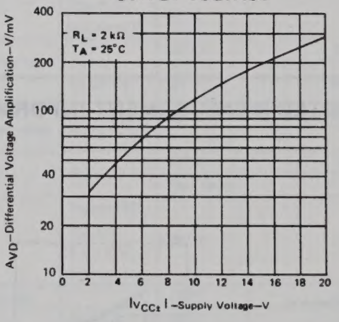


FIGURE 6

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

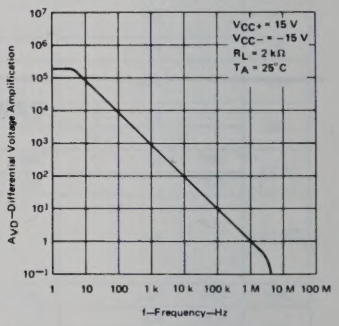


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

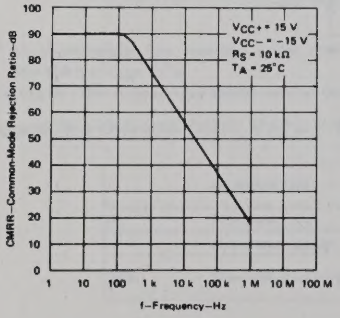


FIGURE 8

OUTPUT VOLTAGE
vs
ELAPSED TIME

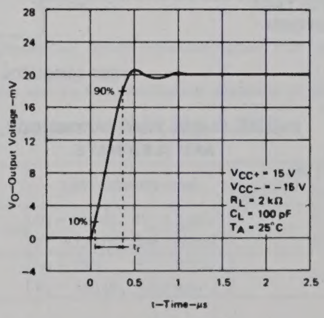


FIGURE 9

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

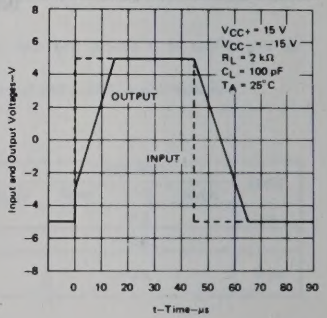


FIGURE 10

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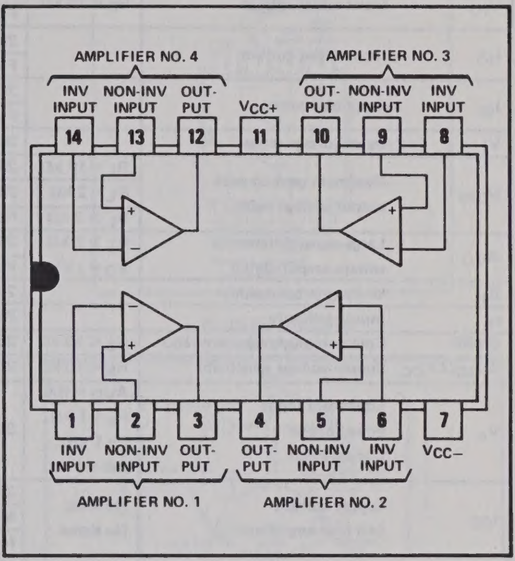
TYPES RM4136, RC4136
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612368, MARCH 1976

- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Unity Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers
- Designed to be Interchangeable with Raytheon RM4136 and RC4136

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The RM4136 and RC4136 are quad high-performance operational amplifiers with each amplifier electrically similar to uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RM4136 is characterized for operation over the full military temperature range of −55°C to 125°C; the RC4136 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RM4136	RC4136	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (See Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		800	800	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES RM4136, RC4136
QUAD HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

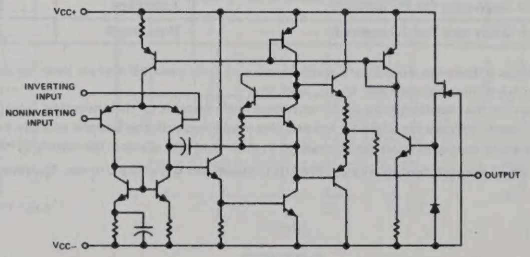
PARAMETER			TEST CONDITIONS†		RM4136			RC4136			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		$R_S \leq 10$ kΩ	25°C		0.5	5		0.5	6	mV
				Full range			6			7.5	
I_{IO}	Input offset current			25°C		5	200		5	200	nA
				Full range			500			300	
I_{IB}	Input bias current			25°C		40	500		40	500	nA
				Full range			1500			800	
V_I	Input voltage range			25°C	±12	±14		±12	±14		V
V_{OPP}	Maximum peak-to-peak output voltage swing		$R_L = 10$ kΩ	25°C	24	28		24	28		V
			$R_L = 2$ kΩ	25°C	20	26		20	26		
			$R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification		$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	50	350		20	300		V/mV
				Full range	25			15			
B_1	Unity-gain bandwidth			25°C	2	3.5			3		MHz
r_i	Input resistance			25°C	0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio		$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity		$R_S \leq 10$ kΩ	25°C		30	150		30	150	µV/V
V_n	Equivalent input noise voltage (closed-loop)		$A_{VD} = 100$, $R_S = 1$ kΩ, $f = 1$ kHz, BW = 1 Hz	25°C		10			10		nV/√Hz
I_{CC}	Supply current (All four amplifiers)		No load, No signal	25°C		5	11.3		5	11.3	mA
				MIN T_A		6	13.3		6	13.7	
				MAX T_A		4.5	10		4.5	10	
P_D	Total power dissipation (All four amplifiers)		No load, No signal	25°C		150	340		150	340	mW
				MIN T_A		180	400		180	400	
				MAX T_A		135	300		135	300	
V_{o1}/V_{o2}	Channel separation	Open loop	$R_S = 1$ kΩ	25°C		105			105		dB
		$A_{VD} = 100$	$f = 10$ kHz	25°C		105			105		

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for RM4136 is −55°C to 125°C and for RC4136 is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	RM4136			RC4136			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF		0.13			0.13		µs
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF		1.5			1.0		V/µs

schematic (each amplifier)



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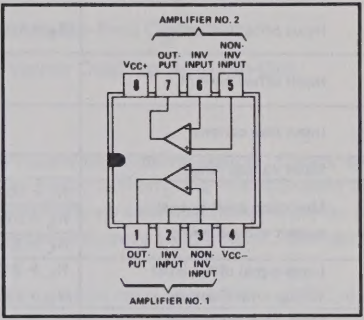
LINEAR INTEGRATED CIRCUITS

TYPES RM4558, RC4558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

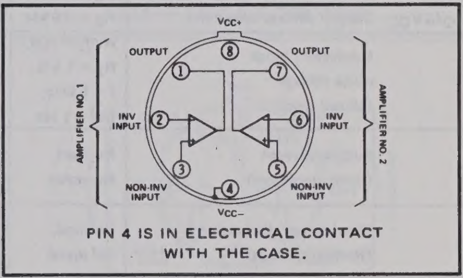
BULLETIN NO. DL-S 7612365, MARCH 1976

- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up
- Unity Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers
- Designed to be Interchangeable with Raytheon RM4558 and RC4558

JG OR P
DUAL-IN-LINE
PACKAGE
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

description

The RM4558 and RC4558 are dual general-purpose operational amplifiers with each half electrically similar to uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RM4558 is characterized for operation over the full military temperature range of −55°C to 125°C; the RC4558 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RM4558	RC4558	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	L Package	600	600	mW
	JG or P Package	680	680	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	JG or L package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	P package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES RM4558, RC4558
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

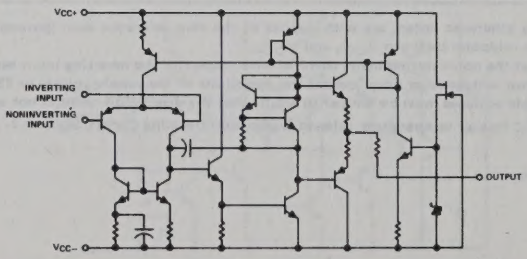
PARAMETER			TEST CONDITIONS†		RM4558			RC4558			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		$R_S \leq 10$ kΩ	25°C		0.5	5		0.5	6	mV
				Full range			6			7.5	
I_{IO}	Input offset current			25°C		5	200		5	200	nA
				Full range			500			300	
I_{IB}	Input bias current			25°C		40	500		40	500	nA
				Full range			1500			800	
V_I	Input voltage range			25°C	±12	±14		±12	±14		V
V_{OPP}	Maximum peak-to-peak output voltage swing		$R_L = 10$ kΩ	25°C	24	28		24	28		V
			$R_L = 2$ kΩ	25°C	20	26		20	26		
			$R_L \geq 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification		$R_L \geq 2$ kΩ, $V_O = \pm 10$ V	25°C	50	350		20	300		V/mV
				Full range	25			15			
B_1	Unity-gain bandwidth			25°C	2	3.5			3		MHz
r_i	Input resistance			25°C	0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio		$R_S \leq 10$ kΩ	25°C	70	90		70	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity		$R_S \leq 10$ kΩ	25°C		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)		$A_{VD} = 100$, $R_S = 1$ kΩ, $f = 1$ kHz, BW = 1 Hz	25°C		10			10		nV/√Hz
I_{CC}	Supply current (Both amplifiers)		No load, No signal	25°C		2.5	5.6		2.5	5.6	mA
				MIN T_A		3.0	6.6		3.0	6.6	
				MAX T_A		2.0	5		2.3	5	
P_D	Total power dissipation (Both amplifiers)		No load, No signal	25°C		75	170		75	170	mW
				MIN T_A		90	200		90	200	
				MAX T_A		60	150		70	150	
V_{o1}/V_{o2}	Channel separation	Open loop	$R_S = 1$ kΩ, $f = 10$ kHz	25°C		105			105		dB
		$A_{VD} = 100$		25°C		105			105		

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for RM4558 is −55°C to 125°C and for RC4558 is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS	RM4558			RC4558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF		0.13			0.13		μs
	Overshoot			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF		1.5			1.0		V/μs

schematic (each amplifier)



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TYPES TL022M, TL022C
DUAL LOW-POWER OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612038, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52L022, SN72L022

- Very Low Power Consumption
- Typical Power Dissipation with ±2-V Supplies . . . 170 μW
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Input Offset Voltage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- Popular Dual Op Amp Pin-Out

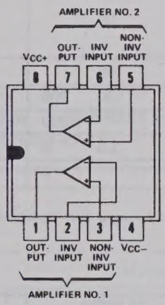
description

The TL022 is a dual low-power operational amplifier designed to replace higher-power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

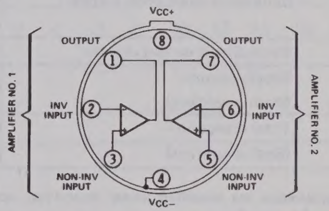
The TL022M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL022C is characterized for operation from 0°C to 70°C.

terminal assignments

JP OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



L
PLUG-IN PACKAGE (TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			TL022M	TL022C	UNIT
Supply voltage V_{CC+} (see Note 1)			22	18	V
Supply voltage V_{CC-} (see Note 1)			−22	−18	V
Differential input voltage (see Note 2)			±30	±30	V
Input voltage (any input, see Notes 1 and 3)			±15	±15	V
Duration of output short-circuit (see Note 4)			unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature range (see Note 5)	Each amplifier		500	500	mW
	Total package	JG or P package	680	680	
		L package	625	625	
Operating free-air temperature range			−55 to 125	0 to 70	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds		JG or L package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds		P package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero-reference level (ground) of the supply voltage where the zero-reference level is the midpoint between V_{CC+} and V_{CC-}. If the zero-reference level of the system is not the midpoint of the supply voltages, all voltage values must be changed accordingly.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES TL022M, TL022C
DUAL LOW-POWER OPERATIONAL AMPLIFIERS

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

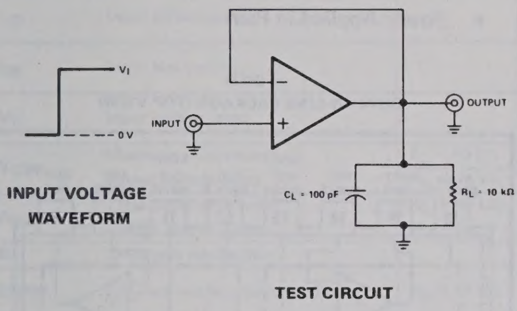
PARAMETER		TEST CONDITIONS†		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leqslant 10$ kΩ	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current		25°C		50	100		100	250	nA
			Full range			250			400	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	25°C	20	26		20	26		V
		$R_L \geqslant 10$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geqslant 10$ kΩ, $V_O = \pm 10$ V	25°C	72	86		60	80		dB
			Full range	72			60			
B_1	Unity-gain bandwidth		25°C		0.8			0.8		MHz
CMRR	Common-mode rejection ratio	$R_S \leqslant 10$ kΩ	25°C	60	72		60	72		dB
			Full range	60			60			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leqslant 10$ kΩ	25°C		30	150		30	200	µV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	$A_{VD} = 20$ dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/$\sqrt{\text{Hz}}$
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (Both amplifiers)	No load, No signal	25°C		130	200		130	250	µA
			Full range			200			250	
P_D	Total dissipation (Both amplifiers)	No load, No signal	25°C		3.9	6		3.9	7.5	mW
			Full range			6			7.5	

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for TL022M is −55°C to 125°C and for TL022C is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10$ kΩ,		0.3			0.3		µs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10$ kΩ, See Figure 1		0.5			0.5		V/µs

PARAMETER MEASUREMENT INFORMATION


V_I
0 V
INPUT
OUTPUT
C_L = 100 pF
R_L = 10 kΩ

INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT FACTOR, AND SLEW RATE

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION vs SUPPLY VOLTAGE

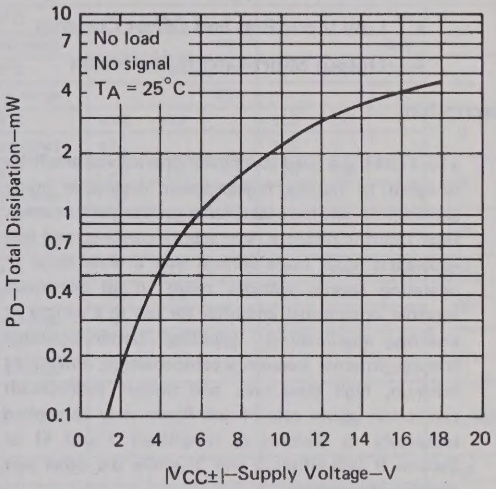
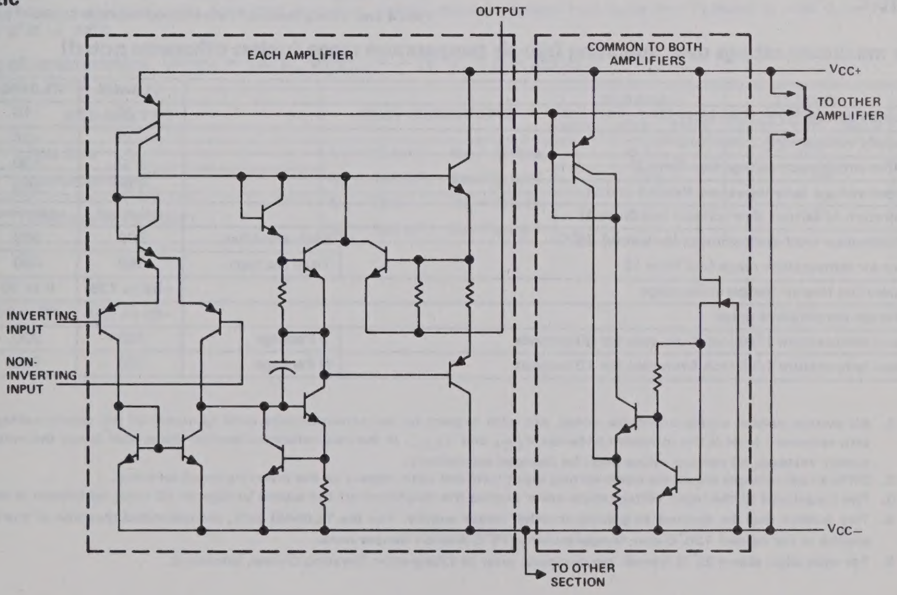


FIGURE 2

schematic


OUTPUT
EACH AMPLIFIER
COMMON TO BOTH AMPLIFIERS
V_CC+
TO OTHER AMPLIFIER
INVERTING INPUT
NON-INVERTING INPUT
V_CC–
TO OTHER SECTION

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TYPES TL044M, TL044C
QUAD LOW-POWER OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612039, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52L044, SN72L044

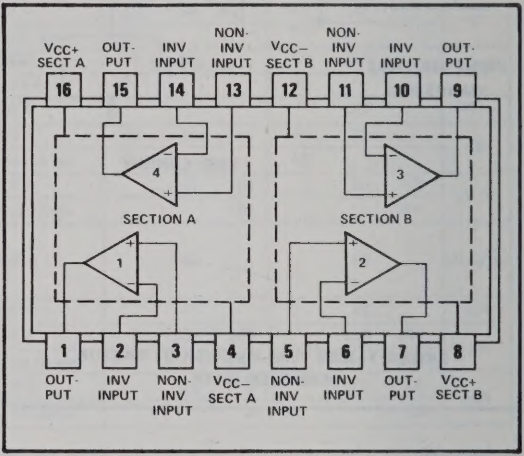
- Very Low Power Consumption
- Typical Power Dissipation with ±2-V Supplies . . . 340 μW
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Input Offset Voltage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- Power Applied in Pairs

description

The TL044 is a quad low-power operational amplifier designed to replace higher-power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use. Power may be applied separately to Section A (amplifiers 1 and 4) or Section B (amplifiers 2 and 3) while the other pair remains unpowered.

The TL044M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL044C is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



Pins 4 and 12 are internally connected together in the N package only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL044M	TL044C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature range (see Note 5)	Each amplifier	500	500	mW
	Total package	680	680	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J Package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N Package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero-reference level (ground) of the supply voltage where the zero-reference level is the midpoint between V_{CC+} and V_{CC-}. If the zero-reference level of the system is not the midpoint of the supply voltages, all voltage values must be changed accordingly.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL044M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

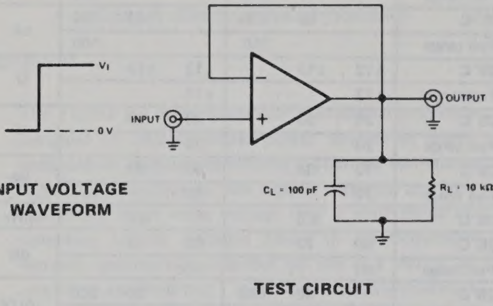
PARAMETER		TEST CONDITIONS†		TL044M			TL044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10$ kΩ	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current		25°C		50	100		100	250	nA
			Full range			250			400	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	25°C	20	26		20	26		V
		$R_L \geq 10$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 10$ kΩ,	25°C	72	86		60	80		dB
		$V_O = \pm 10$ V	Full range	72			60			
B_1	Unity-gain bandwidth		25°C		0.8			0.8		MHz
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	60	72		60	72		dB
			Full range	60			60			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 10$ kΩ	25°C		30	150		30	200	µV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	$A_{VD} = 20$ dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/$\sqrt{Hz}$
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (Four amplifiers)	No load,	25°C		250	400		250	500	µA
		No signal	Full range			400			500	
P_D	Total dissipation (Four amplifiers)	No load,	25°C		7.5	12		7.5	15	mW
		No signal	Full range			12			15	

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for TL044M is −55°C to 125° and for TL044C is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL044M			TL044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV,	$R_L = 10$ kΩ,		0.3			0.3		µs
	Overshoot factor	$C_L = 100$ pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 10$ kΩ, See Figure 1		0.5			0.5		V/µs

PARAMETER MEASUREMENT INFORMATION


V_I
0 V
INPUT
OUTPUT
C_L = 100 pF
R_L = 10 kΩ

INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT FACTOR, AND SLEW RATE

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
vs
SUPPLY VOLTAGE

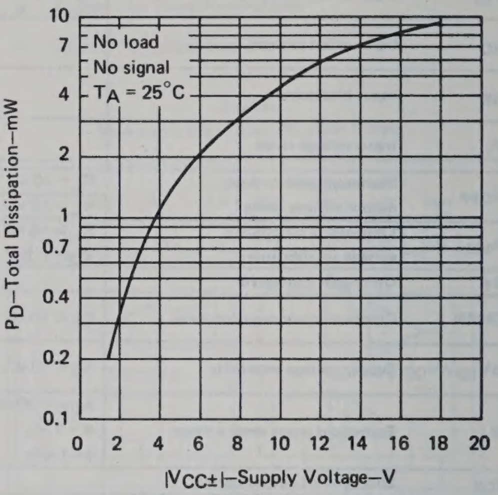
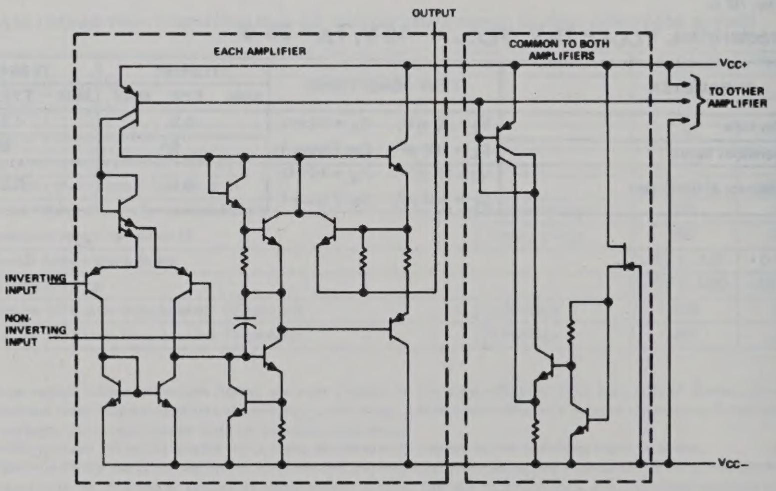


FIGURE 2

schematic (each section)


OUTPUT
EACH AMPLIFIER
COMMON TO BOTH AMPLIFIERS
V_{CC+}
TO OTHER AMPLIFIER
INVERTING INPUT
NON-INVERTING INPUT
V_{CC-}

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FUTURE PRODUCT
TO BE ANNOUNCED

TYPES TL081AC AND TL081C
JFET-INPUT OPERATIONAL AMPLIFIERS

JUNE 1976

- JFET Input Stage
- High Input Impedance. . . $10^9\ \Omega$ Typ
- High Slew Rate Typically 9 V/μs
- Low Input Bias Current . . . 2 nA Typ
- Low Input Offset Current . . . 0.2 nA Typ
- No Frequency Compensation Required
- Continuous-Short-Circuit Protection
- Unity Gain Bandwidth . . . 3 MHz Typ
- No Latch-Up
- Low Power Consumption

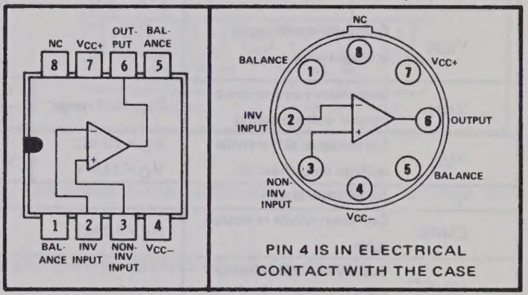
description

This monolithic JFET-input operational amplifier incorporates well-matched, high-voltage BI-FET technology (JFET's on the same chip with standard bipolar transistors). The device features low input bias and offset currents, low offset voltage and offset voltage temperature coefficient, coupled with offset adjustment that does not degrade temperature coefficient or common-mode rejection.

The TL081C is characterized for operation from 0°C to 70°C.

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

L
PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	18 V
Supply voltage V_{CC-} (see Note 1)	−18 V
Differential input voltage (see Note 2)	±30 V
Input voltage (see Notes 1 and 3)	±15 V
Duration of output short-circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	670 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG or L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

TENTATIVE DATA SHEET

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES TL081AC AND TL081C
JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL081AC			TL081C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S = 50\ \Omega$				6		10	15	mV
		$R_S = 50\ \Omega$,	T_A = full range			7.5		13	20	
α_{VIO}	Temperature coefficient of input offset voltage	$R_S = 50\ \Omega$,	T_A = full range		10			10		µV/°C
I_{IO}	Input offset current				0.2	0.5		0.2	0.5	nA
		T_A = full range			0.4	1		0.4	1	
I_{IB}	Input bias current				2	4		2	4	nA
		T_A = full range			3	6		3	6	
V_{ICR}	Common-mode input voltage range			+12 to −12			+10 to −10			V
V_{OPP}	Maximum peak-to-peak output voltage swing	T_A = full range	$R_L \geq 10\ k\Omega$	24	26		24	26		V
			$R_L \geq 2\ k\Omega$	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L = 10\ k\Omega$, $V_O = \pm10$ V	$T_A = 25°C$	25	200		25	200		V/mV
			T_A = full range	15			15			
r_i	Input resistance				10^9			10^9		Ω
CMRR	Common-mode rejection ratio	$R_S = 10\ k\Omega$		70	90		70	90		dB
k_{SVR}*	Supply voltage rejection ratio			70	80		70	80		dB
I_{CC}	Supply current	No load, No signal	$T_A = 25°C$		2	4		2	4	mA
			T_A = full range		3	6		3	6	

*$k_{SVR} = \Delta V_{CC\pm}/\Delta V_{IO}$.

†All characteristics are specified under open-loop operation, unless otherwise noted. Full range for T_A is 0°C to 70°C.

operating characteristics, $V_{CC} = \pm15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL081AC			TL081C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF	$R_L = 2\ k\Omega$,		9			9		V/µs

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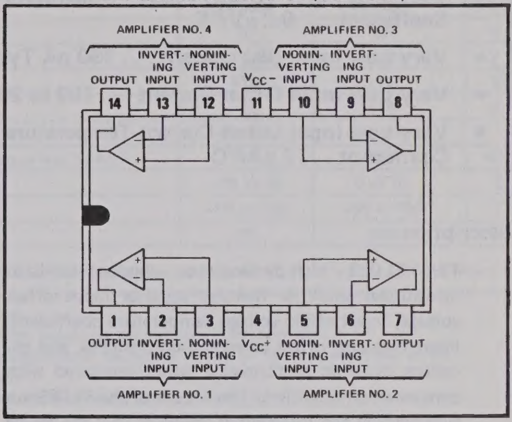
FUTURE PRODUCT
TO BE ANNOUNCED

TYPE TL084C
QUAD JFET-INPUT OPERATIONAL AMPLIFIER

JUNE 1976

- High Input Impedance – JFET Input Stage
- Continuous-Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Gain and Phase Match Between Amplifiers
- High Slew Rate . . . 9 V/μs Typ

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


AMPLIFIER NO. 4
AMPLIFIER NO. 3
OUTPUT
INVERTING INPUT
NONINVERTING INPUT
V_{CC-}
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT
INVERTING INPUT
NONINVERTING INPUT
V_{CC+}
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
AMPLIFIER NO. 1
AMPLIFIER NO. 2

description

The TL084 is a monolithic quadruple JFET-input operational amplifier. The high slew rate, high input impedance, and low input bias and offset currents make this device excellent for high-speed analog applications. The output circuitry has been carefully balanced and symmetrically connected to minimize offset. This device is compatible with the LM324, MC3403, and HA4741 quadruple operational amplifier pinout.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Input voltage	±15 V
Continuous total dissipation at (or below) 25°C free-air temperature	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

electrical characteristics

		MIN	TYP	MAX	UNIT
Input offset voltage:	at 25°C		10	15	mV
	over temperature range			20	mV
Temperature coefficient of input offset voltage			10		μV/°C
Input offset current:	at 25°C		0.2	0.5	nA
	over temperature range			1	nA
Input bias current:	at 25°C		2	4	nA
	over temperature range			6	nA
Maximum peak to peak output voltage swing at 25°C		24	26		V
Large signal differential voltage amplification:	at 25°C	25	200		V/mV
	over temperature range	15			V/mV
Common-mode rejection ratio		70	90		dB
Supply voltage rejection ratio		70	80		dB
Supply current per amplifier			2	4	mA

TENTATIVE DATA SHEET
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES TL089I, TL089C
CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612421, JUNE 1976

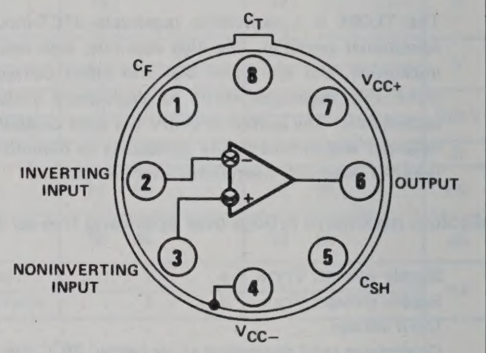
- Very Low Input Offset Voltage . . . 25 to 50 μV Typ
- Very Low Input Offset Voltage Temperature Coefficient . . . 0.2 μV/°C
- Very Low Input Bias Current . . . 150 pA Typ
- Very Low Input Offset Current . . . 100 to 200 pA Typ
- Very Low Input Offset Current Temperature Coefficient . . . 2 pA/°C
- Output Short-Circuit Protection
- High Slew Rate . . . 10 V/μs Typ
- High Gain-Bandwidth Product . . . 3 MHz Typ
- Wide Common-Mode and Differential Voltage Ranges
- Very High Voltage Amplification . . . 175 dB Typ

description

The TL089 high-performance chopper-stabilized operational amplifier features superior input offset voltage, input offset voltage temperature coefficient, input bias and offset current characteristics, and excellent dynamic performance when compared with conventional amplifiers. The inputs of the TL089 are symmetrical and differential, meaning that the device may be operated in any conventional op-amp feedback configuration. Applications include high-gain dc instrumentation, precision integrators, and as a substitute for other operational amplifiers wherever much lower errors without external adjustments are required. The TL089 can replace the Harris HA2900 series of devices in most applications. It is available in an eight-pin hermetic plug-in package with standard pin-out and requires only three capacitors for operation.

The TL089I is characterized for operation from −25°C to 85°C and the TL089C from 0°C to 70°C.

L PLUG-IN PACKAGE
(TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

functional block diagram

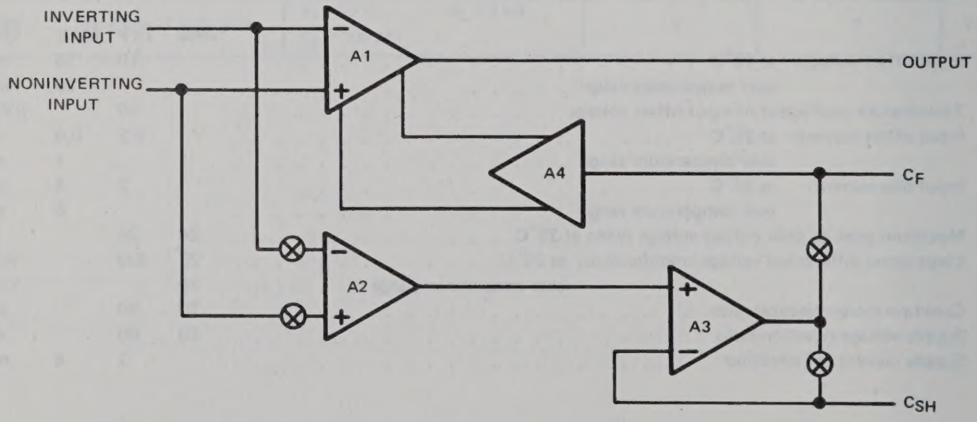


FIGURE 1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL089I	TL089C	UNIT
Supply voltage, V_{CC+} (see Note 1)	20	20	V
Supply voltage, V_{CC-} (see Note 1)	−20	−20	V
Differential input voltage (see Note 2)	±15	±15	V
Input voltage (any input, see Notes 1 and 3)	±15	±15	V
Duration of output short-circuit (see Note 4)	unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	625	625	mW
Operating free-air temperature range	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	300	300	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero-reference level (ground) of the supply voltages where the zero-reference level is the midpoint between V_{CC+} and V_{CC-}. If the zero-reference level of the system is not the midpoint of the supply voltages, all voltage values must be changed accordingly.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

	TL089I		TL089C		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC+}	10	20	10	20	V
Supply voltage, V_{CC-}	−10	−20	−10	−20	V
Operating free-air temperature, T_A	−25	85	0	70	°C

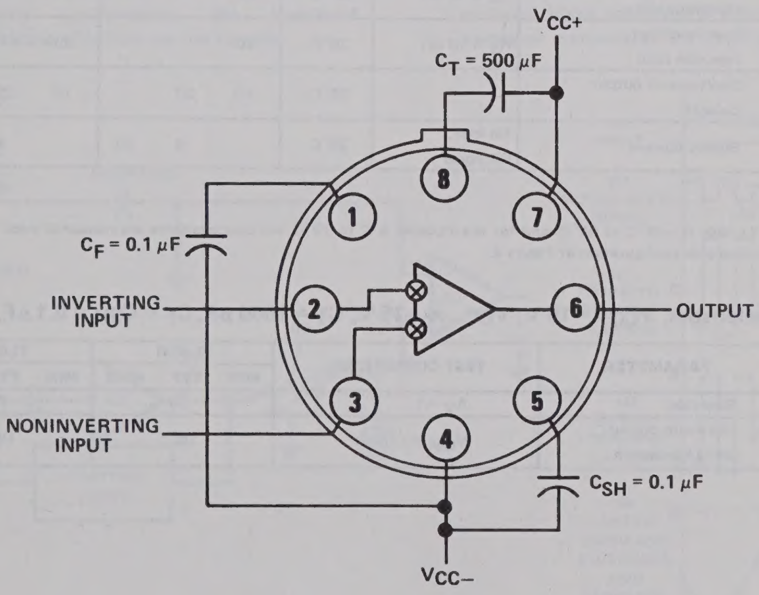


FIGURE 2–TYPICAL GAIN CONFIGURATION SHOWING EXTERNAL COMPONENTS

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		TL089I			TL089C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		25	50		50	150	μV
			Full range			80			200	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		0.2			0.2		μV/°C
I_{IO}	Input offset current		25°C		100	300		200	600	pA
			Full range			600			1000	
α_{IIO}	Average temperature coefficient of input offset current		Full range		2			2		pA/°C
I_{IB}	Input bias current		25°C		150	500		150	1000	pA
			Full range			10			15	nA
V_{ICR}	Common-mode input voltage range		25°C	±10			±10			V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 2 kΩ	25°C	20	24		20	24		V
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, V_O = ±10 V	25°C	100	175		100	175		dB
f_{ch}	Chopper frequency		25°C		400			400		Hz
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		100			100		MΩ
r_o	Output resistance		25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ	25°C	80			80			dB
k_{SVR}*	Supply voltage rejection ratio	$R_S \leq$ 10 kΩ	25°C	80			80			dB
I_{OS}	Short-circuit output current		25°C	10	20		10	20		mA
I_{CC}	Supply current	No load, No signal	25°C		6	10		6	10	mA

*$k_{SVR} = \Delta V_{CC}/\Delta V_{IO}$.

†Full range for the TL089I is −25°C to 85°C and for the TL089C 0°C to 70°C. All characteristics are measured with external components connected in the typical gain configuration of Figure 2.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, C_T = 1500 pF, C_F = C_{SH} = 0.1 μF, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL089I			TL089C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_V = 1		10			10		V/μs
B_{OM}	Maximum-output-swing bandwidth	$V_{OM} \geq$ ±10 V		160			160		kHz

PRINCIPLES OF OPERATION

Traditional integrated operational amplifiers have inherent problems that cause inaccuracies in many of the dc and very-low-frequency applications of these devices. The major problems are:

1. Input offset voltage
2. Thermally-induced change of input offset voltage
3. Input offset current
4. Thermally-induced change of input offset current
5. Gain deficiencies
6. Input resistance effects

Chopper stabilization is a technique that is effective in substantially reducing the initial and long-term input offset voltage, input-offset-voltage drift and gain deficiencies. Other circuit techniques can be utilized to reduce the effects of offset current, offset-current drift, and input resistance effects.

Most chopper-stabilized amplifiers feature single-ended, inverting operation. These are available as bulky modular devices fabricated by discrete or hybrid approaches. For space-critical applications, or for applications requiring the noninverting or common-mode configuration, the traditional chopper-stabilized amplifiers are not suitable.

The TL089 is an effective application of chopper-stabilization techniques to an integrated circuit design. It is fabricated in a popular standard package and incorporates a unique differential-input configuration that permits common-mode input voltages and application in inverting or noninverting configurations. Circuit techniques and state-of-the-art technologies have been combined to provide low input bias current, low input offset current, low offset-voltage temperature coefficient and drift, and very high input resistance.

The following discussion is provided to familarize the user with chopper-stabilization techniques. For simplicity, the technique will be described first by reference to a simplified single-ended chopper-stabilized amplifier. Principles will then be extended to the TL089 differential-input integrated-circuit operation amplifier.

The general approach to chopper stabilization is accomplished by processing low-frequency signal components separately from the higher-frequency components. This is illustrated in Figure 3. The upper signal path passes higher-frequency (>100 hertz, for example) signal components directly. These higher-frequency components are amplified directly by the

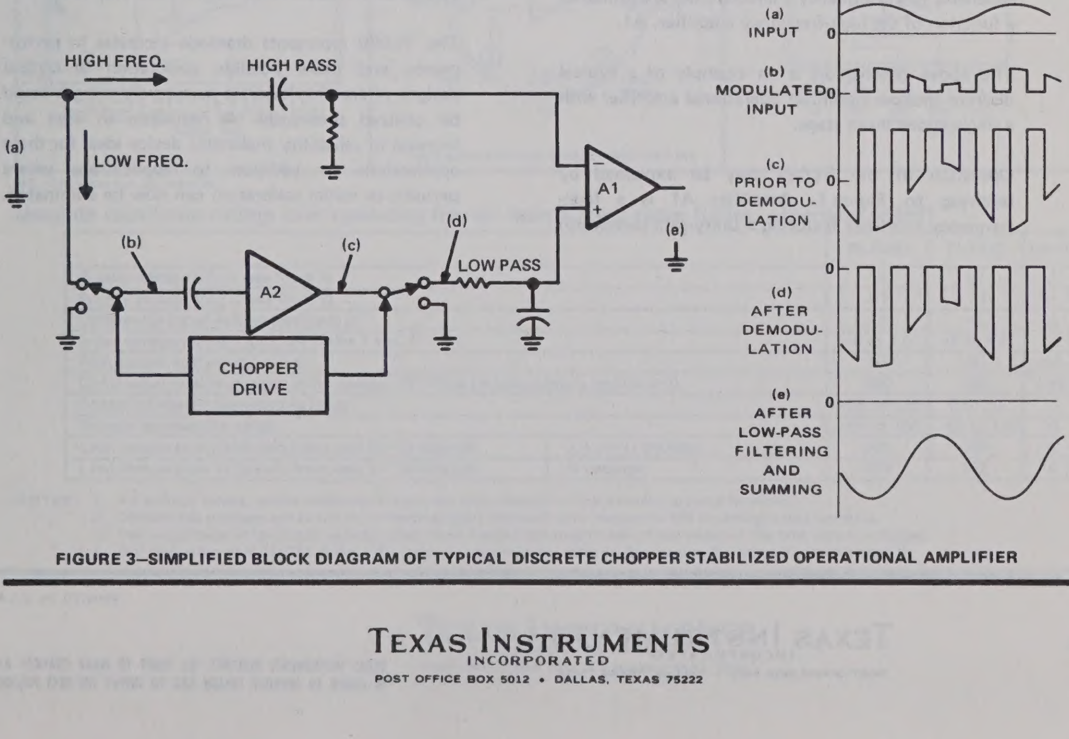


FIGURE 3–SIMPLIFIED BLOCK DIAGRAM OF TYPICAL DISCRETE CHOPPER STABILIZED OPERATIONAL AMPLIFIER

wide-band amplifier, A1. The low-frequency components (<100 hertz in this example) are processed through the lower signal path — the chopper channel. The low-frequency signal is periodically shunted to ground by the action of the input chopper. The resulting waveform at the output of this chopper is amplified by applying it to the ac amplifier, A2. After amplification, the signal is demodulated in synchronism with the input chopper switch to restore the proper dc level. A low-pass filter smooths the demodulated signal and attenuates any noise created by the demodulation switch. The resultant low-frequency signal is finally amplified by the high-frequency amplifier, A1. The chopper path, therefore, processes the low-frequency signal components by converting them to higher-frequency ac signals, amplifying them, and finally converting them back to low-frequency components by demodulation. This technique reduces the offset and drift of amplifier A1 by the gain of the chopper amplifier. Overall low-frequency gain is a combination of the gain of the higher frequency and lower frequency channels.

This chopper-stabilization technique results in extremely high low-frequency gains and extremely low voltage offset. Since reduction in offset-voltage change does not depend on cancellation of change due to matched components, the chopper-stabilized amplifier is relatively immune to change due to thermal effects. Long-term-drift stability is also excellent. High-frequency characteristics are primarily a function of the high-frequency amplifier, A1.

The above description is an example of a typical discrete chopper-stabilized operational amplifier with a single-ended input stage.

Operation of the TL089 may be explained by referring to Figure 1. Amplifier A1 is a high-frequency amplifier featuring a unity-gain bandwidth of 3 MHz and a unity-gain slew rate of 10 volts per microsecond. Frequency compensation is internal.

The low-frequency input signals are "chopped" by the differential input chopper periodically shorting the differential inputs together. During this interval of time, the offsets of amplifiers A2, A3, and other system errors are cancelled out. The sample-hold capacitor, C_{SH}, holds this condition during the next interval of time, while the input chopper couples the offset voltage of A1 to the input of A2. After amplification by A2 and A3, this signal is demodulated by the synchronous demodulator.

The output of amplifier A4 is used to null the initial offset of amplifier A1. This nulling is accomplished at a point in the input stage of A1 that is similar to the external null-offset terminals of a conventional integrated-circuit operational amplifier. The chopper-stabilization circuit samples and nulls the offset of A1 at a 750-Hz rate, thereby effecting an almost continuous correction of offset. While A2 and A3 are in a state of auto-zero, capacitor C_F retains the previous correction voltage at the input of A4.

Using the basic differential-input chopper stabilization technique described above results in input voltage offset and drift much superior to conventional integrated-circuit operational amplifiers. A review and comparison will also reveal input current, input offset current, bandwidth, slew rate, and voltage amplification superior to these amplifiers.

The TL089 represents dramatic increases in performance and make possible application in critical designs where only discrete or modular designs could be utilized previously. A reduction in cost and increase in reliability make this device ideal for these applications in addition to applications where periodic or initial calibration can now be eliminated.

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LINEAR
INTEGRATED CIRCUITS

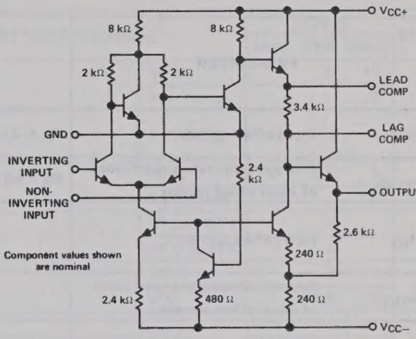
TYPES TL702M, TL702C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612407, JUNE 1976

FORMERLY SN52702, SN72702

- Open-Loop Voltage Amplification . . . 2600 Typ
- CMRR . . . 80 dB Typ

schematic


VCC+
8 kΩ
8 kΩ
2 kΩ
2 kΩ
LEAD COMP
3.4 kΩ
GND
LAG COMP
INVERTING INPUT
2.4 kΩ
NON-INVERTING INPUT
OUTPUT
2.6 kΩ
Component values shown are nominal
240 Ω
2.4 kΩ
480 Ω
240 Ω
VCC−

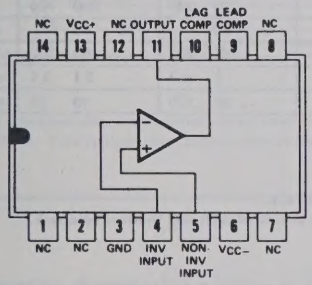
description

The TL702 is a high-gain, wideband operational amplifier having differential inputs and single-ended emitter-follower outputs. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Component matching, inherent in silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. The TL702 is particularly useful for applications requiring transfer or generation of linear and non-linear functions up to a frequency of 30 MHz.

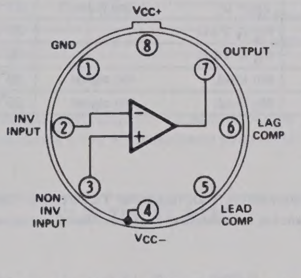
The TL702M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL702C is characterized for operation over the temperature range of 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

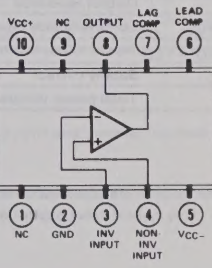

NC
VCC+
NC
OUTPUT
LAG COMP
LEAD COMP
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
GND
INV INPUT
NON-INV INPUT
VCC−
NC

L PLUG-IN PACKAGE (TOP VIEW)


VCC+
GND
OUTPUT
8
1
7
INV INPUT
2
6
LAG COMP
3
5
NON-INV INPUT
4
LEAD COMP
VCC−

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)


VCC+
NC
OUTPUT
LAG COMP
LEAD COMP
10
9
8
7
6
1
2
3
4
5
NC
GND
INV INPUT
NON-INV INPUT
VCC−

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL702M	TL702C	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		−6 to 1.5	−6 to 1.5	V
Peak output current ($t_w \leq 1$ s)		50	50	mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the lesser of the two supply voltages.
4. For operation of TL702M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES TL702M, TL702C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

TL702M

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS†			TL702M						UNIT
					$V_{CC+} = 12$ V $V_{CC-} = -6$ V			$V_{CC+} = 6$ V $V_{CC-} = -3$ V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 2$ kΩ		25°C		2	5		2	5	mV
				Full range			6			6	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50$ Ω		−55°C to 25°C		10			10		μV/°C
				25°C to 125°C		5			5		
I_{IO}	Input offset current			25°C		0.5	2		0.3	2	μA
				−55°C		1	3			3	
				125°C		0.2	3			3	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		6			5		nA/°C
				25°C to 125°C		3			2		
I_{IB}	Input bias current			25°C		4	10		2.5	7	μA
				−55°C		6.5	20			14	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100$ kΩ			10	10.6		5	5.4		V
		$R_L = 10$ kΩ				8			4		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100$ kΩ	$V_O = \pm 5$ V	25°C	1400	2600					
				Full range	1000						
			$V_O = \pm 2.5$ V	25°C				380	700		
r_i	Input resistance			25°C	8	25		12	40		kΩ
				Full range	3			4			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2$ kΩ		25°C	70	80		70	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 2$ kΩ		25°C		60	300		60	300	μV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.9	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	35	mW

† All characteristics are specified under open-loop operation. Full range for TL702M is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

TL702C

electrical characteristics at specified free-air temperature, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V

PARAMETER		TEST CONDITIONS†			TL702C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 2$ kΩ		25°C		5	10	mV
				Full Range			15	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50$ Ω		Full Range		5		µV/°C
I_{IO}	Input offset current			25°C		0.5	5	µA
				Full Range			7.5	
α_{IIO}	Average temperature coefficient of input offset current			0°C to 25°C		5		nA/°C
				25°C to 70°C		3		
I_{IB}	Input bias current			25°C		4	15	µA
				0°C		4.5	20	
V_I	Input voltage range	Positive swing		25°C	0.5	1		V
		Negative swing			−4	−5		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100$ kΩ		25°C	10	10.6		V
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100$ kΩ,	$V_O = \pm 5$ V	25°C	1000	2600		
				Full Range	800			
r_i	Input resistance			25°C	6	25		kΩ
				Full Range	3.5			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	600	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2$ kΩ		25°C	65	80		dB
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 2$ kΩ		25°C		60	300	µV/V
I_{CC}	Supply current	No load,	No signal	25°C		5	7	mA
P_D	Total power dissipation	No load,	No signal	25°C		90	125	mW

†All characteristics are specified under open-loop operation. Full range for TL702C is 0°C to 70°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

TL702M, TL702C

operating characteristics $V_{CC+} = 12$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		BOTH TYPES			UNIT
					MIN	TYP	MAX	
t_r	Rise time	1	$V_I = 10$ mV,	$C_L = 0$		25	120	ns
		2	$V_I = 1$ mV			10	30	ns
	Overshoot factor	1	$V_I = 10$ mV,	$C_L = 100$ pF		10%	50%	
		2	$V_I = 1$ mV			20%	40%	
SR	Slew rate	1	$V_I = 6$ V,	$C_L = 100$ pF		1.7		V/µs
		2	$V_I = 100$ mV			11		

PARAMETER MEASUREMENT INFORMATION

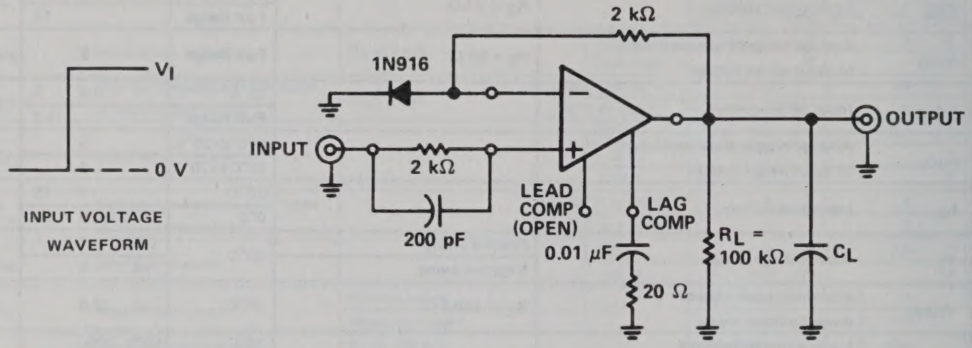

V_I
0 V
INPUT VOLTAGE WAVEFORM
2 kΩ
1N916
INPUT
2 kΩ
200 pF
LEAD COMP (OPEN)
LAG COMP
0.01 μF
20 Ω
R_L = 100 kΩ
C_L
OUTPUT

FIGURE 1–UNITY-GAIN AMPLIFIER

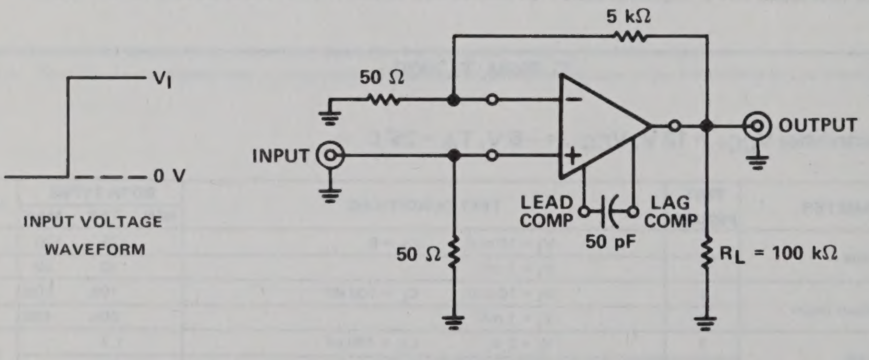

V_I
0 V
INPUT VOLTAGE WAVEFORM
5 kΩ
50 Ω
INPUT
50 Ω
LEAD COMP
50 pF
LAG COMP
R_L = 100 kΩ
OUTPUT

FIGURE 2–GAIN-OF-100 AMPLIFIER

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY
(for various lag compensations)

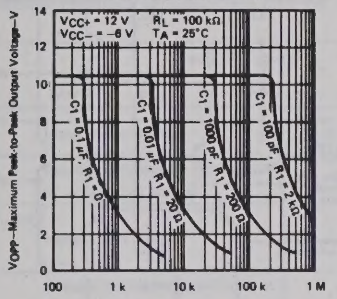
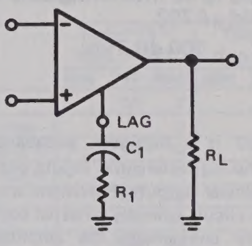


FIGURE 3



LAG COMPENSATION CIRCUIT
FOR FIGURES 3, 4, AND 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

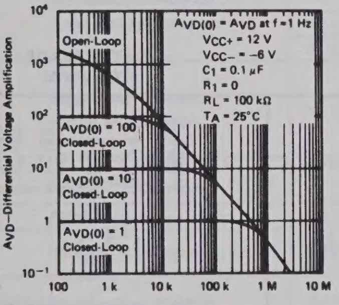


FIGURE 4

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

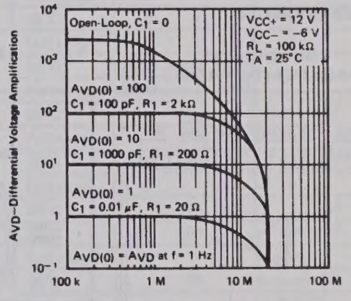


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

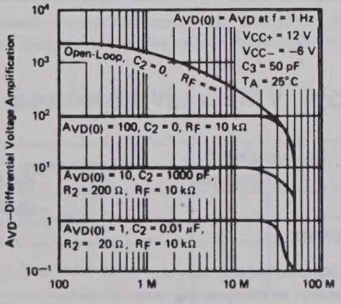
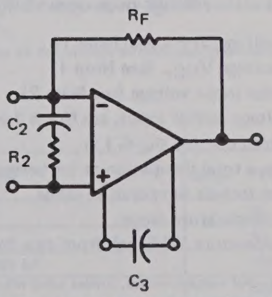


FIGURE 6



LEAD-LAG COMPENSATION CIRCUIT
FOR FIGURE 6

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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

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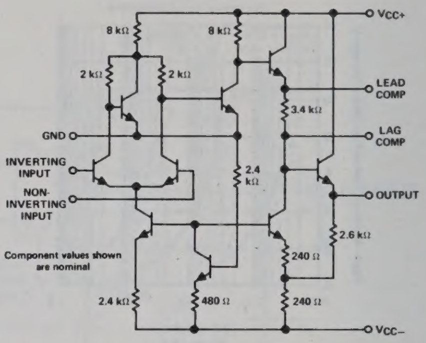
TYPE uA702M
GENERAL-PURPOSE OPERATIONAL AMPLIFIER

BULLETIN NO. DL-S 7612408, JUNE 1976

FORMERLY SN52702A

- Open-Loop Voltage Amplification . . . 3600 Typ
- Designed to be Interchangeable With Fairchild μA702
- CMRR . . . 100 dB Typ

schematic


VCC+
8 kΩ
8 kΩ
2 kΩ
2 kΩ
LEAD COMP
3.4 kΩ
GND
LAG COMP
INVERTING INPUT
2.4 kΩ
NON-INVERTING INPUT
OUTPUT
2.6 kΩ
240 Ω
2.4 kΩ
480 Ω
240 Ω
VCC–

Component values shown are nominal

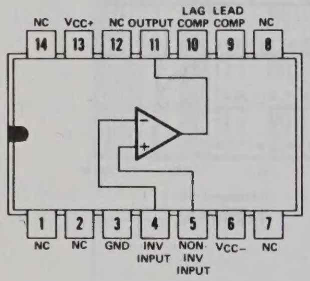
description

The uA702 is a high-gain, wideband operational amplifier having differential inputs and single-ended emitter-follower outputs. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. Component matching, inherent in silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. The uA702 is particularly useful for applications requiring transfer or generation of linear and non-linear functions up to a frequency of 30 MHz.

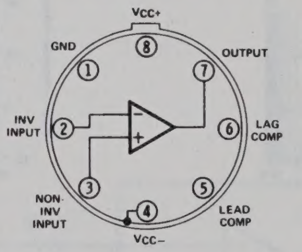
The uA702M is characterized for operation over the full military temperature range of –55°C to 125°C.

terminal assignments

J DUAL-IN-LINE
PACKAGE (TOP VIEW)

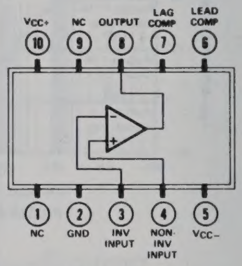

NC
VCC+
NC
OUTPUT
LAG COMP
LEAD COMP
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
GND
INV INPUT
NON-INV INPUT
VCC–
NC

L PLUG-IN PACKAGE
(TOP VIEW)


VCC+
GND
OUTPUT
INV INPUT
LAG COMP
NON-INV INPUT
LEAD COMP
VCC–
1
2
3
4
5
6
7
8

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U
FLAT PACKAGE
(TOP VIEW)


VCC+
NC
OUTPUT
LAG COMP
LEAD COMP
10
9
8
7
6
1
2
3
4
5
NC
GND
INV INPUT
NON-INV INPUT
VCC–

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	–7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Notes 1 and 3)	–6 V to 1.5 V
Peak output current ($t_W \leq 1$ s)	50 mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4)	300 mW
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or U package	300°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the lesser of the two supply voltages.
4. For operation above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature

	PARAMETER	TEST CONDITIONS†			V_{CC+} = 12 V V_{CC-} = −6 V			V_{CC+} = 6 V V_{CC-} = −3 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 2\ k\Omega$		25°C		0.5	2		0.7	3	mV
				Full range			3			4	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$		−55°C to 25°C		2	10		3	15	µV/°C
				25°C to 125°C		2.5	10		3.5	15	
I_{IO}	Input offset current			25°C		0.2	0.5		0.12	0.5	µA
				−55°C		0.4	1.5		0.3	1.5	
				125°C		0.08	0.5		0.05	0.5	
α_{IIO}	Average temperature coefficient of input offset current			−55°C to 25°C		3	16		2	13	nA/°C
				25°C to 125°C		1	5		0.7	4	
I_{IB}	Input bias current			25°C		2	5		1.2	3.5	µA
				−55°C		4.3	10		2.6	7.5	
V_I	Input voltage range	Positive swing		25°C	0.5	1		0.5	1		V
		Negative swing			−4	−5		−1.5	−2		
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 100\ k\Omega$		25°C	10	10.6		5	5.4		V
				Full range	10			5			
		$R_L = 10\ k\Omega$		25°C	7	8		3	4		
		$R_L \geq 10\ k\Omega$		Full range	7			3			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 100\ k\Omega$	$V_O = \pm 5$ V	25°C	2500	3600	6000				
				Full range	2000		7000				
			$V_O = \pm 2.5$ V	25°C				600	900	1500	
				Full range				500		1750	
r_i	Input resistance			25°C	16	40		22	67		kΩ
				Full range	6			8			
r_o	Output resistance	$V_O = 0$,	See Note 3	25°C		200	500		300	700	Ω
CMRR	Common-mode rejection ratio	$R_S \leq 2\ k\Omega$		25°C	80	100		80	100		dB
				Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 2\ k\Omega$		25°C		75			75		µV/V
				Full range			200			200	
I_{CC}	Supply current	No load,	No signal	25°C		5	6.7		2.1	3.3	mA
				−55°C		5	7.5		2.1	3.9	
				125°C		4.4	6.7		1.7	3.3	
P_D	Total power dissipation	No load,	No signal	25°C		90	120		19	30	mW
				−55°C		90	135		19	35	
				125°C		80	120		15	30	

†All characteristics are specified under open-loop operation. Full range is −55°C to 125°C.

NOTE 3: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

	PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise time	1	$V_I = 10$ mV,	$C_L = 0$		25	120	ns
		2	$V_I = 1$ mV			10	30	ns
	Overshoot factor	1	$V_I = 10$ mV,	$C_L = 100$ pF		10%	50%	
		2	$V_I = 1$ mV			20%	40%	
SR	Slew rate	1	$V_I = 6$ V,	$C_L = 100$ pF		1.7		V/µs
		2	$V_I = 100$ mV			11		

PARAMETER MEASUREMENT INFORMATION

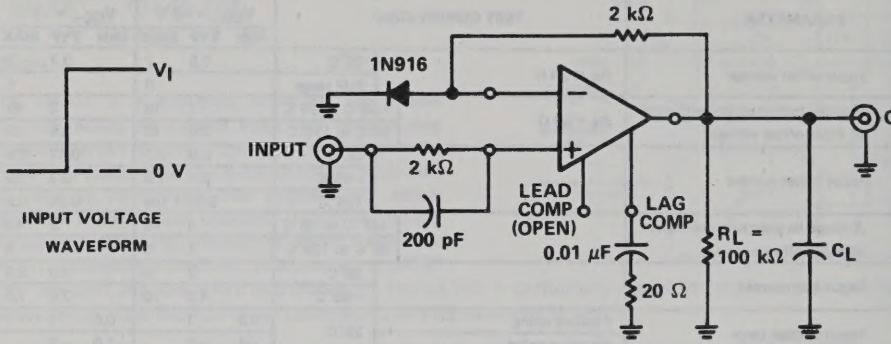

V_I
0 V
INPUT VOLTAGE
WAVEFORM
2 kΩ
1N916
INPUT
2 kΩ
200 pF
LEAD
COMP
(OPEN)
LAG
COMP
0.01 μF
20 Ω
R_L =
100 kΩ
C_L
OUTPUT

FIGURE 1—UNITY-GAIN AMPLIFIER

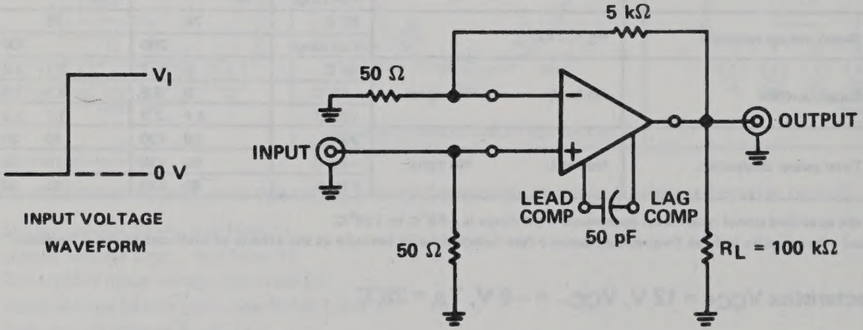

V_I
0 V
INPUT VOLTAGE
WAVEFORM
5 kΩ
50 Ω
INPUT
50 Ω
LEAD
COMP
50 pF
LAG
COMP
R_L = 100 kΩ
OUTPUT

FIGURE 2—GAIN-OF-100 AMPLIFIER

TYPE uA702M
GENERAL-PURPOSE OPERATIONAL AMPLIFIER

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY
(for various lag compensations)

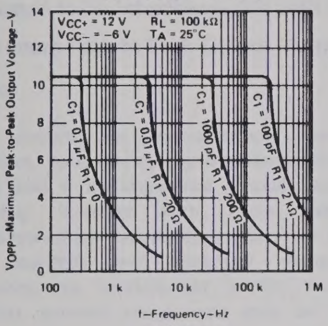
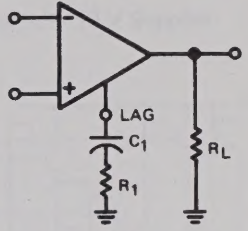


FIGURE 3



LAG COMPENSATION CIRCUIT
FOR FIGURES 3, 4, AND 5

LARGE SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

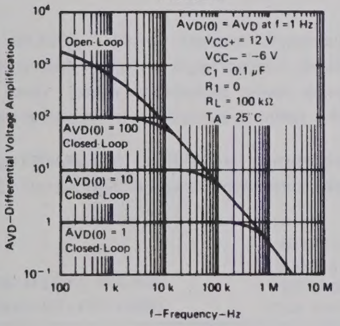


FIGURE 4

LARGE SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

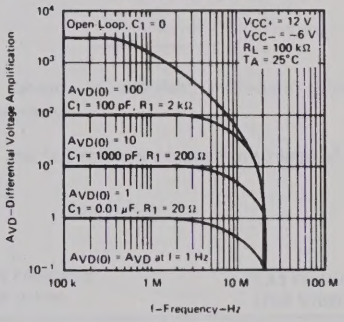


FIGURE 5

LARGE SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY
(for various lag compensations)

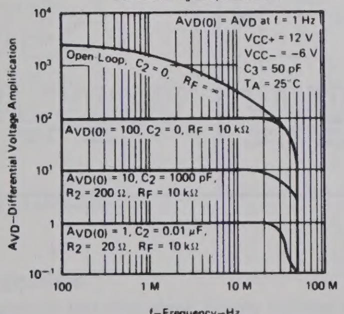
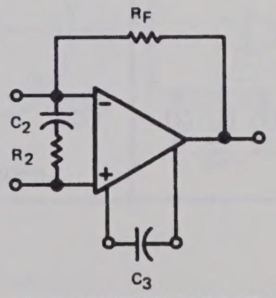


FIGURE 6



LEAD-LAG COMPENSATION CIRCUIT
FOR FIGURE 6

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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

TYPES uA709AM, uA709M, uA709C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611447, FEBRUARY 1971—REVISED JUNE 1976

FORMERLY SN52709A, SN52709, SN72709

- **Common-Mode Input Range . . . ±10 V Typical**
- **Designed to be Interchangeable with Fairchild μA709A, μA709, and μA709C**
- **Maximum Peak-to-Peak Output Voltage Swing . . . 28 V Typical with 15 V Supplies**

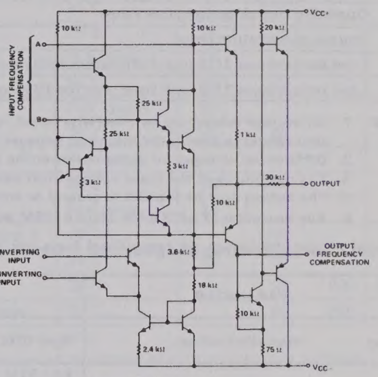
description

These circuits are general-purpose operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

The uA709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the uA709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are guaranteed.

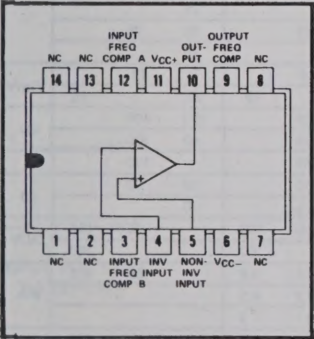
The uA709AM and uA709M are characterized for operation over the full military temperature range of −55°C to 125°C. The uA709C is characterized for operation from 0°C to 70°C.

schematic

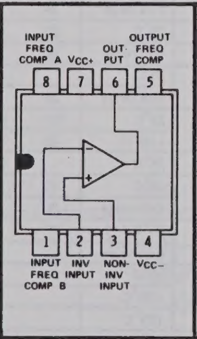

VCC+
10 kΩ
10 kΩ
20 kΩ
A
INPUT FREQUENCY COMPENSATION
B
25 kΩ
25 kΩ
1 kΩ
3 kΩ
3 kΩ
30 kΩ
OUTPUT
10 kΩ
INVERTING INPUT
NONINVERTING INPUT
3.6 kΩ
OUTPUT FREQUENCY COMPENSATION
18 kΩ
10 kΩ
2.4 kΩ
75 Ω
VCC−

Component values shown are nominal.

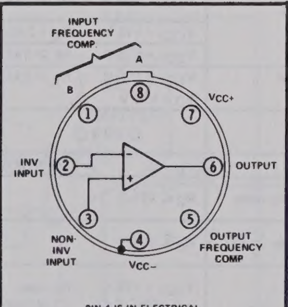
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
NC
INPUT FREQ COMP A
VCC+
OUTPUT
OUTPUT FREQ COMP
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
INPUT FREQ COMP B
INV INPUT
NON-INV INPUT
VCC−
NC

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

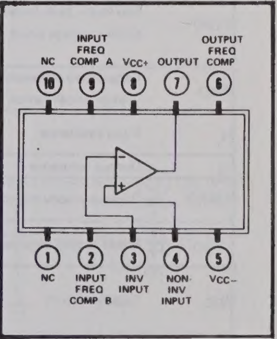

INPUT FREQ COMP A
VCC+
OUT-PUT
OUTPUT FREQ COMP
8
7
6
5
1
2
3
4
INPUT FREQ COMP B
INV INPUT
NON-INV INPUT
VCC−

L PLUG-IN PACKAGE (TOP VIEW)


INPUT FREQUENCY COMP.
A
B
8
VCC+
1
7
INV INPUT
2
6
OUTPUT
3
5
4
NON-INV INPUT
VCC−
OUTPUT FREQUENCY COMP

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)


NC
INPUT FREQ COMP A
VCC+
OUTPUT
OUTPUT FREQ COMP
10
9
8
7
6
1
2
3
4
5
NC
INPUT FREQ COMP B
INV INPUT
NON-INV INPUT
VCC−

NC—No internal connection

voltages specified

Throughout this data sheet, supply voltages are specified either as a range or as a specific value. A positive voltage within the specified range (or of the specified value) is applied to V_{CC+}, and an equal negative voltage is applied to V_{CC-}.

TYPES uA709AM, uA709M, uA709C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA709AM uA709M	uA709C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 5)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation of uA709AM and uA709M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 9$ V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		uA709AM			uA709M			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		0.6	2		1	5	mV
			Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$	Full range		1.8	10		3		µV/°C
		$R_S = 10\ k\Omega$	−55°C to 25°C		4.8	25		6		
			25°C to 125°C		2	15		6		
I_{IO}	Input offset current		25°C		10	50		50	200	nA
			−55°C		40	250		100	500	
			125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current		−55°C to 25°C		0.45	2.8				nA/°C
			25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current		25°C		0.1	0.2		0.2	0.5	µA
			−55°C		0.3	0.6		0.5	1.5	
V_I	Input voltage range	$V_{CC\pm} = \pm 15$ V	25°C	±8	±10		±8	±10		V
			Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm} = \pm 15$ V, $R_L \geq 10\ k\Omega$	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm} = \pm 15$ V, $R_L = 2\ k\Omega$	25°C	20	26		20	26		
		$V_{CC\pm} = \pm 15$ V, $R_L \geq 2\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 15$ V, $R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	25°C		45			45		V/mV
			Full range	25		70	25		70	
r_i	Input resistance		25°C	350	750		150	400		kΩ
			−55°C	85	185		40	100		
r_o	Output resistance	$V_O = 0$, See Note 6	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	80	110		70	90		dB
			Full range	80			70			
$\Delta V_{IO}/\Delta V_{CC}$	Power supply sensitivity	$R_S \leq 10\ k\Omega$	25°C		40	100		25	150	µV/V
			Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm} = \pm 15$ V, No load, No signal	25°C		2.5	3.6		2.6	5.5	mA
			−55°C		2.7	4.5				
			125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm} = \pm 15$ V, No load, No signal	25°C		75	108		78	165	mW
			−55°C		81	135				
			125°C		63	90				

†All characteristics are specified under open-loop operation. Full range for uA709AM and uA709M is −55°C to 125°C.

‡All typical values are at $V_{CC\pm} = \pm 15$ V.

Note 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm} = \pm 15$ V)

PARAMETER		TEST CONDITIONS†		uA709C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm} = \pm 9$ V to ± 15 V, $R_S \leq 10$ kΩ	25°C		2	7.5	mV
			Full range			10	
I_{IO}	Input offset current	$V_{CC\pm} = \pm 9$ V to ± 15 V	25°C		100	500	nA
			Full range			750	
I_{IB}	Input bias current	$V_{CC\pm} = \pm 9$ V to ± 15 V	25°C		0.3	1.5	µA
			Full range			2	
V_I	Input voltage range		25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \geq 10$ kΩ	25°C	24	28		V
			Full range	24			
		$R_L = 2$ kΩ	25°C	20	26		
		$R_L \geq 2$ kΩ	Full range	20			
A_{VD}	Large-signal differential voltage amplification	$R_L \leq 2$ kΩ, $V_O = \pm 10$ V	25°C	15	45		V/mV
			Full range	12			
r_i	Input resistance		25°C	50	250		kΩ
			Full range	35			
r_o	Output resistance	$V_O = 0$, See Note 6	25°C		150		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ	25°C	65	90		dB
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 10$ kΩ	25°C		25	200	µV/V
P_D	Total power dissipation	No load, No signal	25°C		80	200	mW

†All characteristics are specified under open-loop operation. Full range for uA709C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm} = \pm 9$ V to ± 15 V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS		uA709AM uA709M uA709C			UNIT
				MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, See Figure 1	$C_L = 0$		0.3	1	µs
	Overshoot factor		$C_L = 100$ pF		6%	30%	

PARAMETER MEASUREMENT INFORMATION

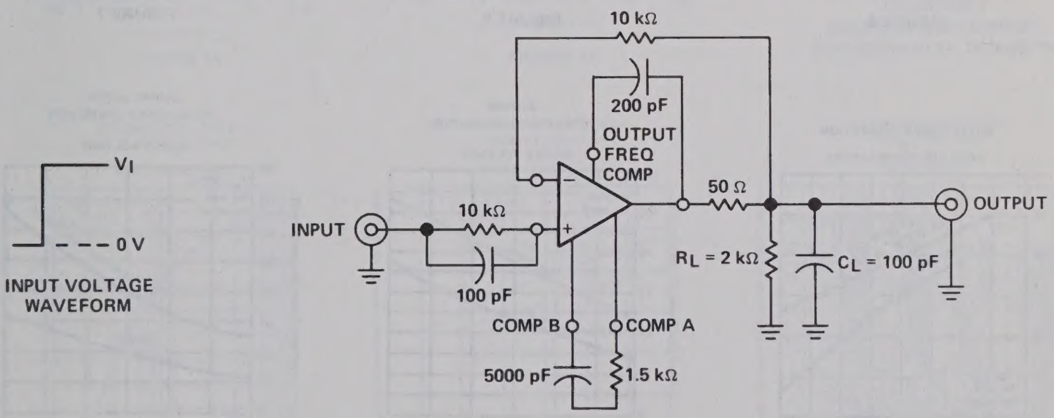


FIGURE 1—RISE TIME AND SLEW RATE

TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

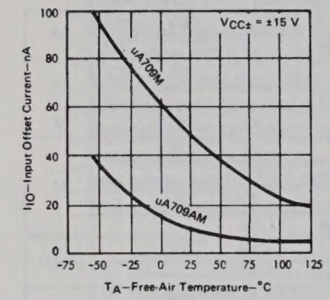


FIGURE 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

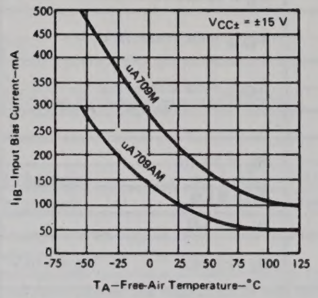


FIGURE 3

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

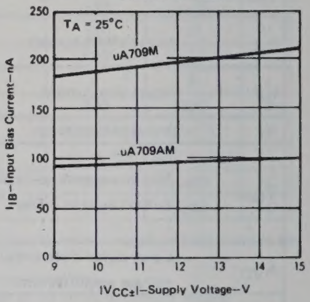


FIGURE 4

INPUT VOLTAGE RANGE
vs
SUPPLY VOLTAGE

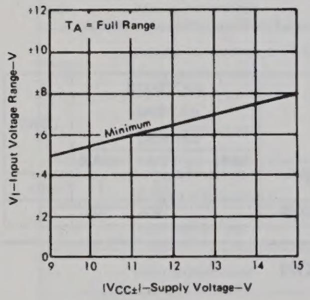


FIGURE 5

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

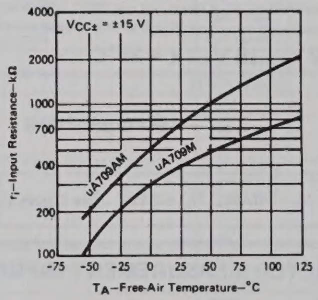


FIGURE 6

uA709AM
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

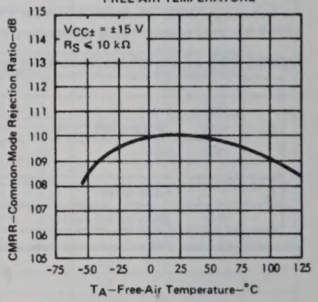


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

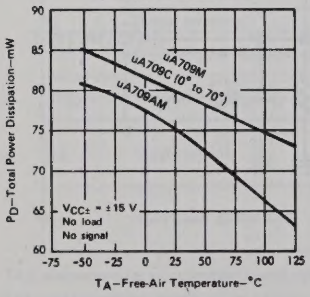


FIGURE 8

uA709AM
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

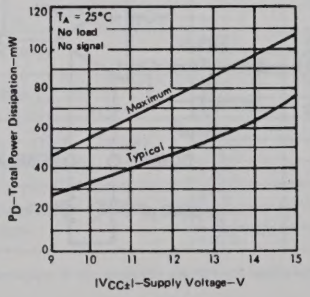


FIGURE 9

uA709M, uA709C
TOTAL POWER DISSIPATION
vs
SUPPLY VOLTAGE

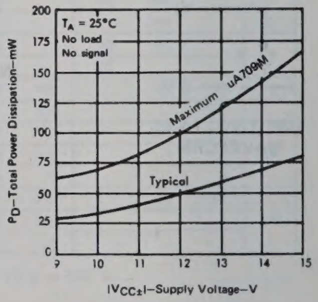


FIGURE 10

TYPICAL CHARACTERISTICS
(unless designated maximum or minimum)

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

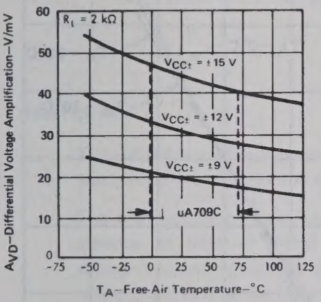


FIGURE 11

uA709AM, uA709M
OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

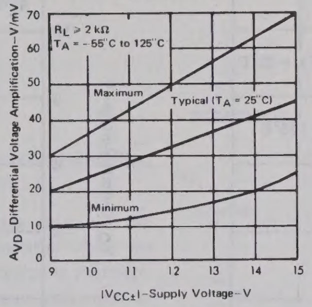


FIGURE 12

uA709C
OPEN-LOOP LARGE-SCALE
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

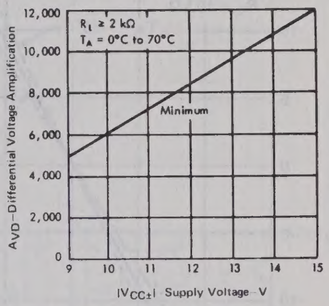


FIGURE 13

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

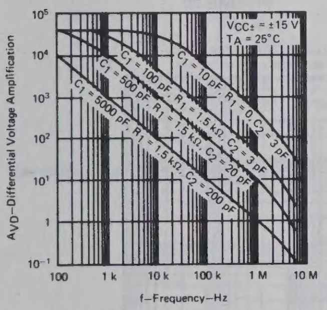


FIGURE 14

CLOSED-LOOP LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

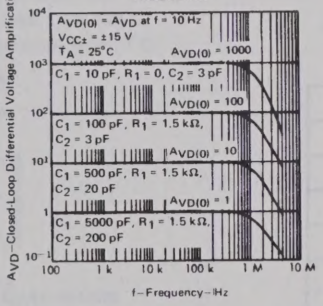
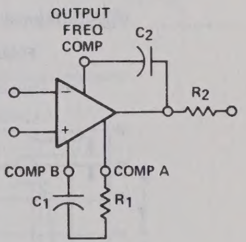


FIGURE 15



When the amplifier is operated with capacitive loading, $R_2 = 50\ \Omega$.

FREQUENCY COMPENSATION CIRCUIT FOR FIGURES 14, 15, AND 18

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

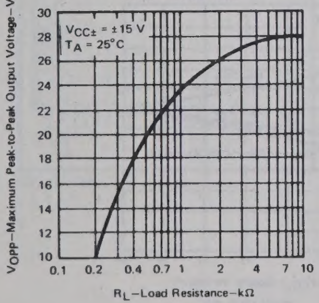


FIGURE 16

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

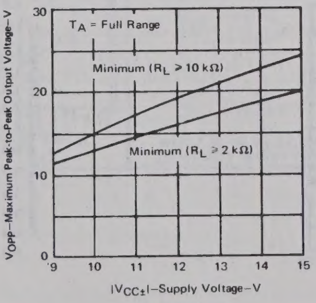


FIGURE 17

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

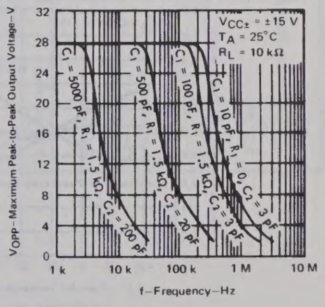


FIGURE 18

TYPICAL CHARACTERISTICS

uA709AM, uA709M
VOLTAGE TRANSFER
CHARACTERISTICS

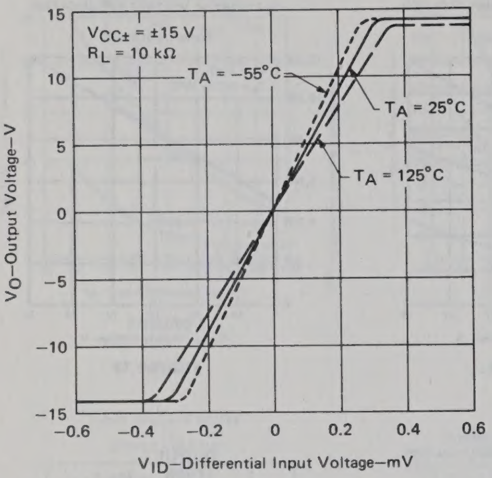


FIGURE 19

uA709C
VOLTAGE TRANSFER
CHARACTERISTICS

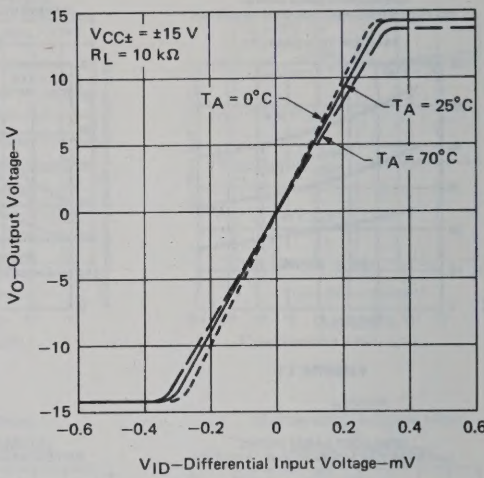


FIGURE 20

RELATIVE OUTPUT SWING
vs
ELAPSED TIME

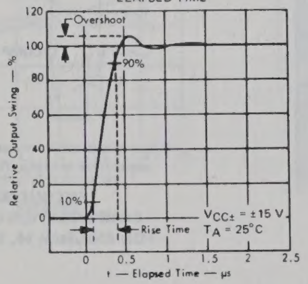


FIGURE 21

SLEW RATE
vs
CLOSED-LOOP DIFFERENTIAL
VOLTAGE AMPLIFICATION

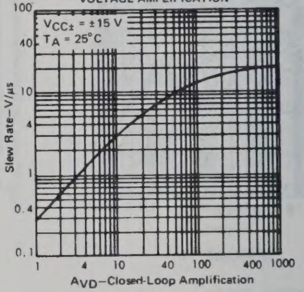


FIGURE 22

NORMALIZED FREQUENCY CHARACTERISTICS
vs
FREE-AIR TEMPERATURE

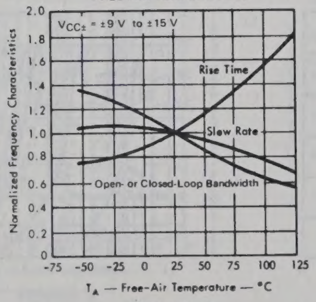


FIGURE 23

NORMALIZED FREQUENCY CHARACTERISTICS
vs
SUPPLY VOLTAGE

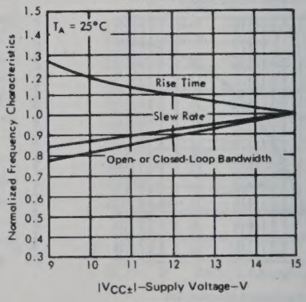


FIGURE 24

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TYPES uA741M, uA741C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611363, NOVEMBER 1970—REVISED JUNE 1976

FORMERLY SN52741, SN72741

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up

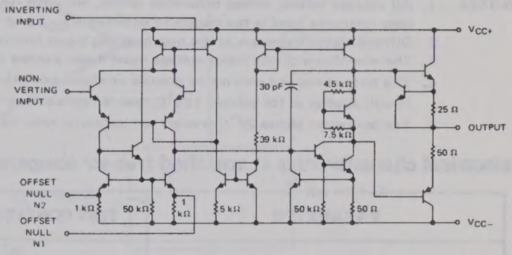
description

The uA741 is a general-purpose operational amplifier, featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA741M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA741C is characterized for operation from 0°C to 70°C.

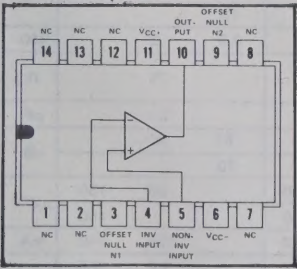
schematic


INVERTING INPUT
NON-VERTING INPUT
OFFSET NULL N2
OFFSET NULL N1
VCC+
OUTPUT
VCC−
30 pF
4.5 kΩ
7.5 kΩ
39 kΩ
25 Ω
50 Ω
1 kΩ
50 kΩ
1 kΩ
5 kΩ
50 kΩ
50 Ω

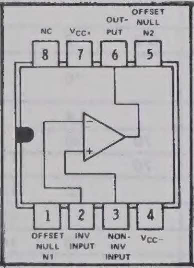
COMPONENT VALUES SHOWN ARE NOMINAL

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

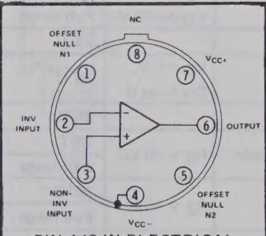

NC
NC
NC
VCC+
OUT-PUT
OFFSET NULL N2
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL N1
INV INPUT
NON-INV INPUT
VCC−
NC

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
VCC+
OUT-PUT
OFFSET NULL N2
8
7
6
5
1
2
3
4
OFFSET NULL N1
INV INPUT
NON-INV INPUT
VCC−

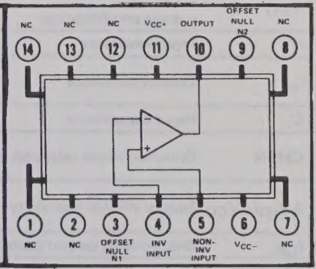
NC—No internal connection

L PLUG-IN PACKAGE (TOP VIEW)


NC
OFFSET NULL N1
VCC+
INV INPUT
OUTPUT
NON-INV INPUT
OFFSET NULL N2
VCC−
1
2
3
4
5
6
7
8

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)


NC
NC
NC
VCC+
OUTPUT
OFFSET NULL N2
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL N1
INV INPUT
NON-INV INPUT
VCC−
NC

TEXAS INSTRUMENTS
INCORPORATED
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TYPES uA741M, uA741C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741M	uA741C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		uA741M			uA741C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S ≤ 10 kΩ	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		R_L ≥ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		R_L ≥ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	50	200		20	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	R_S ≤ 10 kΩ	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

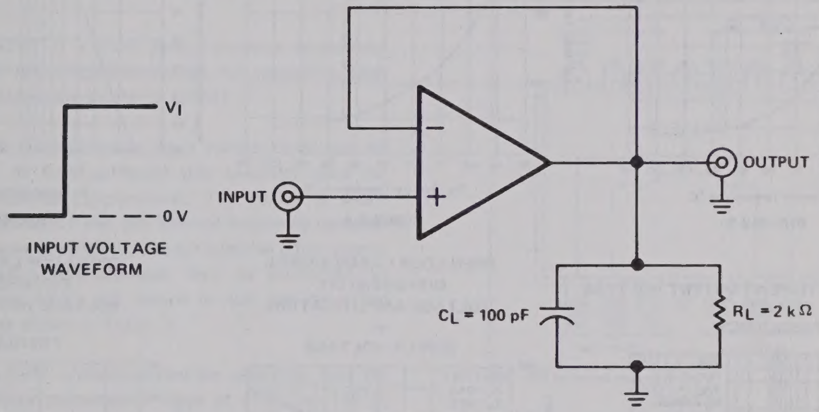
†All characteristics are specified under open-loop operation. Full range for uA741M is −55°C to 125°C and for uA741C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	uA741M			uA741C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.3			0.3		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION


V_I
0 V
INPUT VOLTAGE WAVEFORM
INPUT
−
+
OUTPUT
$C_L = 100$ pF
$R_L = 2$ kΩ

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

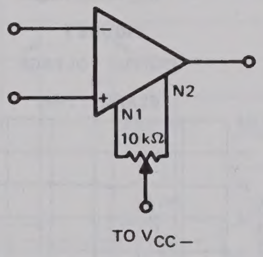

−
+
N2
N1
10 kΩ
TO V_{CC-}

FIGURE 2—INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPES uA741M, uA741C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

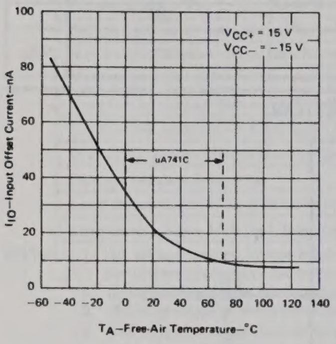
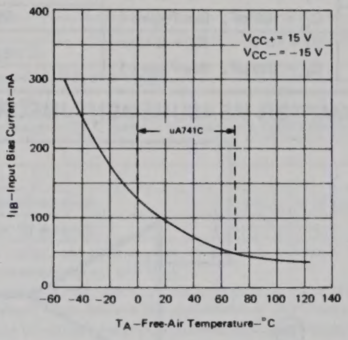


FIGURE 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE



FIGUER 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

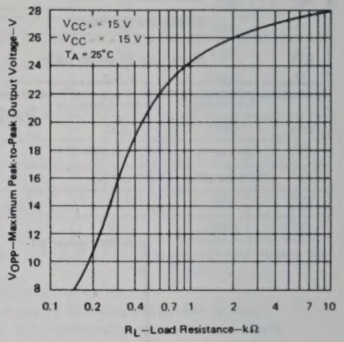


FIGURE 5

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

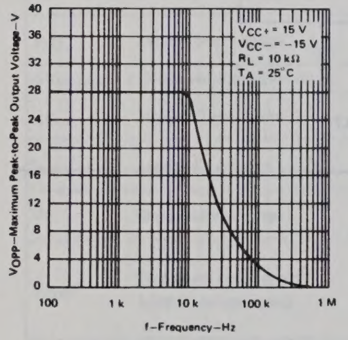


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

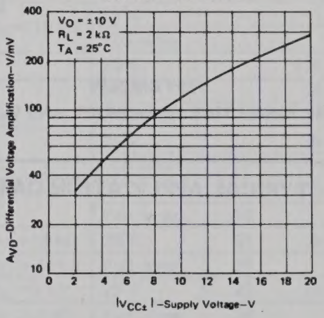


FIGURE 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

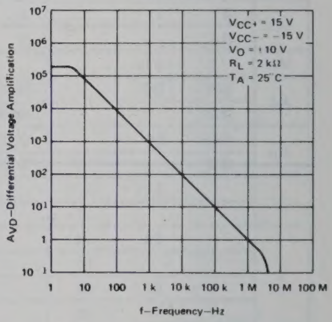


FIGURE 8

COMMON-MODE REJECTION RATIO vs FREQUENCY

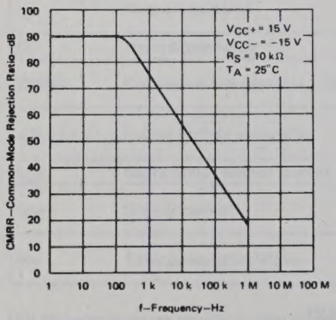


FIGURE 9

OUTPUT VOLTAGE vs ELAPSED TIME

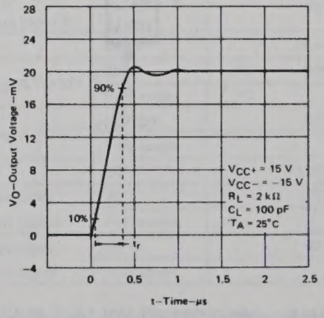


FIGURE 10

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

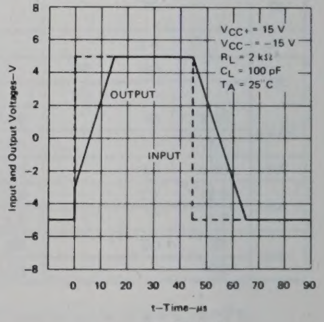


FIGURE 11

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TYPES uA747M, uA747C DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611446, FEBRUARY 1971—REVISED JUNE 1976

FORMERLY SN52747, SN72747

- No frequency Compensation Required
- Low Power Consumption
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- No Latch-up
- Designed to be Interchangeable with Fairchild μA747 and μA747C

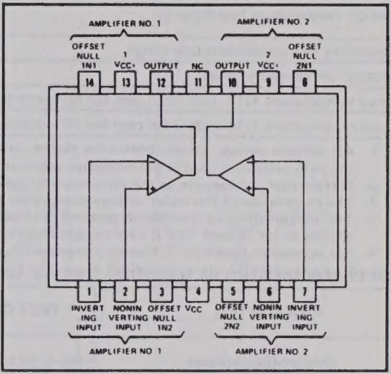
description

The uA747 is a dual general-purpose operational amplifier featuring offset-voltage null capability. Each half is electrically similar to uA741.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

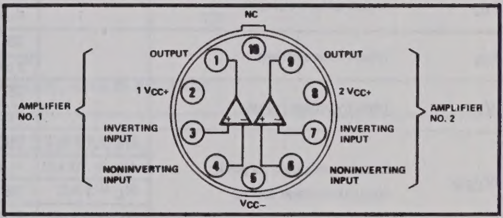
The uA747M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA747C is characterized for operation from 0°C to 70°C.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)


AMPLIFIER NO. 1
AMPLIFIER NO. 2
OFFSET NULL 1N1
1 VCC+
OUTPUT
NC
OUTPUT
2 VCC+
OFFSET NULL 2N1
14
13
12
11
10
9
8
1
2
3
4
5
6
7
INVERTING INPUT
NONINVERTING INPUT
OFFSET NULL 1N2
VCC
OFFSET NULL 2N2
NONINVERTING INPUT
INVERTING INPUT
AMPLIFIER NO 1
AMPLIFIER NO 2

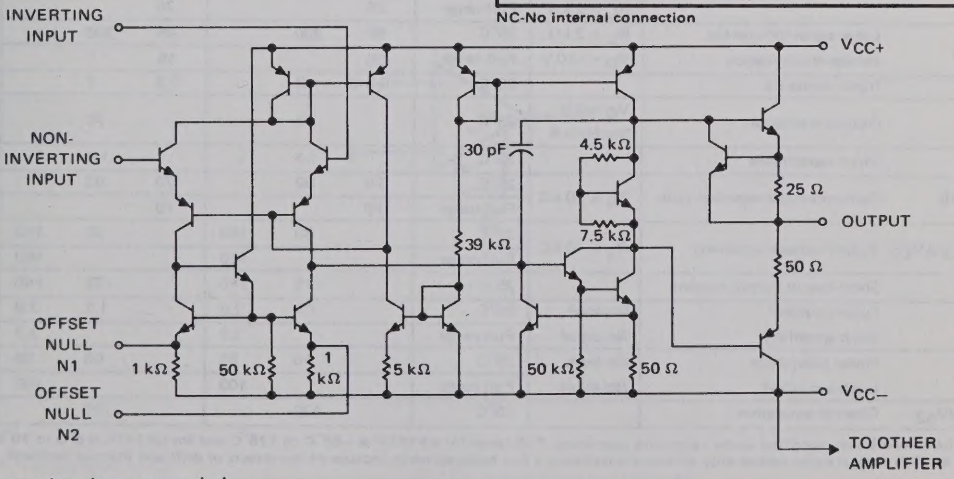
NC—No internal connection

L PLUG-IN
PACKAGE (TOP VIEW)


NC
OUTPUT
OUTPUT
1 VCC+
2 VCC+
AMPLIFIER NO. 1
AMPLIFIER NO. 2
INVERTING INPUT
INVERTING INPUT
NONINVERTING INPUT
NONINVERTING INPUT
VCC−
1
2
3
4
5
6
7
8
9
10

NC-No internal connection

schematic (each amplifier)


INVERTING INPUT
NON-INVERTING INPUT
OFFSET NULL N1
OFFSET NULL N2
1 kΩ
50 kΩ
1 kΩ
5 kΩ
39 kΩ
30 pF
4.5 kΩ
7.5 kΩ
50 kΩ
50 Ω
25 Ω
50 Ω
VCC+
OUTPUT
VCC−
TO OTHER AMPLIFIER

Component values shown are nominal.

TYPES uA747M, uA747C
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			uA747M	uA747C	UNIT
Supply voltage V_{CC+} (see Note 1)			22	18	V
Supply voltage V_{CC-} (see Note 1)			−22	−18	V
Differential input voltage (see Note 2)			±30	±30	V
Input voltage any input (see Notes 1 and 3)			±15	±15	V
Voltage between any offset null terminal (N1/N2) and V_{CC-}			±0.5	±0.5	V
Duration of output short-circuit (see Note 4)			unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	Each amplifier		500	500	mW
	Total package	J, N, or W package	800	800	
		L package	625	625	
Operating free-air temperature range			−55 to 125	0 to 70	°C
Storage temperature range			−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or W package		300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package		260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA747M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature and for total package ratings, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		uA747M			uA747C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	24	28		24	28		V
		$R_L \geq 10\ k\Omega$	Full range	24			24			
		$R_L = 2\ k\Omega$	25°C	20	26		20	26		
		$R_L \geq 2\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $V_O = \pm 10\ V$	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0\ V$, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (each amplifier)	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120		dB

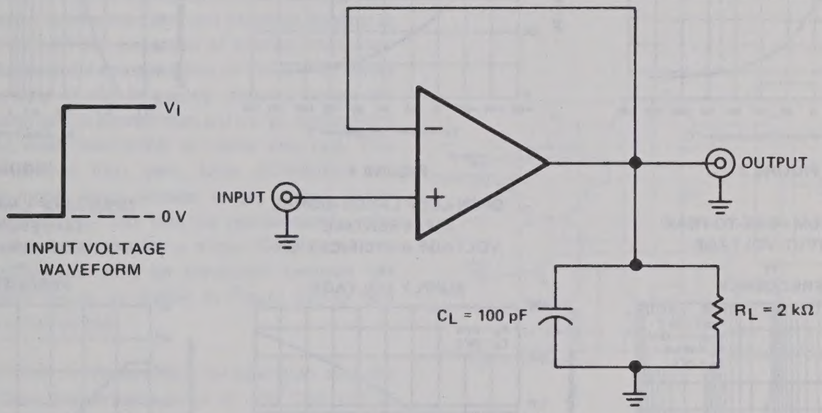
† All characteristics are specified under open-loop operation. Full range for uA747M is −55°C to 125°C and for uA747C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	uA747M			uA747C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.3			0.3		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION


V_I
0 V
INPUT VOLTAGE WAVEFORM
INPUT
OUTPUT
−
+
C_L = 100 pF
R_L = 2 kΩ

TEST CIRCUIT

FIGURE 1–RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

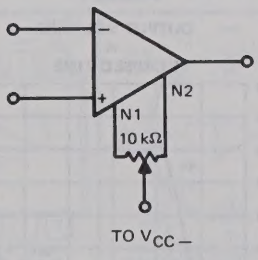

−
+
N2
N1
10 kΩ
TO V_{CC-}

FIGURE 2–INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

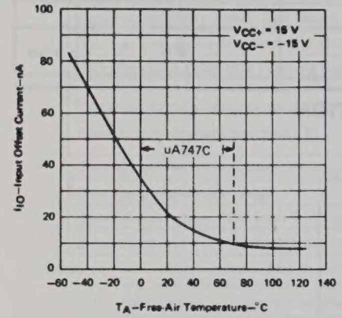


FIGURE 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

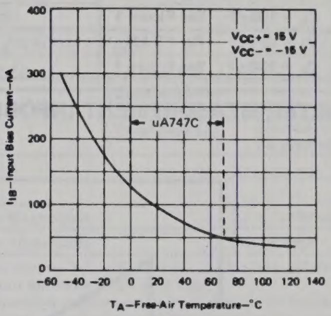


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

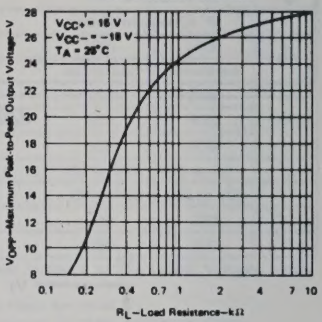


FIGURE 5

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

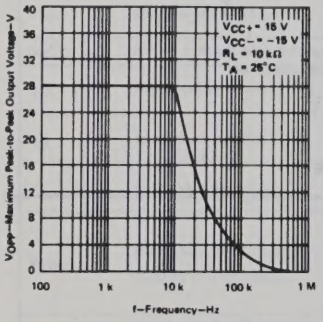


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

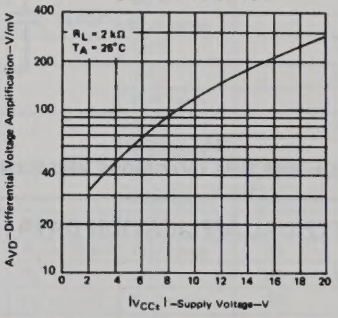


FIGURE 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

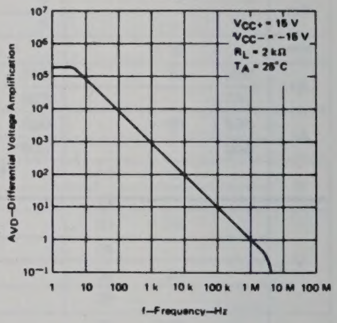


FIGURE 8

COMMON-MODE REJECTION RATIO vs FREQUENCY

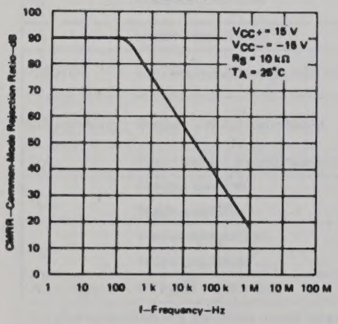


FIGURE 9

OUTPUT VOLTAGE vs ELAPSED TIME

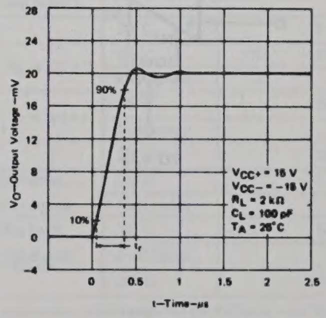


FIGURE 10

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

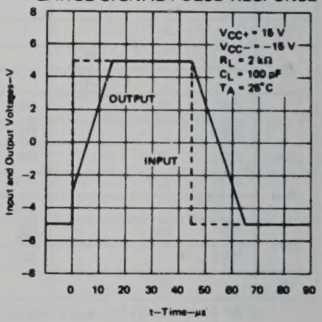


FIGURE 11

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

TYPES uA748M, uA748C GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7611418, DECEMBER 1970—REVISED JUNE 1976

FORMERLY SN52748, SN72748

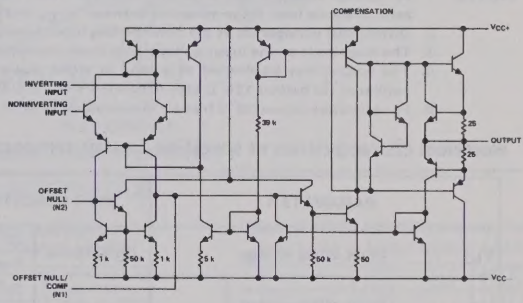
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-up
- Same Pin Assignments as uA709

description

The uA748 is a general-purpose operational amplifier. It offers the same advantages and desirable features as the uA741 with the exception of internal compensation. The external compensation of the uA748 allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. This circuit features high gain, large differential and common-mode input voltage range, output short-circuit protection, and may be compensated under unity-gain conditions with a single 30-pF capacitor. A potentiometer may be connected between the offset null inputs, as shown in Figure 12, to null out the offset voltage.

The uA748M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA748C is characterized for operation from 0°C to 70°C.

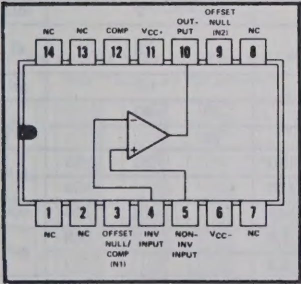
schematic


COMPENSATION
VCC+
INVERTING INPUT
NONINVERTING INPUT
39 k
25
OUTPUT
25
OFFSET NULL (N2)
1 k
50 k
1 k
5 k
50 k
50
OFFSET NULL/ COMP (N1)
VCC−

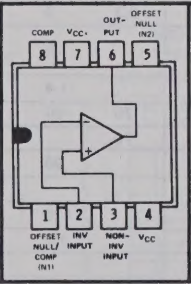
Resistor values shown are nominal and in ohms.

terminal assignments

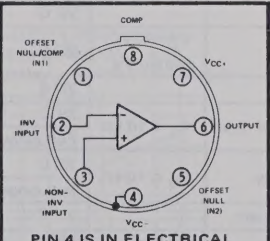
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
NC
COMP
VCC+
OUT-PUT
OFFSET NULL (N2)
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL/ COMP (N1)
INV INPUT
NON-INV INPUT
VCC−
NC

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

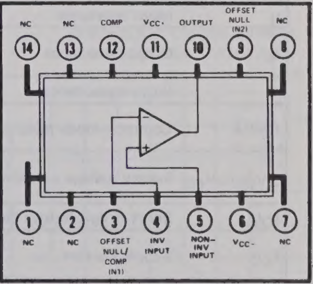

COMP
VCC+
OUT-PUT
OFFSET NULL (N2)
8
7
6
5
1
2
3
4
OFFSET NULL/ COMP (N1)
INV INPUT
NON-INV INPUT
VCC

L PLUG-IN PACKAGE (TOP VIEW)


COMP
OFFSET NULL/COMP (N1)
VCC+
INV INPUT
OUTPUT
NON-INV INPUT
OFFSET NULL (N2)
VCC−
1
2
3
4
5
6
7
8

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)


NC
NC
COMP
VCC+
OUTPUT
OFFSET NULL (N2)
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL/ COMP (N1)
INV INPUT
NON-INV INPUT
VCC−
NC

NC—No internal connection

TYPES uA748M, uA748C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA748M	uA748C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA748M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} =−15 V, C_C = 30 pF

PARAMETER		TEST CONDITIONS†		uA748M			uA748C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 10\ k\Omega$	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			1500			800	
V_I	Input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10\ k\Omega$	25°C	24	28		24	28		V
		$R_L \geq 10\ k\Omega$	Full range	24			24			
		$R_L = 2\ k\Omega$	25°C	20	26		20	26		
		$R_L \geq 2\ k\Omega$	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$, $V_O = \pm 10$ V	25°C	50	200		20	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0 V, See Note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	25°C	70	90		70	90		dB
			Full range	70			70			
$\Delta V_{IO}/\Delta V_{CC}$	Supply voltage sensitivity	$R_S \leq 10\ k\Omega$	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, No signal	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, No signal	25°C		50	85		50	85	mW
			Full range			100			100	

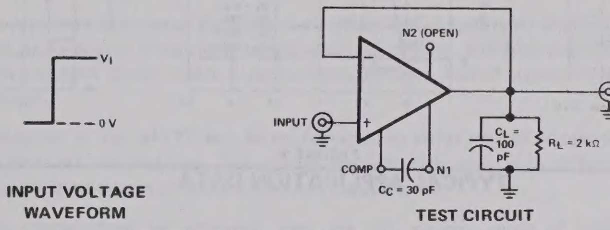
†All characteristics are specified under open-loop operation. Full range for uA748M is −55°C to 125°C and for uA748C is 0°C to 70°C.

NOTE 6: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	uA748M			uA748C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF, $C_C = 30$ pF, See Figure 1		0.3			0.3		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, $C_C = 30$ pF, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

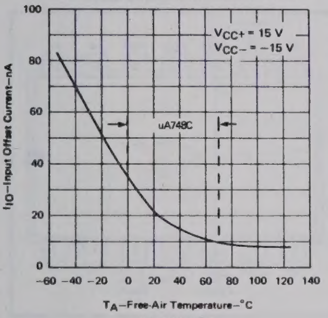


FIGURE 2

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

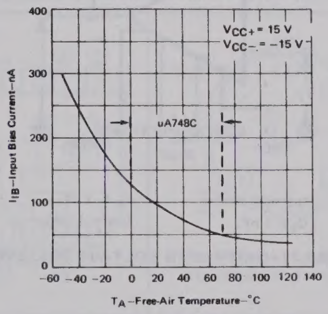


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

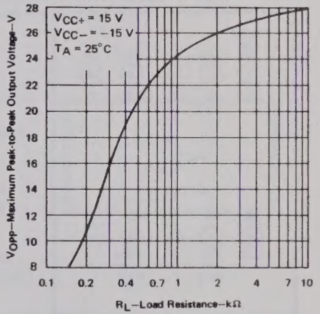


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

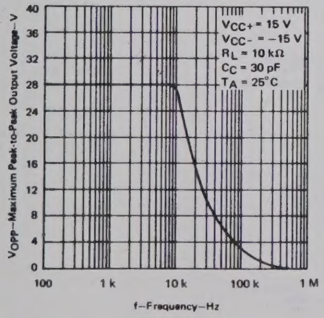


FIGURE 5

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

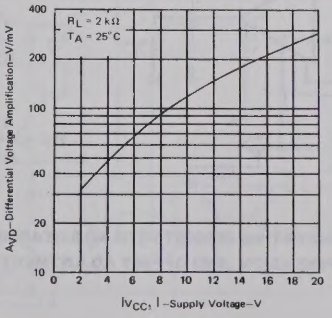


FIGURE 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

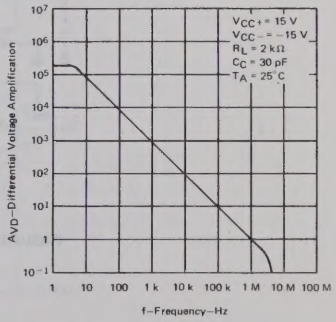


FIGURE 7

TYPES uA748M, uA748C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

TYPICAL CHARACTERISTICS

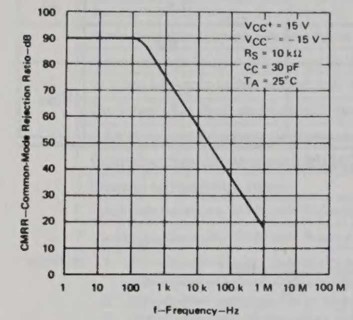

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

FIGURE 8

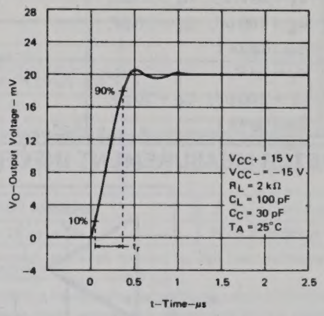

OUTPUT VOLTAGE
vs
ELAPSED TIME

FIGURE 9

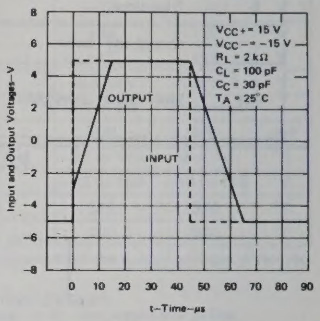
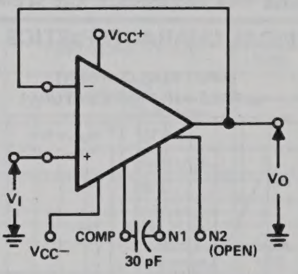

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

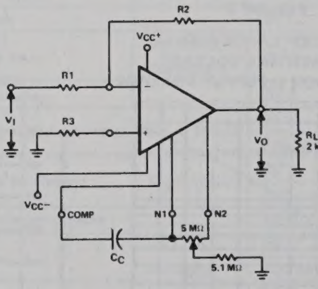
FIGURE 10

TYPICAL APPLICATION DATA



r_i = 400 MΩ, $r_o < 1\ \Omega$,
C_i = 1 pF, BW = 1 MHz

FIGURE 11—UNITY-GAIN VOLTAGE FOLLOWER



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geqslant \frac{R1 \cdot 30\ \text{pF}}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 12—INVERTING CIRCUIT WITH ADJUSTABLE GAIN, COMPENSATION, AND OFFSET ADJUSTMENT

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TYPES uA777M, uA777C
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 7612037, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52777, SN72777

- Low Input Currents
- Low Input Offset Parameters
- Frequency and Transient Response Characteristics Adjustable
- Short-Circuit Protection
- Offset-Voltage Null Capability
- No Latch-Up
- Wide Common-Mode and Differential Voltage Ranges
- Same Pin Assignments as uA748, uA709, LM101A/LM301A

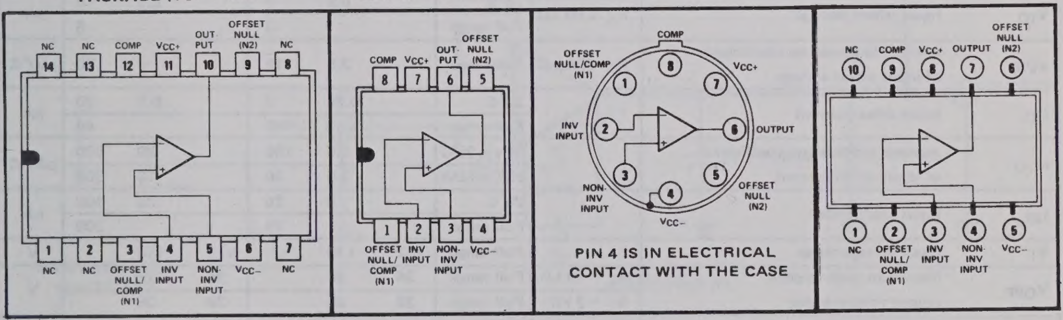
description

The uA777 is a precision operational amplifier. Low offset and bias currents improve system accuracy when used in applications such as long-term integrators, sample-and-hold circuits, and high-source-impedance summing amplifiers. This device is an excellent choice where a performance between that of super-beta and general purpose operational amplifiers is required.

External compensation of the uA777 may be implemented in either normal or feed-forward configuration to satisfy bandwidth and slew-rate requirements. This circuit features high gain, wide differential and common-mode input voltage range, output short-circuit protection, and null capability.

The uA777M is characterized for operation over the full military range of −55°C to 125°C; the uA777C is characterized for operation from 0°C to 70°C.

terminal assignments



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

L PLUG-IN PACKAGE (TOP VIEW)

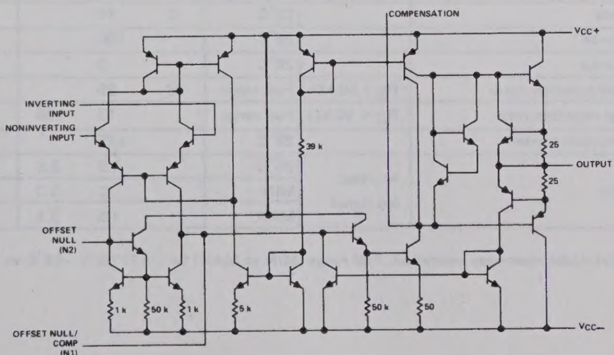
U FLAT PACKAGE (TOP VIEW)

NC
NC
COMP
VCC+
OUT PUT
OFFSET NULL (N2)
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
NC
OFFSET NULL/ COMP (N1)
INV INPUT
NON-INV INPUT
VCC−
NC
COMP
VCC+
OUT-PUT
OFFSET NULL (N2)
OFFSET NULL/ COMP (N1)
INV INPUT
NON-INV INPUT
VCC−
OFFSET NULL/COMP (N1)
INV INPUT
NON-INV INPUT
OUTPUT
OFFSET NULL (N2)
VCC−
OFFSET NULL (N2)
OUTPUT

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

schematic



COMPENSATION
VCC+
INVERTING INPUT
NONINVERTING INPUT
39 k
25
OUTPUT
25
OFFSET NULL (N2)
1 k
50 k
1 k
5 k
50 k
50
VCC−
OFFSET NULL/ COMP (N1)

Resistor values shown are nominal and in ohms.

TYPES uA777M, uA777C
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA777M	uA777C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the zero-reference level (ground) of the supply voltages where the zero-reference level is the midpoint between V_{CC+} and V_{CC-}. If the zero-reference level of the system is not the midpoint of the supply voltages, all voltage values must be changed accordingly.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA777M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $C_C = 30$ pF (unless otherwise noted)

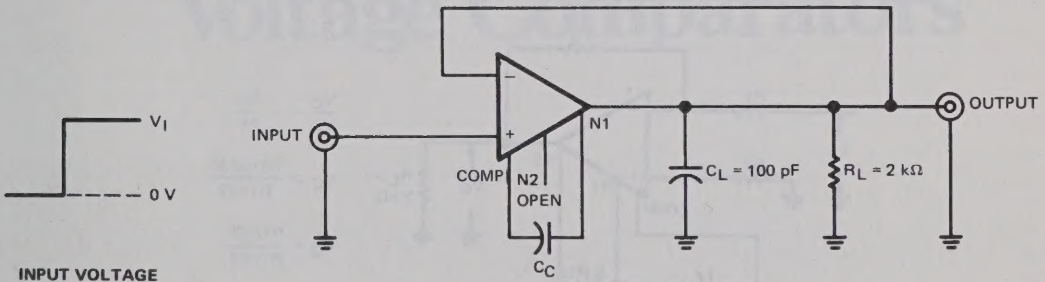
PARAMETER		TEST CONDITIONS†		uA777M			uA777C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leqslant 50$ kΩ	25°C		0.5	2		0.7	5	mV
			Full range			3			5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leqslant 50$ kΩ	Full range		2.5	15		4	30	µV/°C
I_{IO}	Input offset current		25°C		0.25	3		0.7	20	nA
			Full range			10			40	
α_{IIO}	Average temperature coefficient of input offset current		MIN to 25°C		6.5	150		20	600	pA/°C
			25°C to MAX		2.5	30		10	300	
I_{IB}	Input bias current		25°C		8	25		25	100	nA
			Full range			75			200	
V_I	Input voltage range		Full range	±12	±13		±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L = 10$ kΩ	Full range	24	28		24	28		V
		$R_L = 2$ kΩ	Full range	20	26		20	26		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L \geqslant 2$ kΩ	25°C	50	250		25	250		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	2	10		1	2		MΩ
r_o	Output resistance		25°C		100			100		Ω
C_i	Input capacitance		25°C		3			3		pF
CMRR	Common-mode rejection ratio	$R_S = 50$ kΩ	Full range	80	95		70	95		dB
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	$R_S \leqslant 50$ kΩ	Full range		13	100		15	150	µV/V
I_{OS}	Short-circuit output current		25°C		±25			±25		mA
I_{CC}	Supply current	No load, No signal	25°C		1.9	2.8		1.9	3.3	mA
			MIN		2	3.3			3.3	
			MAX		1.5	2.5			3.3	

† All characteristics are specified under open-loop operation. Full range (MIN to MAX) for uA777M is −55°C to 125°C and for uA777C is 0°C to 70°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		uA777M			uA777C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF	$A_V = 1$, $C_C = 30$ pF		0.3			0.3		μs
			$A_V = 10$, $C_C = 3.5$ pF		0.2			0.2		
	Overshoot factor	$V_I = 20$ mV, $R_L = 2$ kΩ, $C_L = 100$ pF	$A_V = 1$, $C_C = 30$ pF		5%			5%		
			$A_V = 10$, $C_C = 3.5$ pF		5%			5%		
SR	Slew rate	$R_L = 2$ kΩ, $C_L = 100$ pF	$A_V = 1$, $C_C = 30$ pF		0.5			0.5		V/μs
			$A_V = 10$, $C_C = 3.5$ pF		5.5			5.5		

PARAMETER MEASUREMENT INFORMATION



INPUT VOLTAGE WAVEFORM

TEST CIRCUIT

FIGURE 1—RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL CHARACTERISTICS

PULSE RESPONSE WITH
FEED-FORWARD COMPENSATION

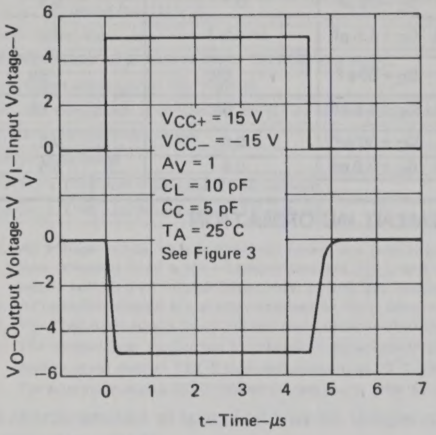


FIGURE 2

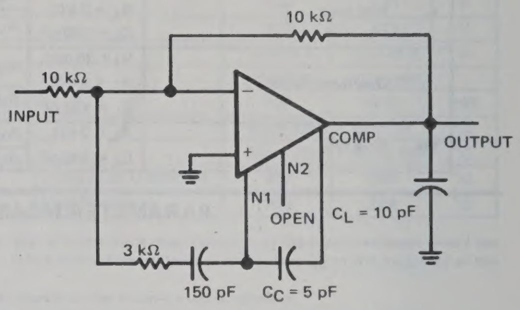
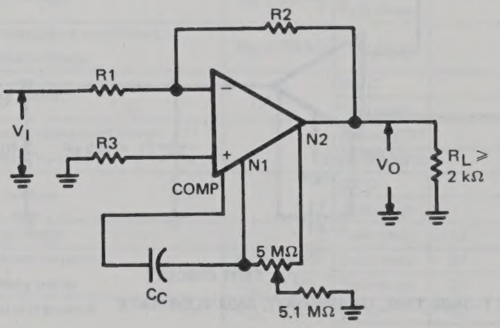

10 kΩ
10 kΩ
INPUT
COMP
OUTPUT
N2
N1
OPEN
C_L = 10 pF
3 kΩ
150 pF
C_C = 5 pF

FIGURE 3—INVERTING CIRCUIT WITH UNITY GAIN AND FEED-FORWARD COMPENSATION

TYPICAL APPLICATION DATA


R2
R1
V_I
R3
N2
N1
COMP
V_O
$R_L \geq$ 2 kΩ
5 MΩ
C_C
5.1 MΩ

$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\text{ pF}}{R1+R2}$$

$$R_3 = \frac{R1 \cdot R2}{R1+R2}$$

FIGURE 4—INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

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INCORPORATED
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Voltage Comparators

VOLTAGE COMPARATOR SELECTION GUIDE

DIFFERENTIAL COMPARATORS

−55°C to 125°C operating temperature range

	DEVICE TYPE	Input Offset Voltage MAX (mV)	Input Offset Current MAX (μA)	Input Bias Current MAX (μA)	Voltage Amplification MIN	Low-Level Output Current MIN (mA)	Response Time MAX (ns)	Power Supplies Required V_{CC+} NOM (V)	Power Supplies Required V_{CC-} NOM (V)	REMARKS
Single	TL710M	6	20	150	500	1.6	40 (Typ)	12	−6	
	uA710M	2	3	20	1250	2	40 (Typ)	12	−6	
	TL810M	3	7	25	10,000	0.5	80	12	−6	Improved TL710M
	LM106	3	7	45	40,000 (Typ)	16	40	12	−3 to −12	Strobe
	LM111†	4	0.02	0.15	200,000 (Typ)	8	140 (Typ)	15	−15	Strobe
	TL510M	3	7	25	10,000	0.5	80	12	−6	Strobe
Dual	LM193	5	0.025	−0.1	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V
	TL820M	3	7	25	10,000	0.5	80	12	−6	Dual TL810M
	TL506M	3	7	45	40,000 (Typ)	16	40	12	−3 to −12	Dual LM106
	TL514M	3	7	25	10,000	0.5	80	12	−6	Dual TL510M
Dual Channel	uA711M	6	20	150	500	0.5	80	12	−6	Strobes
	TL811M	6	5	30	8,000	0.5	80	12	−6	Improved uA711M
Quad	LM139	5	0.025	−0.1	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V

†Capable of operating with a single 5-volt supply.

−40°C to 85°C operating temperature range

	DEVICE TYPE	Input Offset Voltage MAX (mV)	Input Offset Current MAX (μA)	Input Bias Current MAX (μA)	Voltage Amplification MIN	Low-Level Output Current MIN (mA)	Response Time MAX (ns)	Power Supplies Required V_{CC+} NOM (V)	Power Supplies Required V_{CC-} NOM (V)	REMARKS
Dual	LM2903	7	0.05	−0.25	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V
Quad	LM2901	7	0.05	−0.25	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V

VOLTAGE COMPARATOR SELECTION GUIDE

DIFFERENTIAL COMPARATORS

−25°C to 85°C operating temperature range

	DEVICE TYPE	Input Offset Voltage MAX (mV)	Input Offset Current MAX (μA)	Input Bias Current MAX (μA)	Voltage Amplification MIN	Low-Level Output Current MIN (mA)	Response Time MAX (ns)	Power Supplies Required V_{CC+} NOM (V)	Power Supplies Required V_{CC-} NOM (V)	REMARKS
Single	LM206	3	7	45	40,000 (Typ)	16	40	12	−3 to −12	Strobe
Dual	LM293	5	0.05	−0.25	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V
Quad	LM239	5	0.05	−0.25	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V

0°C to 70°C operating temperature range

	DEVICE TYPE	Input Offset Voltage MAX (mV)	Input Offset Current MAX (μA)	Input Bias Current MAX (μA)	Voltage Amplification MIN	Low-Level Output Current MIN (mA)	Response Time MAX (ns)	Power Supplies Required V_{CC+} NOM (V)	Power Supplies Required V_{CC-} NOM (V)	REMARKS
Single	TL710C	10	25	150	500		40	12	−6	
	TL810C	4.5	7.5	30	8,000	0.5	80	12	−6	Improved TL710C
	LM306	6.5	7.5	40	40,000 (Typ)	16	28 (Typ)	12	−3 to −12	Strobe
	LM311†	10	0.07	0.3	200,000 (Typ)	8	165 (Typ)	15	−15	Strobe
	TL510C	4.5	7.5	30	8,000	0.5	80	12	−6	Strobe
Dual	LM393	5	0.05	−0.25	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V
	TL720C	10	25	150	500		40 (Typ)	12	−6	Dual TL710C
	TL820C	4.5	7.5	30	8,000	0.5	80	12	−6	Dual TL810C
	TL506C	6.5	7.5	40	40,000 (Typ)	16	28 (Typ)	12	−3 to −12	Dual LM306
	TL514C	4.5	7.5	30	8,000	0.5	80	12	−6	Dual TL510C
Dual Channel	uA711C	10	25	150	500	0.5	40 (Typ)	12	−6	Strobe
	TL811C	10	10	50	5,000	0.5	33 (Typ)	12	−6	Improved uA711C
Quad	LM339	5	0.05	−0.25	200,000 (Typ)	6	1300 (Typ)	5	0	V_{CC} range 2 V to 36 V

†Capable of operating with a single 5-volt supply.

GLOSSARY
DIFFERENTIAL COMPARATOR TERMS, DEFINITIONS, AND SYMBOLS

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to the specified level.
NOTE: The input offset voltage may also be defined for the case where two equal resistances (R_S) are inserted in series with the input leads.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left| \frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right| \quad \text{where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left| \frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}} \right| \quad \text{where } T_{A(1)} \text{ and } T_{A(2)} \text{ are the specified temperature extremes.}$$

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Current ($I_{IH(S)}$)

The current flowing into or out of* the strobe at a high-level voltage.

Low-Level Strobe Current ($I_{IL(S)}$)

The current flowing out of* the strobe at a low-level voltage.

High-Level Strobe Voltage ($V_{IH(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed not to interfere with the operation of the comparator.

Low-Level Strobe Voltage ($V_{IL(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.

Input Voltage Range (V_I)

The range of voltage that if exceeded at either input terminal will cause the comparator to cease functioning properly.

---

*Current out of a terminal is given as a negative value.

GLOSSARY
DIFFERENTIAL COMPARATOR TERMS, DEFINITIONS, AND SYMBOLS

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the comparator to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Differential Input Voltage Range (V_{ID})

The range of voltage between the two input terminals that if exceeded will cause the comparator to cease functioning properly.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output voltage to the change in differential input voltage producing it with the common-mode input voltage held constant.

High-Level Output Voltage (V_{OH})

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Voltage (V_{OL})

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

High-Level Output Current, (I_{OH})

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Current, (I_{OL})

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Output Resistance (r_o)

The resistance between an output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

---

*Current out of a terminal is given as a negative value.

GLOSSARY
DIFFERENTIAL COMPARATOR TERMS, DEFINITIONS, AND SYMBOLS

Supply Current (I_{CC+}, I_{CC-})

The current into* the V_{CC+} or V_{CC-} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Response Time

The interval between the application of an input step function and the time when the output crosses the logic threshold voltage.
NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time

The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

5

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*Current out of a terminal is given as a negative value.

LINEAR INTEGRATED CIRCUITS

TYPES LM106, LM206, LM306 DIFFERENTIAL COMPARATORS WITH STROBES

BULLETIN NO. DL-S 7611586, JANUARY 1972–REVISED JUNE 1976

FORMERLY SN52106, SN72306

- Fast Response Times
- Improved Gain and Accuracy
- Fan-Out to 10 Series 54/74 TTL Loads
- Strobe Capability
- Short-Circuit and Surge Protection
- Designed to be interchangeable with National Semiconductor LM106, LM206, and LM306

description

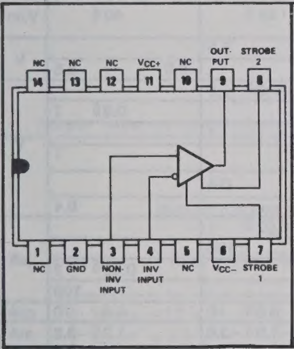
The LM106, LM206, and LM306 are high-speed voltage comparators with differential inputs, a low-impedance output with high-sink-current capability (100 mA), and two strobe inputs. These devices detect low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

The circuit is similar to a TL810 with gated output. A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between −3 V and −12 V with little difference in performance.

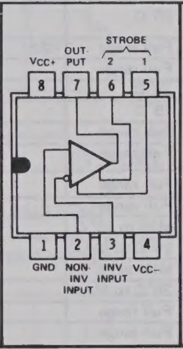
The LM106 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM206 is characterized for operation from −25°C to 85°C, and the LM306 from 0°C to 70°C.

terminal assignments

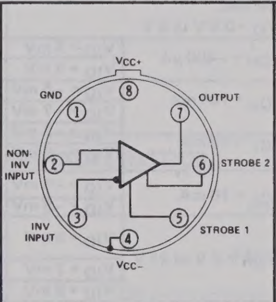
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

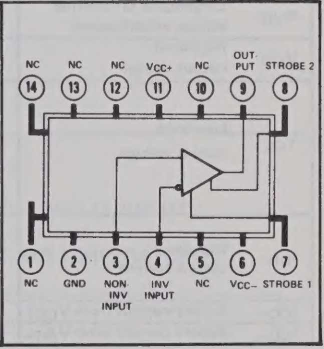


L PLUG-IN PACKAGE (TOP VIEW)



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Notes 1 and 3)	±7 V
Strobe voltage range (see Note 1)	0 V to V_{CC+}
Output voltage (see Note 1)	24 V
Voltage from output to V_{CC-}	30 V
Duration of output short-circuit (see Note 4)	10 s
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)	600 mW
Operating free-air temperature range: LM106 Circuits	−55°C to 125°C
LM206 Circuits	−25°C to 85°C
LM306 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, JG, L or U package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES:
1. All voltage values, except differential voltages and the voltage from the output to V_{CC-}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 25°C free-air temperature, refer to Dissipation Curves, Section 2.

TYPES LM106, LM206, LM306
DIFFERENTIAL COMPARATORS WITH STROBES

---

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −3 V to −12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM106, LM206			LM306			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$,	See Note 6	25°C		0.5§	2		1.6§	5	mV
				Full range			3			6.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$,	See Note 6	Full range		3	10		5	20	µV/°C
I_{IO}	Input offset current		See Note 6	25°C		0.7§	3		1.8§	5	µA
				MIN		2	7		1	7.5	
				MAX		0.4	3		0.5	5	
α_{IIO}	Average temperature coefficient of input offset current		See Note 6	MIN to 25°C		15	75		24	100	nA/°C
				25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	V_O = 0.5 V to 5 V		MIN to 25°C			45			40	µA
				25°C to MAX		7§	20		16§	25	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)}$ = 0.4 V		Full range		−1.7§	−3.2		−1.7§	−3.2	mA
$V_{IH(S)}$	High level strobe voltage			Full range	2.2			2.2			V
$V_{IL(S)}$	Low-level strobe voltage			Full range			0.9			0.9	V
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V to −12 V		Full range	±5			±5			V
V_{ID}	Differential input voltage range			Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0.5 V to 5 V		25°C		40 §			40 §		V/mV
V_{OH}	High-level output voltage	I_{OH} = −400 µA	V_{ID} = 5 mV	Full range	2.5		5.5				V
			V_{ID} = 8 mV	Full range				2.5		5.5	
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	V_{ID} = −5 mV	25°C		0.8§	1.5				V
			V_{ID} = −7 mV	25°C					0.8§	2	
		I_{OL} = 50 mA	V_{ID} = −5 mV	Full range			1				
			V_{ID} = −8 mV	Full range						1	
		I_{OL} = 16 mA	V_{ID} = −5 mV	Full range			0.4				
			V_{ID} = −8 mV	Full range						0.4	
I_{OH}	High-level output current	V_{OH} = 8 V to 24 V	V_{ID} = 5 mV	MIN to 25°C		0.02§	1				µA
				25°C to MAX			100				
			V_{ID} = 7 mV	MIN to 25°C					0.02§	2	
			V_{ID} = 8 mV	25°C to MAX						100	
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 mV, No load		Full range		6.6§	10		6.6	10	mA
I_{CC-}	Supply current from V_{CC-}	No load		Full range		−1.9§	−3.6		−1.9§	−3.6	mA

†Unless otherwise noted, all characteristics are measured with the strobe open.

§These typical values are at V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C. Full range (MIN to MAX) for LM106 is −55°C to 125°C; for LM206 is −25°C to 85°C; and for LM306 is 0°C to 70°C.

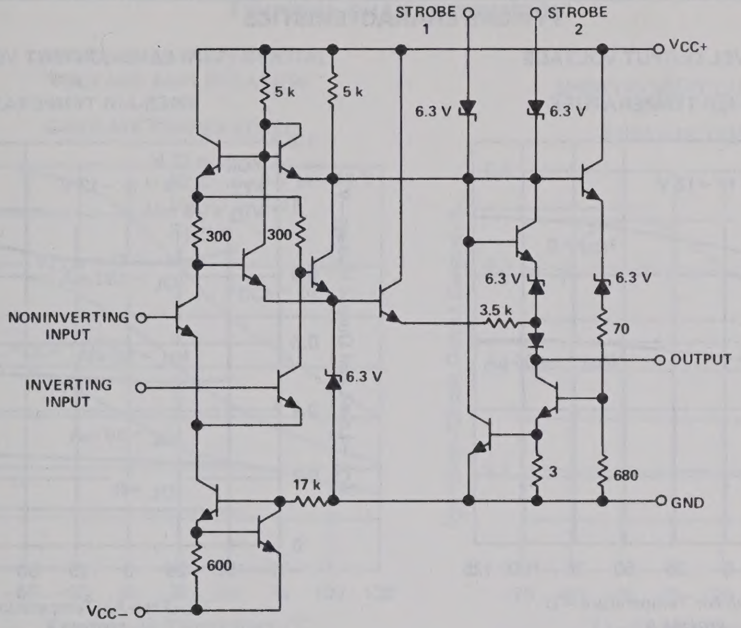
NOTE 6: The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS†	LM106, LM206			LM306			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time, low-to-high-level output	R_L = 390 Ω to 5 V, C_L = 15 pF, See Note 7		28	40		28		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive. The typical value is specified for a nominal threshold voltage of 1.4 V.

schematic


STROBE 1
STROBE 2
VCC+
5 k
5 k
6.3 V
6.3 V
300
300
6.3 V
6.3 V
3.5 k
70
NONINVERTING INPUT
INVERTING INPUT
6.3 V
OUTPUT
3
680
17 k
GND
600
VCC−

Resistor values are nominal in ohms.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

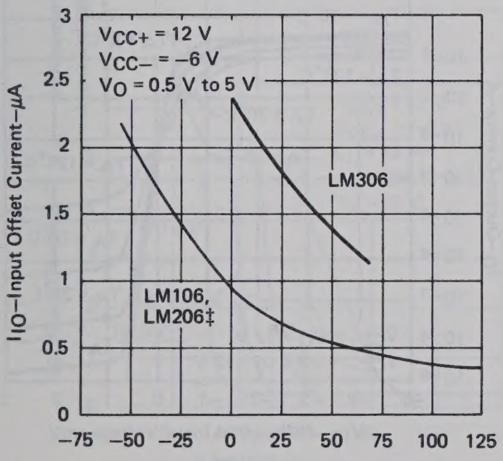


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

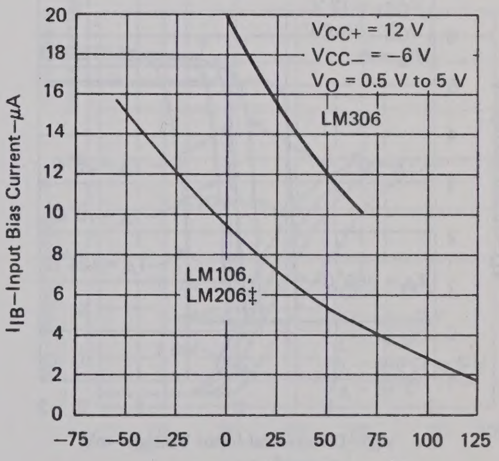


FIGURE 2

---

‡Data for free-air temperatures below −25°C and above 85°C is applicable for LM106 only.

TYPICAL CHARACTERISTICS‡

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

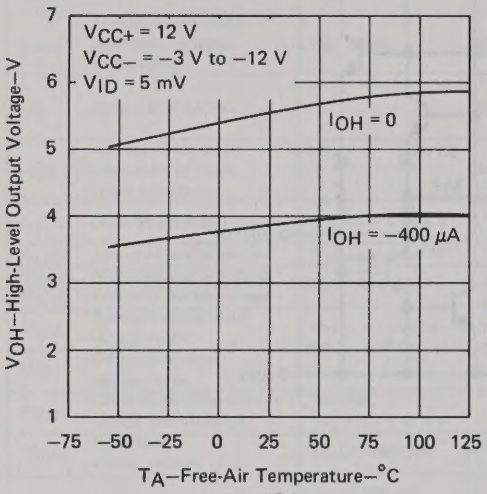


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

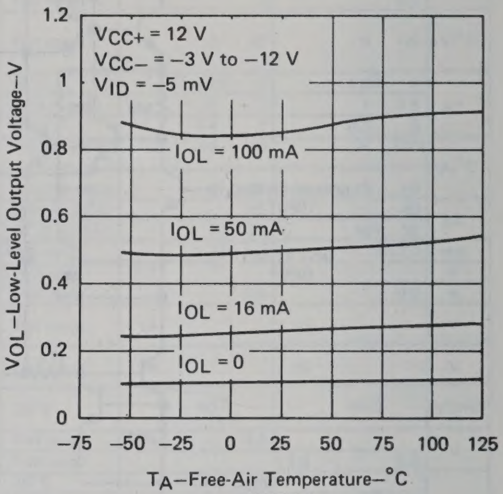


FIGURE 4

VOLTAGE TRANSFER CHARACTERISTICS

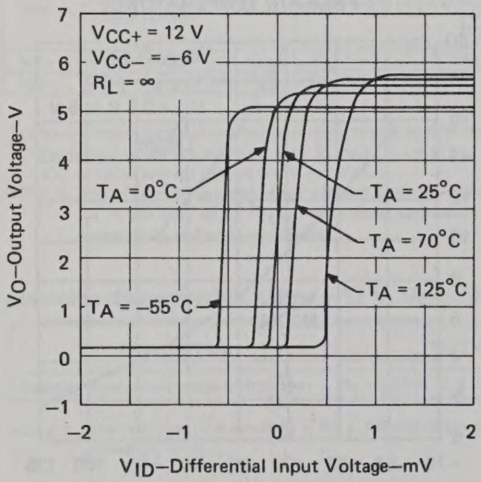


FIGURE 5

OUTPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

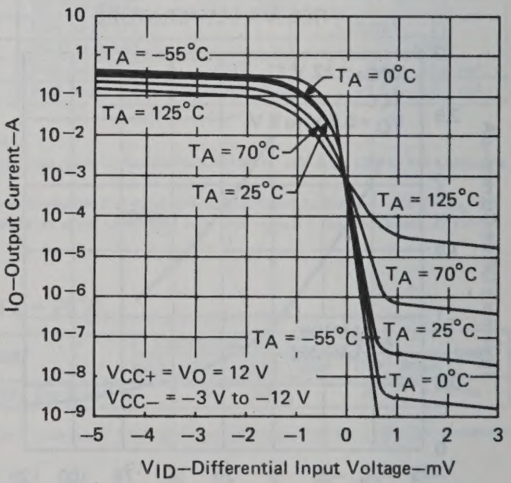


FIGURE 6

---

‡Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable for those types.

TYPICAL CHARACTERISTICS‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

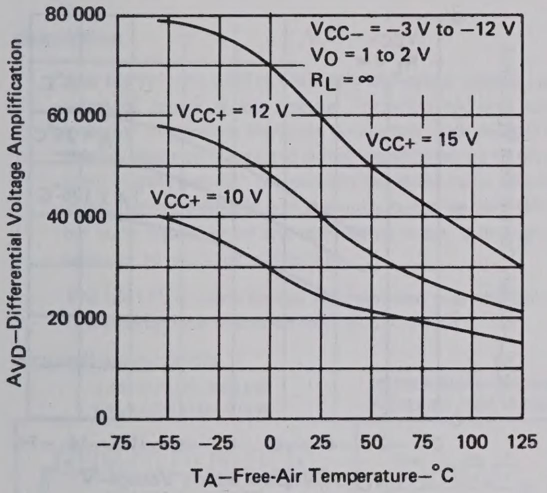


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

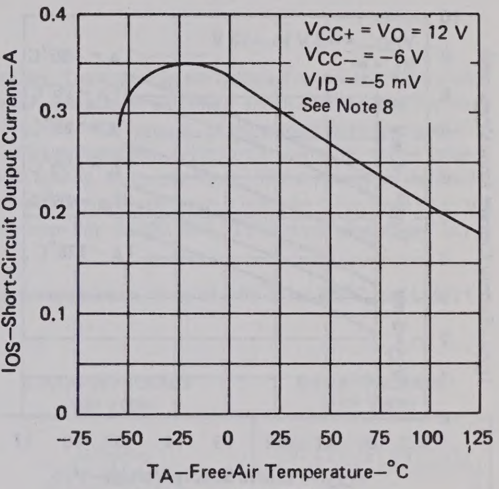


FIGURE 8

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

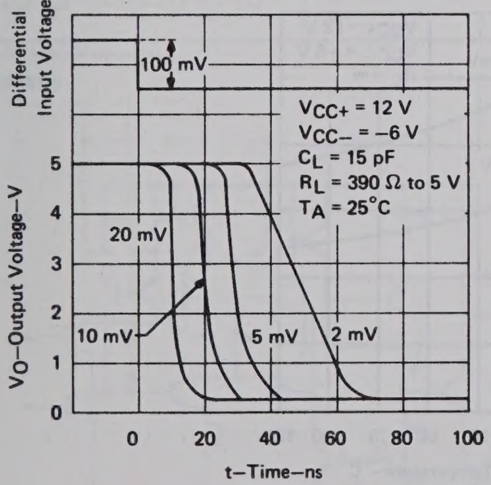


FIGURE 9

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

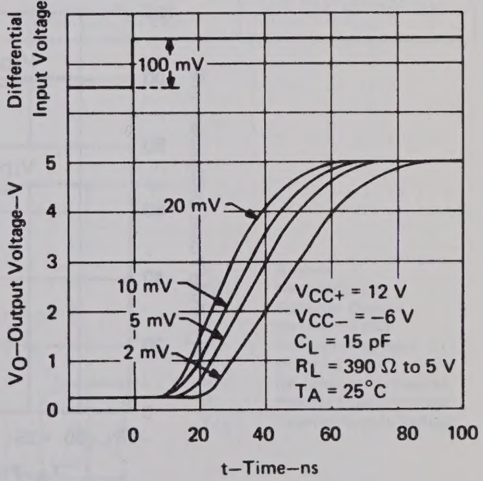


FIGURE 10

---

‡Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable for those types.

NOTE 8: This parameter was measured using a single 5-ms pulse.

TYPICAL CHARACTERISTICS‡

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

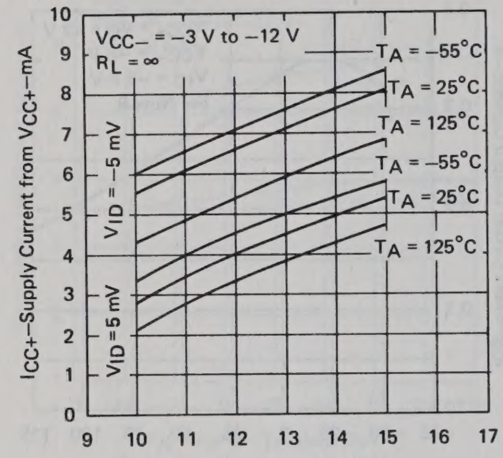


FIGURE 11

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

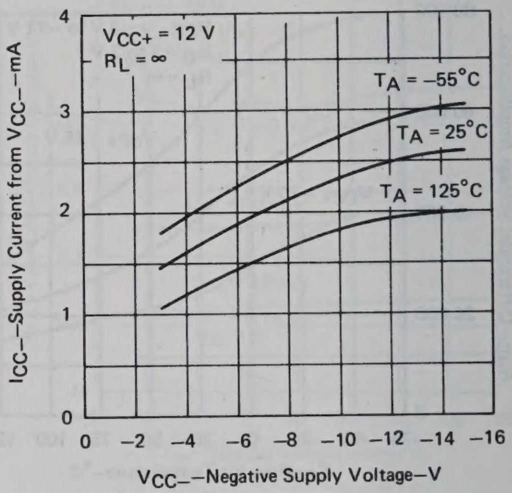


FIGURE 12

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

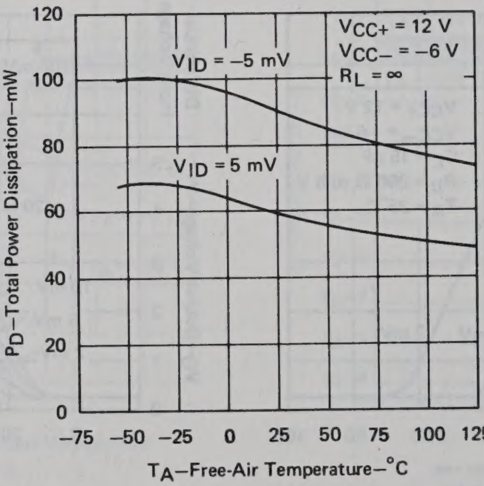


FIGURE 13

---

‡Data for free-air temperature outside the range specified in the absolute maximum ratings for LM206 or LM306 is not applicable for those types.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

LINEAR
INTEGRATED CIRCUITS

TYPES LM111, LM311
DIFFERENTIAL COMPARATORS WITH STROBE

BULLETIN NO. DL-S 7611797, SEPTEMBER 1973—REVISED JULY 1976

FORMERLY SN52111, SN72311

- Fast Response Times
- Strobe Capability
- Designed to be Interchangeable with National Semiconductor LM111 and LM311
- Maximum Input Bias Current . . . 300 nA
- Maximum Input Offset Current . . . 70 nA
- Can Operate From Single 5-V Supply

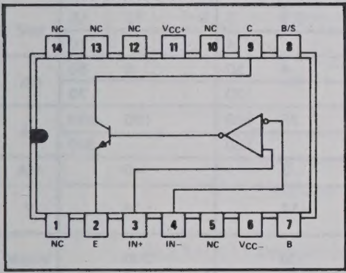
description

The LM111 and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltage, including ±15-volt supplies for operational amplifiers and 5-volt supplies for logic systems. The output levels are compatible with most DTL, TTL, and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 volts at 50 milliamperes. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+}, or V_{CC-}. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the probe input is low, the output will be in the off state regardless of the differential input. Although slower than the TL506 and TL514, these devices are not as sensitive to spurious oscillations.

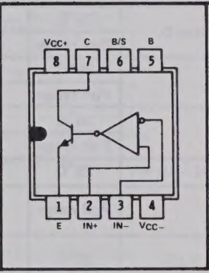
The LM111 is characterized for operation over the full military temperature range of −55°C to 125°C; the LM311 is characterized for operation from 0°C to 70°C.

terminal assignments

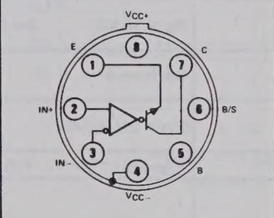
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)


NC 14
NC 13
NC 12
VCC+ 11
NC 10
C 9
B/S 8
1 NC
2 E
3 IN+
4 IN−
5 NC
6 VCC−
7 B

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

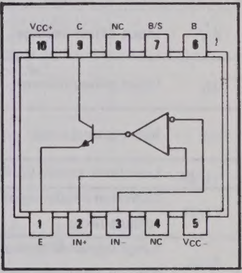

VCC+ 8
C 7
B/S 6
B 5
1 E
2 IN+
3 IN−
4 VCC−

L PLUG-IN PACKAGE (TOP VIEW)


VCC+ 8
E 1
C 7
IN+ 2
B/S 6
IN− 3
B 5
VCC− 4

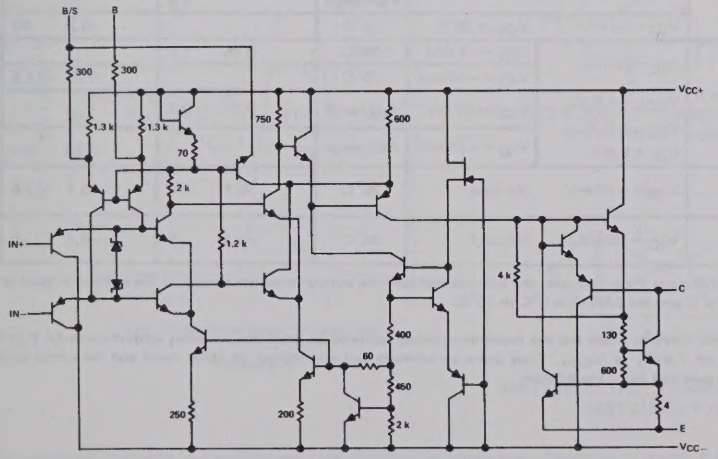
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE (TOP VIEW)


VCC+ 10
C 9
NC 8
B/S 7
B 6
1 E
2 IN+
3 IN−
4 NC
5 VCC−

NC—No internal connection

schematic


B/S
B
300
300
1.3 k
1.3 k
70
750
600
VCC+
2 k
1.2 k
IN+
IN−
4 k
C
400
60
450
2 k
130
600
4
250
200
E
VCC−

B	Balance
B/S	Balance/Strobe
C	Collector Output
E	Emitter Output
IN+	Noninverting Input
IN−	Inverting Input
NC	No Internal Connection
V_{CC+}	Positive Supply Voltage
V_{CC-}	Negative Supply Voltage

Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM111	LM311	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	V
Voltage from emitter output to V_{CC-}		30	30	V
Voltage from collector output to V_{CC-}		50	40	V
Duration of output short-circuit (see Note 4)		10	10	s
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	J, JG, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 60 seconds	N or P package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero-reference level (ground) of the supply voltages where the zero-reference level is at the midpoint between V_{CC+} and V_{CC-}. If the zero-reference level of the system is not the midpoint of the supply voltages, all voltage values must be adjusted accordingly.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 V, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM111			LM311			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$R_S \leq 50$ kΩ,	See Note 6	25°C		0.7	3		2	7.5	mV
				Full range			4			10	
I_{IO}	Input offset current	See Note 6		25°C		4	10		6	50	nA
				Full range			20			70	
I_{IB}	Input bias current	$V_O = 1$ V to 14 V		25°C		75	100		100	250	nA
				Full range			150			300	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)} = 0.3$ V,	$V_{ID} \leq -10$ mV	25°C		−3			−3		mA
V_{ICR}	Common-mode input voltage range			Full range		±14			±14		V
A_{VD}	Large-signal differential voltage amplification	$V_O = 5$ V to 35 V,	$R_L = 1$ kΩ	25°C		200			200		V/mV
I_{OH}	High-level (collector) output current	$V_{ID} = 5$ mV,	$V_{OH} = 35$ V	25°C		0.2	10				nA
				Full range			0.5				μA
		$V_{ID} = 10$ mV	$V_{OH} = 35$ V	25°C					0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	$I_{OL} = 50$ mA	$V_{ID} = -5$ mV	25°C		0.75	1.5				V
			$V_{ID} = -10$ mV	25°C					0.75	1.5	
		$V_{CC+} = 4.5$ V, $V_{CC-} = 0$ V, $I_{OL} = 8$ mA	$V_{ID} = -6$ mV	Full range		0.23	0.4				
			$V_{ID} = -10$ mV	Full range					0.23	0.4	
I_{CC+}	Supply current from V_{CC+}, output low	$V_{ID} = -10$ mV,	No load	25°C		5.1	6		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output high	$V_{ID} = 10$ mV,	No load	25°C		−4.1	−5		−4.1	−5	mA

†Unless otherwise noted, all characteristics are measured with the balance and balance/strobe terminals open and the emitter output grounded. Full range for LM111 is −55°C to 125°C and for LM311 is 0°C to 70°C.

‡All typical values are at $T_A = 25$°C.

NOTE 6: The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pull-up resistor of 7.5 kΩ to V_{CC+}. Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

switching characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	$R_C = 500\ \Omega$ to 5 V, $C_L = 5$ pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive. The typical values are specified for a nominal threshold voltage of 1.4 V.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

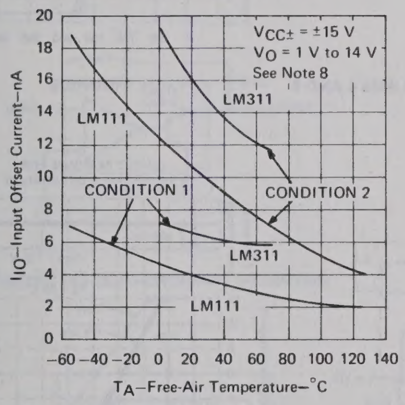


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

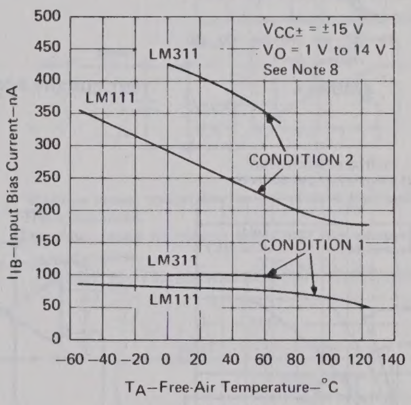


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS

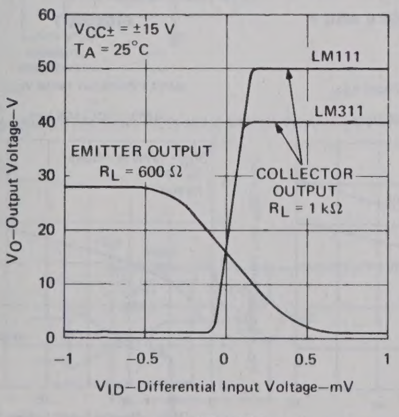
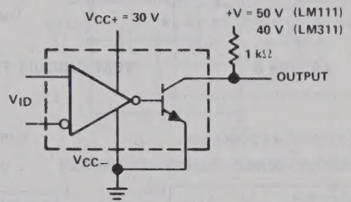
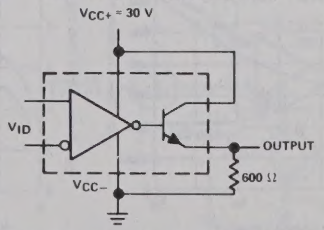


FIGURE 3



COLLECTOR OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3



EMITTER OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3

NOTE 8: Condition 1 is with the balance and balance/strobe terminals open. Condition 2 is with the balance and balance/strobe terminals connected to V_{CC+}.

TYPICAL CHARACTERISTICS

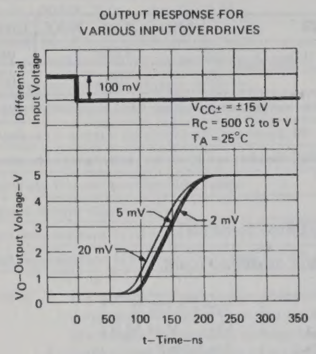
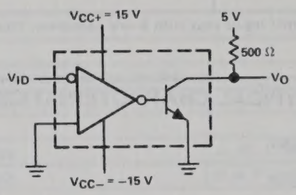

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

FIGURE 4



TEST CIRCUIT FOR FIGURES 4 AND 5

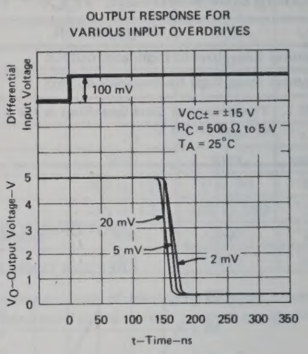

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

FIGURE 5

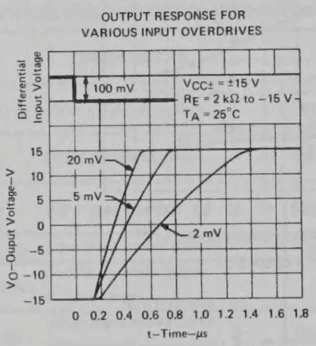
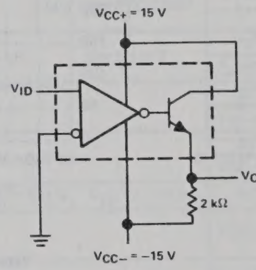

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

FIGURE 6



TEST CIRCUIT FOR FIGURES 6 AND 7

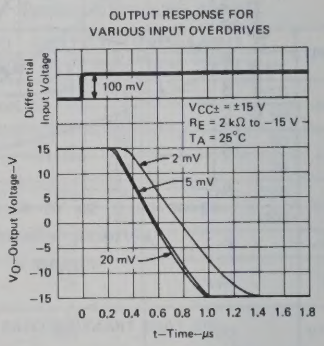

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

FIGURE 7

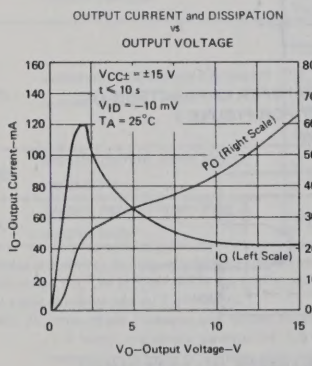

OUTPUT CURRENT and DISSIPATION vs OUTPUT VOLTAGE

FIGURE 8

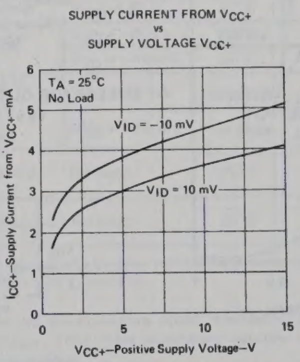

SUPPLY CURRENT FROM VCC+ vs SUPPLY VOLTAGE VCC+

FIGURE 9

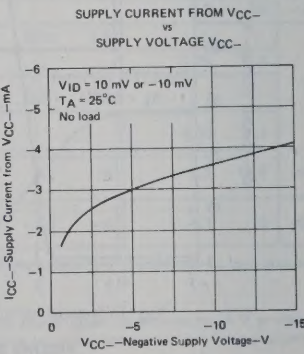

SUPPLY CURRENT FROM VCC− vs SUPPLY VOLTAGE VCC−

FIGURE 10

TYPICAL APPLICATION DATA

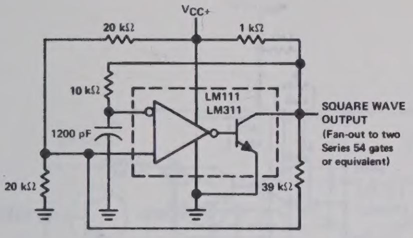

VCC+
20 kΩ
1 kΩ
10 kΩ
LM111
LM311
1200 pF
SQUARE WAVE OUTPUT
(Fan-out to two Series 54 gates or equivalent)
20 kΩ
39 kΩ

FIGURE 11—100-kHz FREE-RUNNING MULTIVIBRATOR

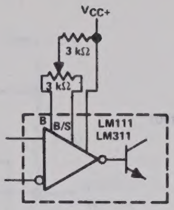

VCC+
3 kΩ
3 kΩ
B
B/S
LM111
LM311

FIGURE 12 OFFSET BALANCING

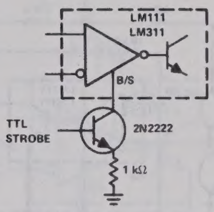

LM111
LM311
B/S
TTL STROBE
2N2222
1 kΩ

FIGURE 13—STROBING

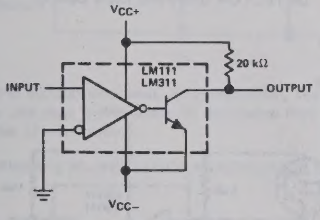
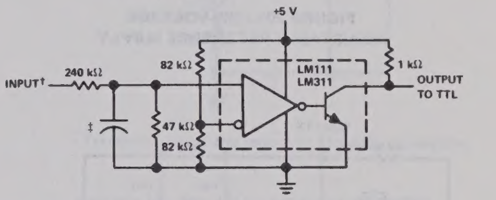

VCC+
20 kΩ
LM111
LM311
INPUT
OUTPUT
VCC−

FIGURE 14—ZERO-CROSSING DETECTOR


+5 V
82 kΩ
1 kΩ
240 kΩ
INPUT†
LM111
LM311
OUTPUT TO TTL
‡
47 kΩ
82 kΩ

†Resistor values shown are for a 0-to-30-V logic swing and a 15-V threshold.

‡May be added to control speed and reduce susceptibility to noise spikes.

FIGURE 15—TTL INTERFACE WITH HIGH-LEVEL LOGIC

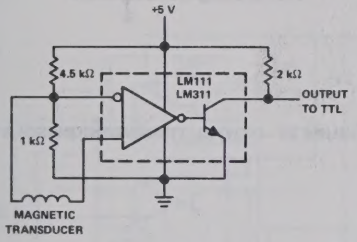

+5 V
4.5 kΩ
2 kΩ
LM111
LM311
OUTPUT TO TTL
1 kΩ
MAGNETIC TRANSDUCER

FIGURE 16—DETECTOR FOR MAGNETIC TRANSDUCER

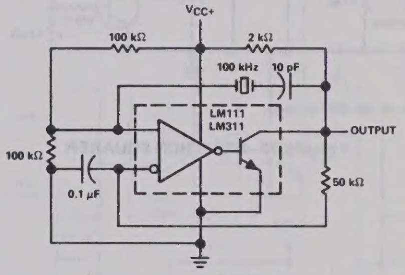

VCC+
100 kΩ
2 kΩ
100 kHz
10 pF
LM111
LM311
OUTPUT
100 kΩ
0.1 μF
50 kΩ

FIGURE 17—100-kHz CRYSTAL OSCILLATOR

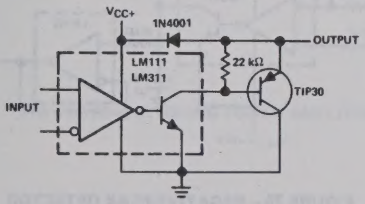
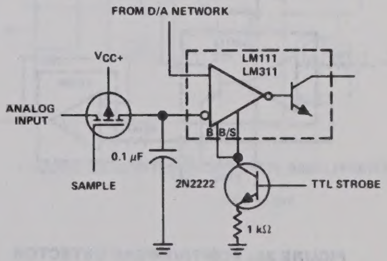

VCC+
1N4001
OUTPUT
LM111
LM311
22 kΩ
TIP30
INPUT

FIGURE 18—COMPARATOR AND SOLENOID DRIVER


FROM D/A NETWORK
VCC+
LM111
LM311
ANALOG INPUT
B
B/S
0.1 μF
SAMPLE
2N2222
TTL STROBE
1 kΩ

Typical input current is 50 pA with inputs strobed off.

FIGURE 19—STROBING BOTH INPUT AND OUTPUT STAGES SIMULTANEOUSLY

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TYPICAL APPLICATION DATA

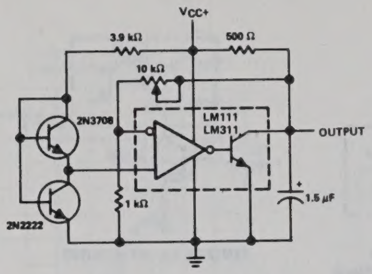

VCC+
3.9 kΩ
500 Ω
10 kΩ
2N3708
LM111
LM311
OUTPUT
1 kΩ
1.5 µF
2N2222

FIGURE 20–LOW-VOLTAGE ADJUSTABLE REFERENCE SUPPLY

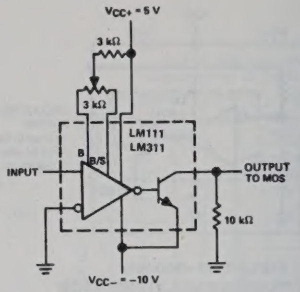
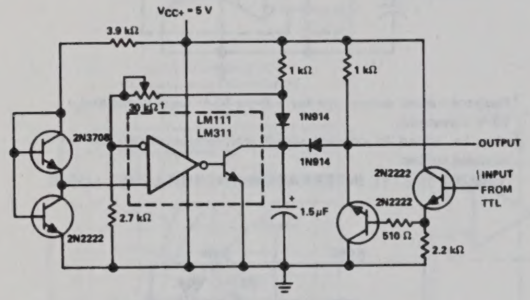

VCC+ = 5 V
3 kΩ
3 kΩ
LM111
LM311
B
B/S
INPUT
OUTPUT TO MOS
10 kΩ
VCC– = –10 V

FIGURE 21– ZERO-CROSSING DETECTOR DRIVING MOS LOGIC


VCC+ = 5 V
3.9 kΩ
1 kΩ
1 kΩ
20 kΩ†
LM111
LM311
1N914
2N3708
OUTPUT
1N914
2N2222
INPUT FROM TTL
2N2222
1.5µF
2.7 kΩ
2N2222
510 Ω
2.2 kΩ

†Adjust to set clamp level.

FIGURE 22–PRECISION SQUARER

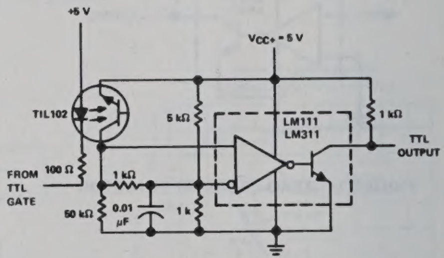

+5 V
VCC+ = 5 V
TIL102
5 kΩ
LM111
LM311
1 kΩ
TTL OUTPUT
FROM TTL GATE
100 Ω
1 kΩ
50 kΩ
0.01 µF
1 k

FIGURE 23–DIGITAL TRANSMISSION ISOLATOR

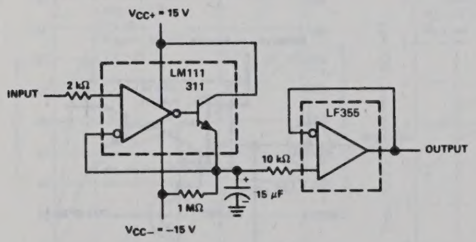

VCC+ = 15 V
LM111
311
INPUT
2 kΩ
LF355
OUTPUT
10 kΩ
1 MΩ
15 µF
VCC– = –15 V

FIGURE 24– POSITIVE-PEAK DETECTOR

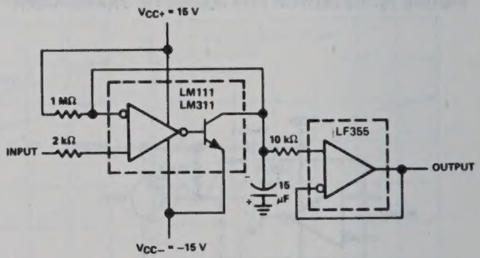
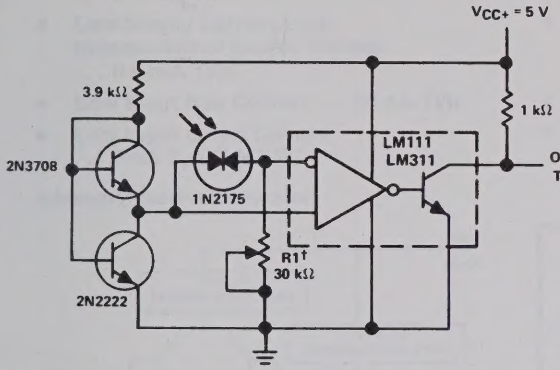

VCC+ = 15 V
LM111
LM311
1 MΩ
2 kΩ
INPUT
10 kΩ
LF355
OUTPUT
15 µF
VCC– = –15 V

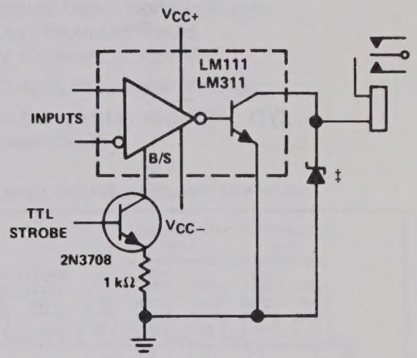
FIGURE 25– NEGATIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA


VCC+ = 5 V
3.9 kΩ
1 kΩ
2N3708
1N2175
LM111
LM311
OUTPUT
TO TTL
R1†
30 kΩ
2N2222

†R1 sets the comparision level. At comparision, the photodiode has less than 5 mV across it, decreasing dark current by an order of magnitude.

FIGURE 26—PRECISION PHOTODIODE COMPARATOR


VCC+
LM111
LM311
INPUTS
B/S
‡
TTL
STROBE
VCC–
2N3708
1 kΩ

‡Transient voltage and inductive kickback protection.

FIGURE 27—RELAY DRIVER WITH STROBE

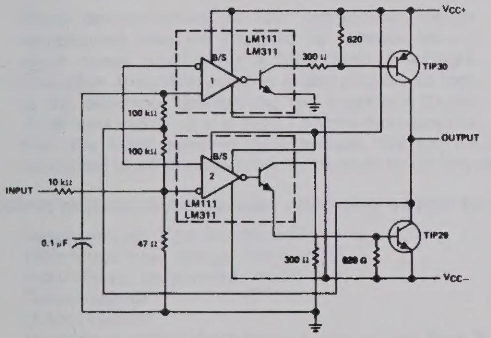

VCC+
LM111
LM311
B/S
1
620
300 Ω
TIP30
100 kΩ
100 kΩ
OUTPUT
B/S
2
INPUT
10 kΩ
LM111
LM311
0.1 μF
47 Ω
300 Ω
620 Ω
TIP29
VCC–

FIGURE 28—SWITCHING POWER AMPLIFIER

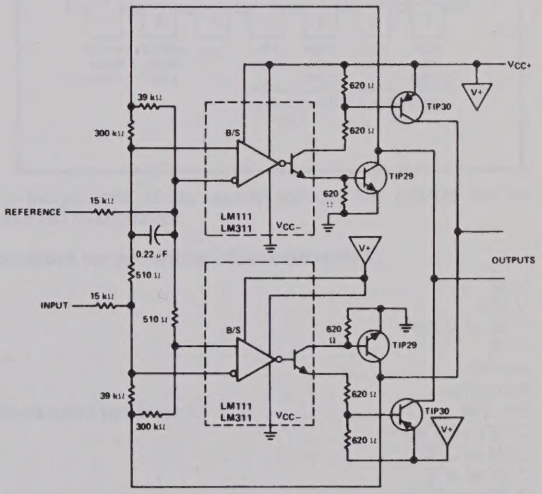

VCC+
620 Ω
39 kΩ
V+
TIP30
300 kΩ
B/S
620 Ω
TIP29
620 Ω
REFERENCE
15 kΩ
LM111
LM311
VCC–
0.22 μF
V+
510 Ω
OUTPUTS
INPUT
15 kΩ
510 Ω
B/S
620 Ω
TIP29
39 kΩ
620 Ω
TIP30
LM111
LM311
VCC–
300 kΩ
V+
620 Ω

FIGURE 29—SWITCHING POWER AMPLIFIERS

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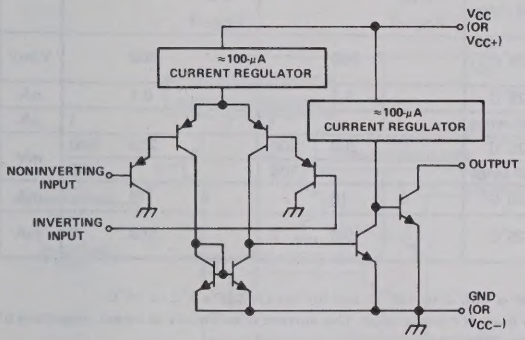
TYPES LM139, LM239, LM339
QUADRUPLE DIFFERENTIAL COMPARATORS

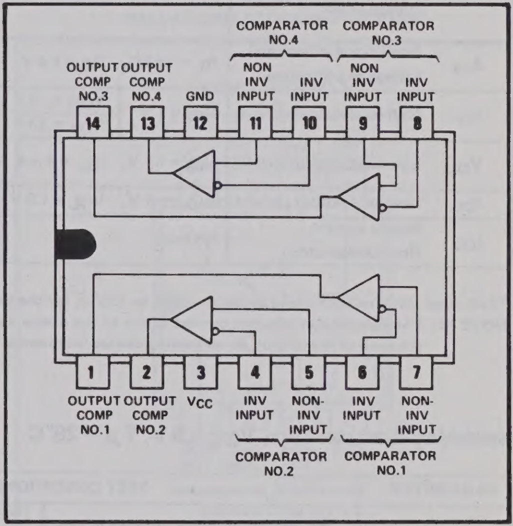
BULLETIN NO. DL-S 7612236, MARCH 1975–REVISED JUNE 1976

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM139)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, DTL, MOS, and CMOS

schematic (each comparator)


VCC (OR VCC+)
≈100-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
GND (OR VCC−)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


COMPARATOR NO.4
COMPARATOR NO.3
OUTPUT COMP NO.3
OUTPUT COMP NO.4
GND
NON INV INPUT
INV INPUT
NON INV INPUT
INV INPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT COMP NO.1
OUTPUT COMP NO.2
VCC
INV INPUT
NON-INV INPUT
INV INPUT
NON-INV INPUT
COMPARATOR NO.2
COMPARATOR NO.1

description

These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 volts to 36 volts and pin 3 is at least 1.5 volts more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	900 mW
Operating free-air temperature range: LM139	−55°C to 125°C
LM239	−25°C to 85°C
LM339	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to VCC can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES LM139, LM239, LM339
QUADRUPLE DIFFERENTIAL COMPARATORS

electrical characteristics at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS†			LM139			LM239, LM339			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$, V_O = 1.4V		25°C		2	5		2	5	mV
				Full range			9			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50	nA
				Full range			100			150	
I_{IB}	Input bias current	See Note 5		25°C		−25	−100		−25	−250	nA
				Full range			−300			−400	
V_{ICR}	Common-mode input voltage range	V_{CC} = 2 V to 36 V		25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			
A_{vd}	Small-signal differential voltage amplification	R_L = 15 kΩ, V_O = 1.4 V		25°C		200			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA		25°C		250	500		250	500	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V		25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	No load		25°C		0.8	2		0.8	2	mA

†Full range (MIN to MAX) for LM139 is −55°C to 125°C, for the LM239 is −85°C to 125°C, and for the LM339 is 0°C to 70°C.

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 6	100-mV input step with 5-mV overdrive		1.3		μs
		TTL-level input step		0.3		

‡C_L includes probe and jig capacitance.

NOTE 6: The typical value is for the interval between the input step function and the time when the output crosses 1.4 V.

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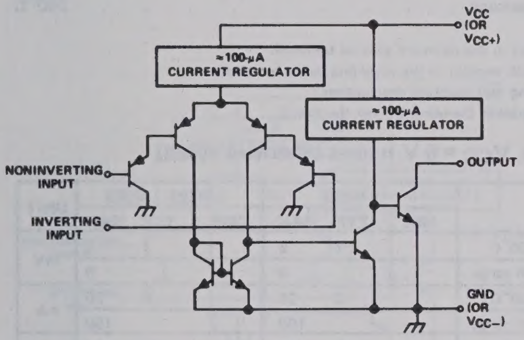
LINEAR INTEGRATED CIRCUITS

TYPES LM193, LM293, LM393 DUAL DIFFERENTIAL COMPARATORS

BULLETIN NO. DL-S 7612411, JUNE 1976

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM193)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, DTL, MOS, and CMOS

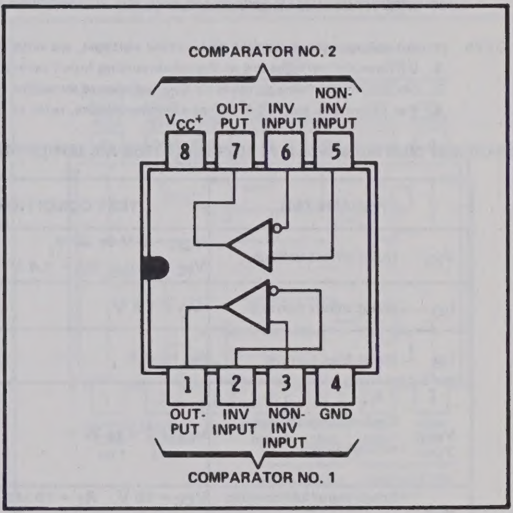
schematic (each comparator)


VCC (OR VCC+)
≈100-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
NONINVERTING INPUT
INVERTING INPUT
OUTPUT
GND (OR VCC−)

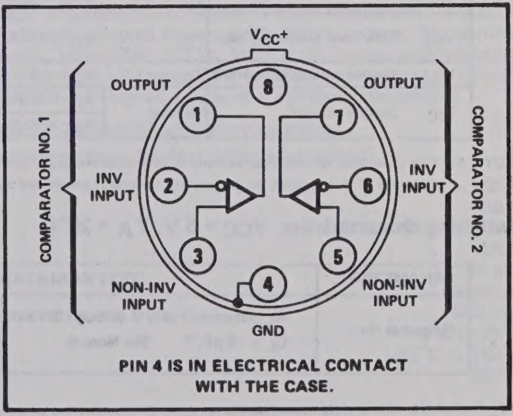
description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 volts to 36 volts and pin 3 is at least 1.5 volts more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)


COMPARATOR NO. 2
VCC+
OUT-PUT
INV INPUT
NON-INV INPUT
8
7
6
5
1
2
3
4
OUT-PUT
INV INPUT
NON-INV INPUT
GND
COMPARATOR NO. 1

L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
OUTPUT
OUTPUT
8
1
7
2
6
3
5
4
COMPARATOR NO. 1
COMPARATOR NO. 2
INV INPUT
INV INPUT
NON-INV INPUT
NON-INV INPUT
GND

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

TYPES LM193, LM293, LM393
DUAL DIFFERENTIAL COMPARATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4):	
JG or P package	900 mW
L package	625 mW
Operating free-air temperature range: LM193	−55°C to 125°C
LM293	−25°C to 85°C
LM393	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG or L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LM193			LM293, LM393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$, V_O = 1.4 V	25°C		1	5		1	5	mV
			Full range			9			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		3	25		5	50	nA
			Full range			100			150	
I_{IB}	Input bias current	See Note 5	25°C		−25	−100		−25	−250	nA
			Full range			−300			−400	
V_{ICR}	Common-mode input voltage range	V_{CC} = 2 V to 36 V	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
A_{vd}	Small-signal differential voltage amplification	V_{CC} = 15 V, R_L = 15 kΩ, V_O = 1.4 V	25°C	50	200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 5 V	25°C		0.1			0.1		nA
		V_{ID} = 1 V, V_{OH} = 30 V	Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		250	400		250	400	mV
			Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_O = 1.5 V	25°C	6	16		6	16		mA
I_{CC}	Supply current	No load, V_{CC} = 5 V	25°C		0.8	1		0.8	1	mA
		No load, V_{CC} = 30 V	Full range			2.5			2.5	

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 6	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

‡C_L includes probe and jig capacitance.

NOTE 6: The typical value is for the interval between the input step function and the time when the output crosses 1.4 V.

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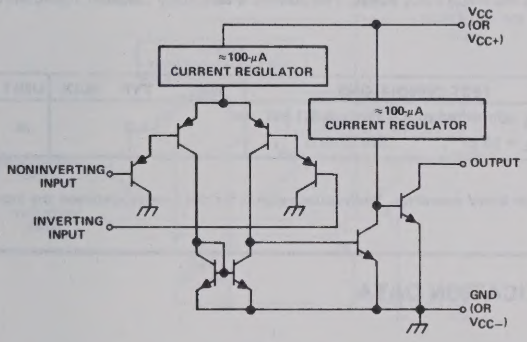
LINEAR
INTEGRATED CIRCUITS

TYPE LM2901
QUADRUPLE DIFFERENTIAL COMPARATOR

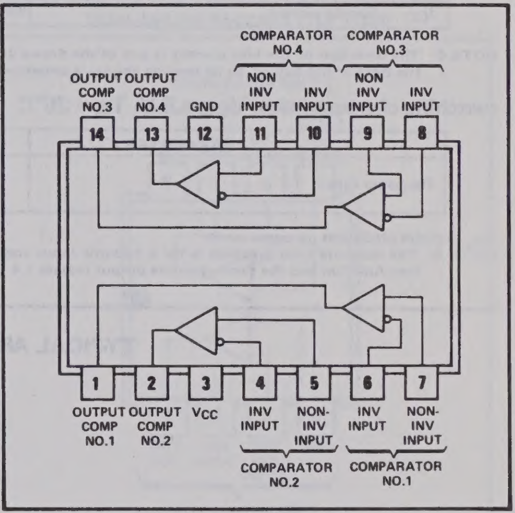
BULLETIN NO. DL-S 7512247, MARCH 1975

- Eliminates Need for Dual Supplies
- Wide Range of Supply Voltages . . . 2 to 36 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias and Offset Parameters
  - Input Offset Voltage . . . 2 mV Typ
  - Input Offset Current . . . 5 nA Typ
  - Input Bias Current . . . –25 nA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
  - . . . 1 mV Typ at 5 μA
  - . . . 70 mV Typ at 1 mA
- Output Compatible with TTL, DTL, MOS, and CMOS

schematic (each comparator)


VCC (OR VCC+)
≈100-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
OUTPUT
NONINVERTING INPUT
INVERTING INPUT
GND (OR VCC–)

N
DUAL-IN-LINE PACKAGE (TOP VIEW)


COMPARATOR NO.4
COMPARATOR NO.3
OUTPUT COMP NO.3
OUTPUT COMP NO.4
GND
NON INV INPUT
INV INPUT
NON INV INPUT
INV INPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT COMP NO.1
OUTPUT COMP NO.2
VCC
INV INPUT
NON-INV INPUT
INV INPUT
NON-INV INPUT
COMPARATOR NO.2
COMPARATOR NO.1

description

The LM2901 consists of four independent voltage comparators designed specifically for automotive and industrial control systems. They operate from a single power supply over a wide range of voltages and the low supply current drain is independent of the magnitude of the supply voltage. A unique characteristic of these comparators is that the common-mode input voltage range includes ground, even though operated from a single supply voltage. Applications include limit comparators, simple analog-to-digital converters, wide-range VCO's, MOS clock timers, multivibrators, high-voltage digital logic gates, and pulse, square-wave, and time-delay generators. The LM2901 was designed to directly interface with CMOS—where the low power drain of the LM2901 is a large advantage over standard comparators.

The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	–0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	900 mW
Operating free-air temperature range	–40°C to 85°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 16 seconds	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPE LM2901
QUADRUPLE DIFFERENTIAL COMPARATOR

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_I \approx 1.4$ V, $V_O = 1.4$ V			2	7	mV
I_{IO}	Input offset current	$V_I \approx 1.4$ V, $V_O = 1.4$ V			5	50	nA
I_{IB}	Input bias current	See Note 5			−25	−250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 2 V to 36 V		0 to $V_{CC}-1.5$			V
A_{vd}	Small-signal differential voltage amplification	R_L = 15 kΩ, V_O = 1.4 V			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 5 V			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 5 μA		1		mV
			I_{OL} = 1 mA		70		
			I_{OL} = 3 mA		200	400	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V		6	16		mA
I_{CC}	Supply current	No load			0.8	2	mA

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stange. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

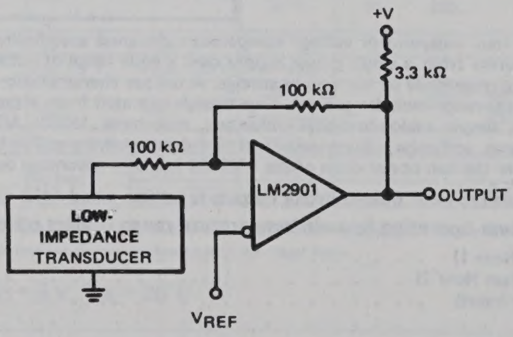
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF†, See Note 6		1.3		μs

†C_L includes probe and jig capacitance.

NOTE 6: The response time specified is for a 100-mV input step with 5-mV overdrive. The typical value is for the interval between the input step function and the time when the output crosses 1.4 V.

TYPICAL APPLICATION DATA



BASIC SINGLE-SUPPLY LEVEL TRANSLATOR

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

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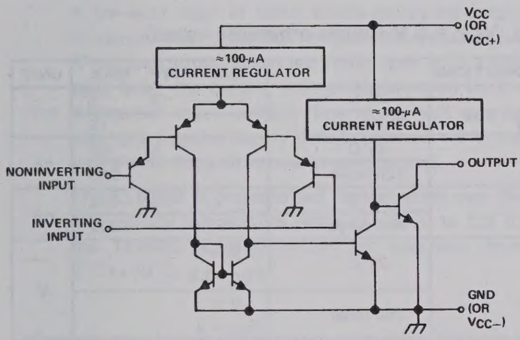
TYPE LM2903
DUAL DIFFERENTIAL COMPARATOR

BULLETIN NO. DL-S 7612412, JUNE 1976

- Eliminates Need for Dual Supplies
- Wide Range of Supply Voltages . . . 2 to 36 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias and Offset Parameters
  - Input Offset Voltage . . . 2 mV Typ
  - Input Offset Current . . . 5 nA Typ
  - Input Bias Current . . . −25 nA Typ
- Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
  - . . . 1 mV Typ at 5 μA
  - . . . 70 mV Typ at 1 mA
- Output Compatible with TTL, DTL, MOS, and CMOS

schematic (each comparator)

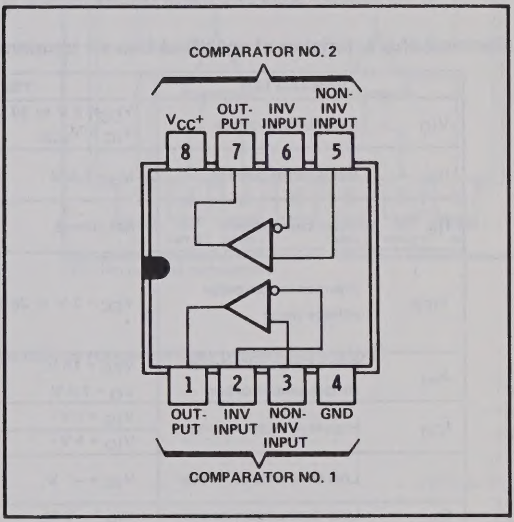

VCC (OR VCC+)
≈100-μA CURRENT REGULATOR
≈100-μA CURRENT REGULATOR
OUTPUT
NONINVERTING INPUT
INVERTING INPUT
GND (OR VCC−)

description

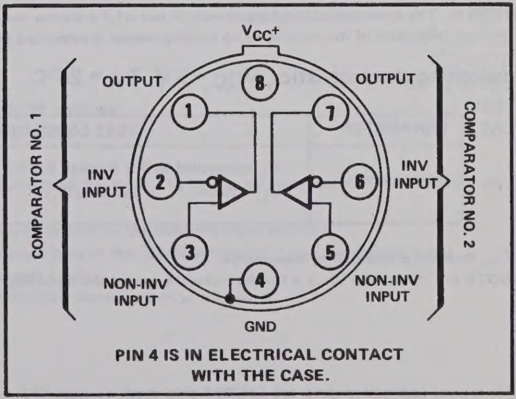
The LM2903 consists of two independent voltage comparators designed specifically for automotive and industrial control systems. They operate from a single power supply over a wide range of voltages and the low supply current drain is independent of the magnitude of the supply voltage. A unique characteristic of these comparators is that the common-mode input voltage range includes ground, even though operated from a single supply voltage. Applications include limit comparators, simple analog-to-digital converters, wide-range VCO's, MOS clock timers, multivibrators, high-voltage digital logic gates, and pulse, square-wave, and time-delay generators. The LM2903 was designed to directly interface with CMOS – where the low power drain of the LM2903 is a large advantage over standard comparators.

The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)


COMPARATOR NO. 2
VCC+
OUT-PUT
INV INPUT
NON-INV INPUT
8
7
6
5
1
2
3
4
OUT-PUT
INV INPUT
NON-INV INPUT
GND
COMPARATOR NO. 1

L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
8
OUTPUT
OUTPUT
1
7
COMPARATOR NO. 1
INV INPUT
2
6
INV INPUT
COMPARATOR NO. 2
3
5
4
NON-INV INPUT
NON-INV INPUT
GND

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

TYPE LM2903
DUAL DIFFERENTIAL COMPARATOR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4): JG or P package	900 mW
L Ipackage	625 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG or L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$,	V_O = 1.4V	25°C		2	7	mV
				Full range			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			200	
I_{IB}	Input bias current	See Note 5		25°C		−25	−250	nA
				Full range			−500	
V_{ICR}	Input common-mode voltage range	V_{CC} = 2 V to 36 V		25°C	0 to V_{CC} −1.5			V
				Full range	0 to V_{CC} − 2			
A_{vd}	Small-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V	R_L = 15 kΩ,		25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_O = 5 V	25°C		1		nA
		V_{ID} = 1 V	V_O = 30 V	Full range			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C			400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current	No load	V_{CC} = 5 V	25°C		0.8	1	mA
			V_{CC} = 30 V	Full range		1	2.5	

NOTE 5: The direction of the bias current is out of the device due to the P-N-P input stage. This current is essentially constant, regardless of the state of the output, so no loading change is presented to the input lines.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF, ‡ See Note 6	100-mV input step with 5-mV overdrive		1.5		μs
		TTL-level input step		0.3		

‡C_L includes probe and jig capacitance.

NOTE 6: The typical value is for the interval between the input step function and the time when the output crosses 1.4 V.

For typical application data, see LM2901 data sheet on page 170.

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TYPES TL506M, TL506C
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

BULLETIN NO. DL-S 7611671, MARCH 1972—REVISED JUNE 1976

FORMERLY SN52506, SN72506

- Each Comparator Identical to LM106 or LM306 with Common V_{CC+}, V_{CC-}, and Ground Connections
- Improved Gain and Accuracy
- Fan-Out to 10 Series 54/74 TTL Loads
- Strobe Capability
- Short-Circuit and Surge Protection
- Fast Response Times

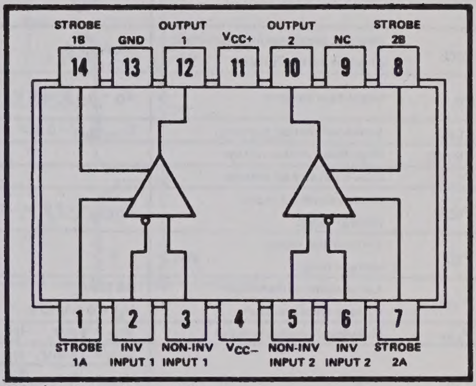
description

The TL506 is a dual high-speed voltage comparator, with each half having differential inputs, a low-impedance output with high-sink-current capability (100 mA), and two strobe inputs. This device detects low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

The circuit is similar to a TL810 with gated output. A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between −3 V and −12 V with little difference in performance.

The TL506M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL506C is characterized for operation from 0°C to 70°C.

J OR N DUAL-IN-LINE PACKAGE OR W FLAT PACKAGE (TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)		15 V
Supply voltage V_{CC-} (see Note 1)		−15 V
Differential input voltage (see Note 2)		±5 V
Input voltage (any input, see Notes 1 and 3)		±7 V
Strobe voltage range (see Note 1)		0 V to V_{CC+}
Output voltage (see Note 1)		24 V
Voltage from output to V_{CC-}		30 V
Duration of output short-circuit (see Note 4)		10 s
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5):	Each amplifier	600 mW
	Total package	800 mW
Operating free-air temperature range:	TL506M Circuits	−55°C to 125°C
	TL506C Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds:	J or W package	300°C
Lead temperature 1/16 inch from case for 10 seconds:	N package	260°C

NOTES:
1. All voltage values, except differential voltages and the voltage from the output to V_{CC-}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 volts, whichever is less.
4. One output at a time may be shorted to ground or either power supply.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES TL506M, TL506C
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = –3 V to –12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL506M			TL506C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 6	25°		0.5§	2		1.6§	5	mV
			Full range			3			6.5	
α_{VIO}	Average temperature coefficient of input offset voltage	See Note 6	Full range		3	10		5	20	µV/°C
I_{IO}	Input offset current	See Note 6	25°C		0.7§	3		1.8§	5	µA
			MIN		2	7		1	7.5	
			MAX		0.4	3		0.5		
α_{IIO}	Average temperature coefficient of input offset current	See Note 6	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	V_O = 0.5 V to 5 V	25°C		7§	20		16§	25	µA
			Full range			45			40	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)}$ = 0.4 V	Full range		–1.7§	–3.3		–1.7§	–3.3	mA
$V_{IH(S)}$	High-level strobe voltage		Full range	2.5			2.5			V
$V_{IL(S)}$	Low-level strobe voltage		Full range			0.9			0.9	V
V_{ICR}	Common-mode input voltage range	V_{CC-} = –7 V to –12 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0.5 V to 5 V	25°C		40 000§			40 000§		
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = –400 µA	Full range	2.5		5.5	2.5		5.5	V
V_{OL}	Low-level output voltage	V_{ID} = –5 mV, I_{OL} = 100 mA	25°C		0.8§	1.5		0.8§	2	V
		V_{ID} = –5 mV, I_{OL} = 50 mA	Full range			1			1	
		V_{ID} = –5 mV, I_{OL} = 16 mA	Full range			0.4			0.4	
I_{OH}	High-level output current	V_{ID} = 5 mV, V_{OH} = 8 V to 24 V	25°C		0.02§	1		0.02§	2	µA
			Full range			100			100	
I_{CC+}	Supply current from V_{CC+}	V_{ID} = –5 mV, See Note 7	Full range		13.9§	20		13.9§	20	mA
I_{CC-}	Supply current from V_{CC-}	See Note 7	Full range		3.2§	7.2		3.2§	7.2	mA

†Unless otherwise noted, all characteristics are measured with the strobe open.

§These typical values are at V_{CC+} = 12 V, V_{CC-} = –6 V, T_A = 25°C. Full range (MIN to MAX) for TL506M is –55°C to 125°C and for the TL506C is 0°C to 70°C.

NOTES: 6. The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

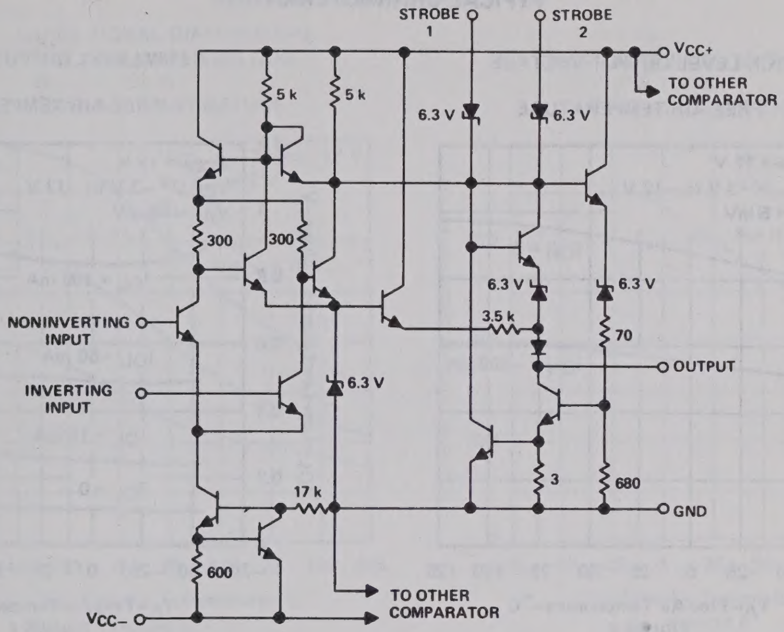
7. Power supply currents are measured with the respective non-inverting inputs and inverting inputs of both comparators connected in parallel. The outputs are open.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = –6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS†	TL506M			TL506C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time, low-to-high-level output	R_L = 390 Ω to 5 V, C_L = 15 pF, See Note 8		28	40		28		ns

NOTE 8: The response time specified is for a 100-mV input step with 5-mV overdrive. The typical value is specified for a nominal threshold voltage of 1.4 V.

schematic (each comparator)


STROBE 1
STROBE 2
VCC+
TO OTHER COMPARATOR
5 k
5 k
6.3 V
6.3 V
300
300
6.3 V
6.3 V
3.5 k
70
NONINVERTING INPUT
OUTPUT
INVERTING INPUT
6.3 V
3
680
17 k
GND
600
TO OTHER COMPARATOR
VCC–

Resistor values are nominal in ohms.

TYPICAL CHARACTERISTICS

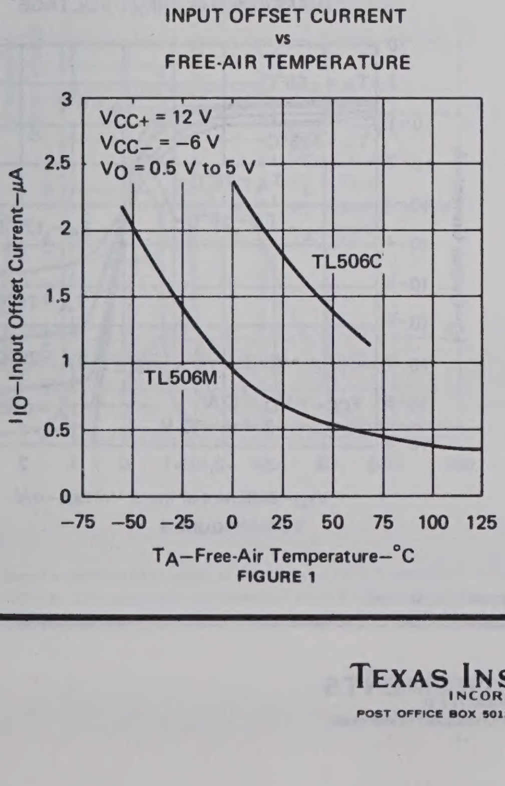


FIGURE 1

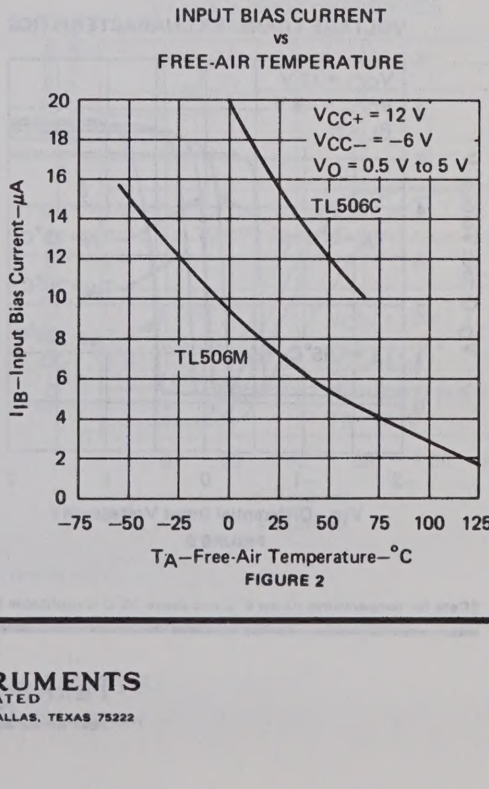


FIGURE 2

TYPICAL CHARACTERISTICS‡

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

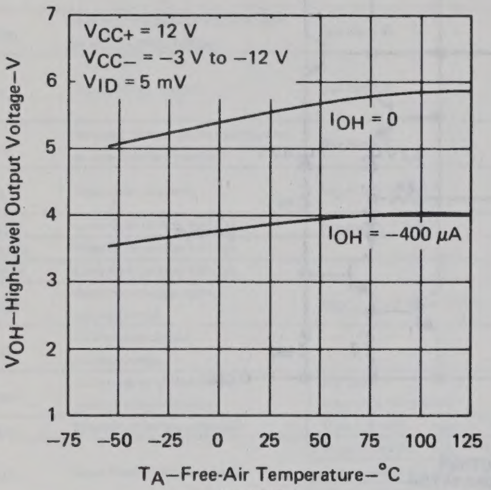


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

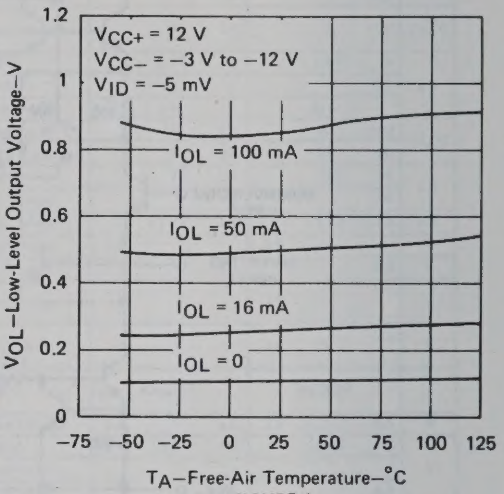


FIGURE 4

VOLTAGE TRANSFER CHARACTERISTICS

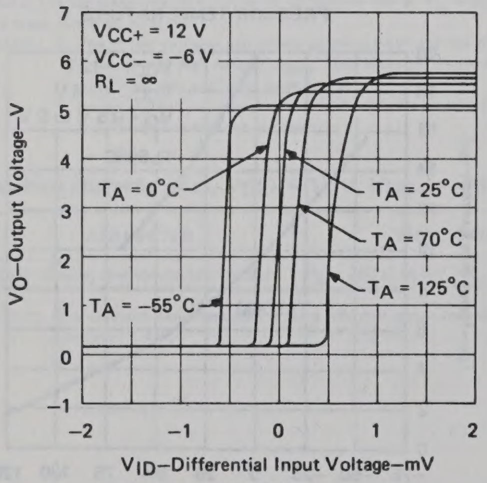


FIGURE 5

OUTPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

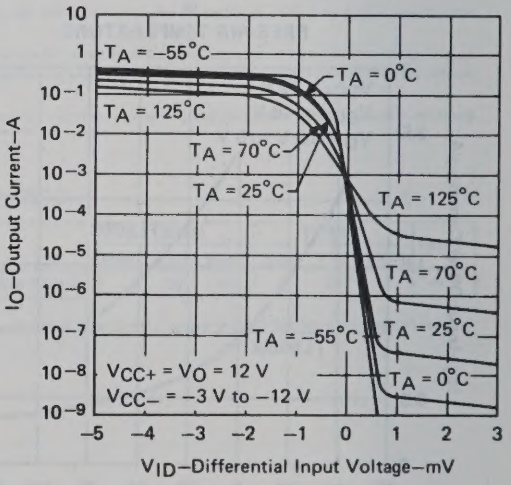


FIGURE 6

---

‡Data for temperatures below 0°C and above 70°C is applicable to TL506M circuits only.

TYPICAL CHARACTERISTICS‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

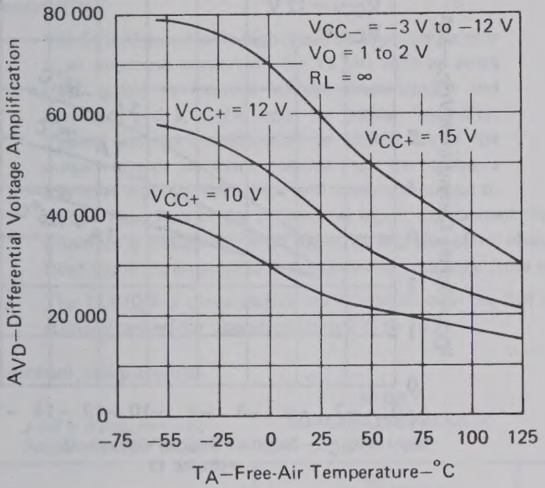


FIGURE 7

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

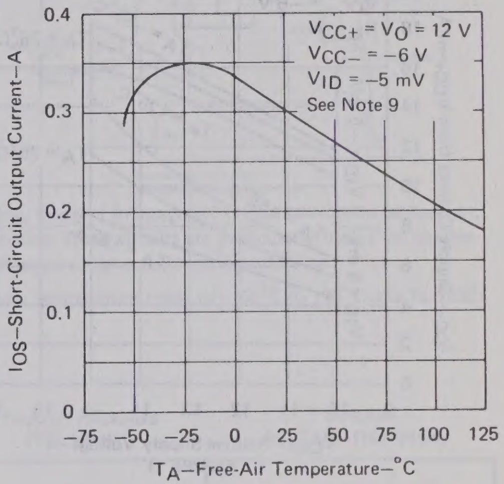


FIGURE 8

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

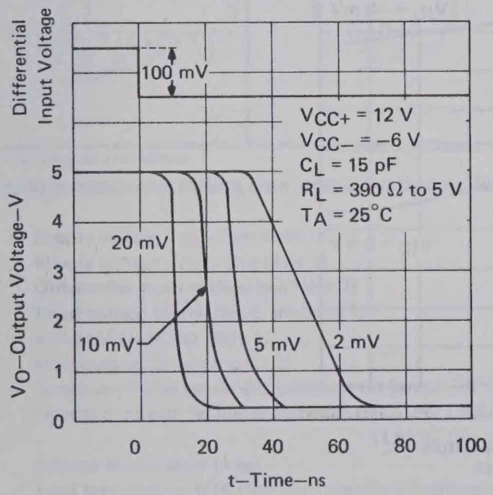


FIGURE 9

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

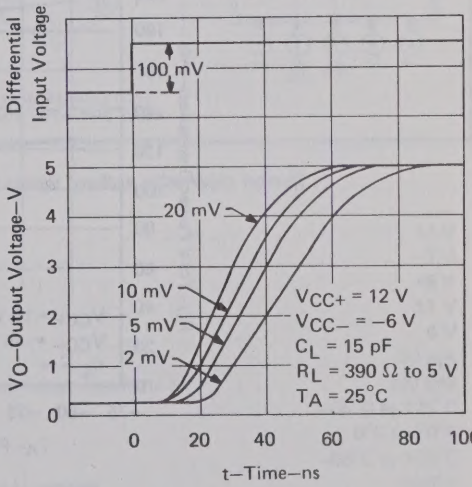


FIGURE 10

---

‡Data for temperatures below 0°C and above 70°C is applicable to TL506M circuits only.

NOTE 9: This parameter was measured using a single 5-ms pulse.

TYPCIAL CHARACTERISTICS‡

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

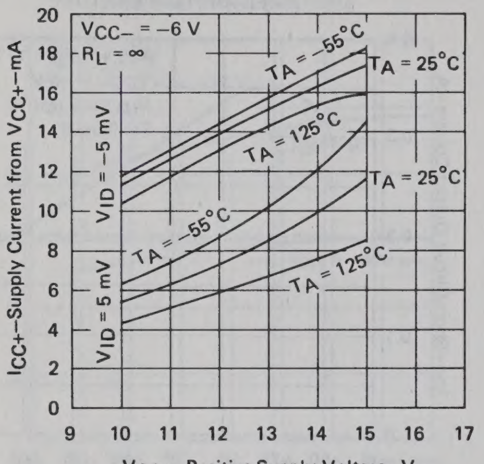


FIGURE 11

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

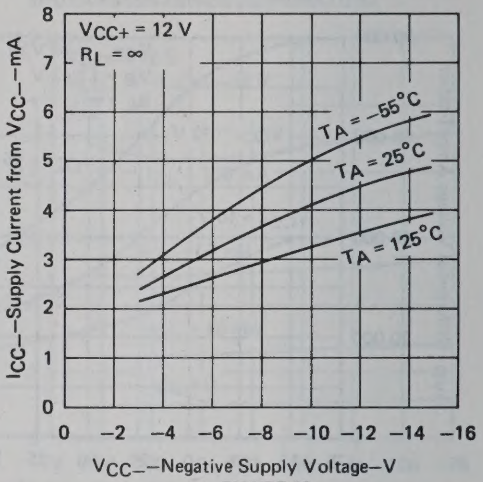


FIGURE 12

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

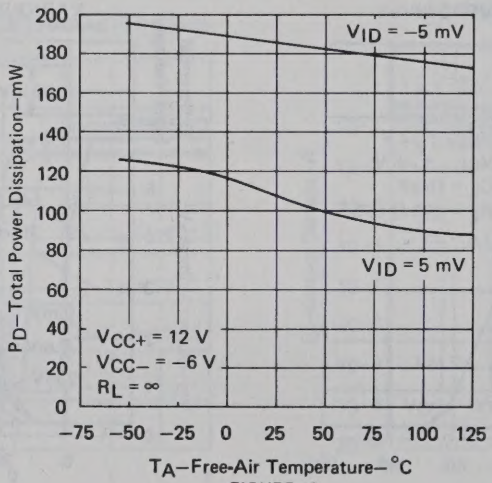


FIGURE 13

‡Data for temperatures below 0°C and above 70°C is applicable to TL506M circuits only.

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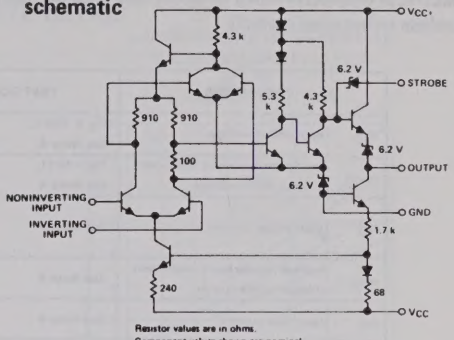
TYPES TL510M, TL510C
DIFFERENTIAL COMPARATORS WITH STROBE

BULLETIN NO. DL-S 7611452, MARCH 1971—REVISED JUNE 1976

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic


VCC+
4.3 k
6.2 V
STROBE
5.3 k
4.3 k
910
910
100
6.2 V
OUTPUT
6.2 V
NONINVERTING INPUT
INVERTING INPUT
GND
1.7 k
240
68
VCC−

Resistor values are in ohms.
Component values shown are nominal.

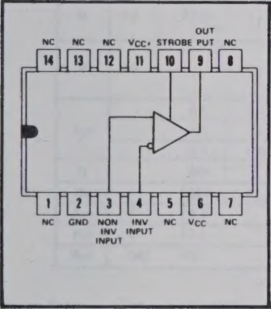
description

The TL510 monolithic high-speed voltage comparator is an improved version of the TL710 with an extra stage added to increase voltage amplification and accuracy, and a strobe input for greater flexibility. Typical voltage amplification is 33,000. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input. Component matching, inherent in integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

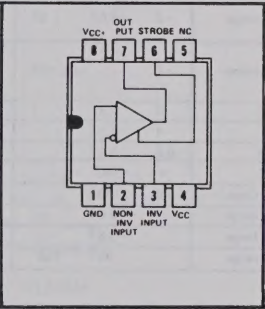
The TL510M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL510C is characterized for operation from 0°C to 70°C.

terminal assignments

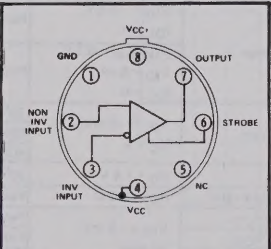
J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)


NC
NC
NC
VCC+
STROBE
OUT PUT
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
GND
NON INV INPUT
INV INPUT
NC
VCC−
NC

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)

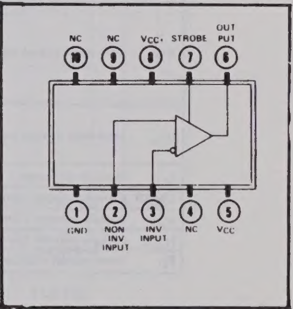

VCC+
OUT PUT
STROBE
NC
8
7
6
5
1
2
3
4
GND
NON INV INPUT
INV INPUT
VCC−

L PLUG-IN PACKAGE
(TOP VIEW)


VCC+
GND
OUTPUT
8
1
7
NON INV INPUT
2
6
STROBE
3
5
INV INPUT
4
NC
VCC−

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT
PACKAGE (TOP VIEW)


NC
NC
VCC+
STROBE
OUT PUT
10
9
8
7
6
1
2
3
4
5
GND
NON INV INPUT
INV INPUT
NC
VCC−

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_W \leqslant 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: TL510M Circuits	−55°C to 125°C
TL510C Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, JG, L, or U package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the TL510M above 70°C free-air temperature, refer to Dissipating Derating Curves, Section 2.

TYPES TL510M, TL510C
DIFFERENTIAL COMPARATORS WITH STROBE

electrical characteristics at specified free-air temperature, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL510M			TL510C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 4	MIN to 25°C		3	10		3	20	µV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	µA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	µA
			MIN		12	25		9	30	
$I_{IH(S)}$	High-level strobe current	$V_{(strobe)} = 5$ V, $V_{ID} = -5$ mV	25°C			±100			±100	µA
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)} = -100$ mV, $V_{ID} = 5$ mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	$V_{CC-} = -7$ V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, $V_O = 0$ to 2.5 V	25°C	12.5	33		10	33		V/mV
			Full range	10			8			
V_{OH}	High-level output voltage	$V_{ID} = 5$ mV, $I_{OH} = 0$	Full range		4§	5		4§	5	V
		$V_{ID} = 5$ mV, $I_{OH} = -5$ mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	$V_{ID} = -5$ mV, $I_{OL} = 0$	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)} = 0.3$ V, $V_{ID} = 5$ mV, $I_{OL} = 0$	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	$V_{ID} = -5$ mV, $V_O = 0$	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	$V_O = 1.4$ V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -5$ mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

† Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for TL510M is −55°C to 125°C and for the TL510C is 0°C to 70°C.

‡ The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§ These typical values are at $T_A = 25$°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL510M, $V_O = 1.8$ V at $T_A = -55$°C, $V_O = 1.4$ V at $T_A = 25$°C, and $V_O = 1$ V at $T_A = 125$°C; for TL510C, $V_O = 1.5$ V at $T_A = 0$°C, $V_O = 1.4$ V at 25°C, and $V_O = 1.2$ V at $T_A = 70$°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V, $T_A = 25$°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	$R_L = \infty$,	$C_L = 5$ pF,	See Note 5		30	80	ns
Strobe release time	$R_L = \infty$,	$C_L = 5$ pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

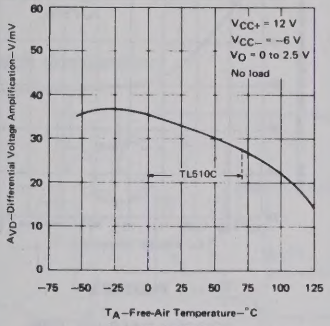


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

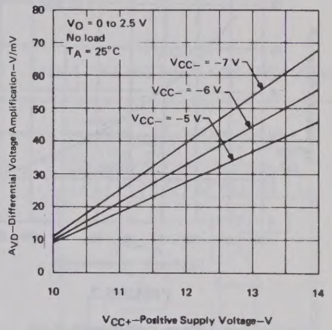


FIGURE 2

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

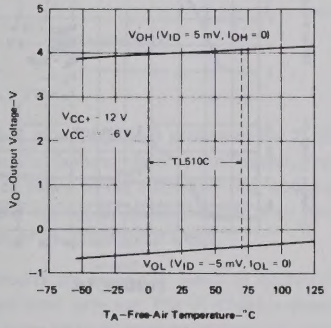


FIGURE 3

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

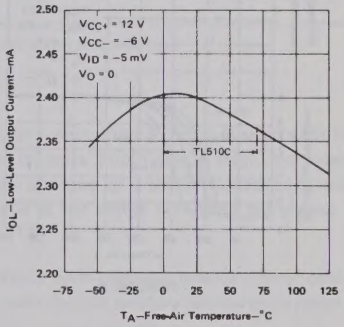


FIGURE 4

TL510M
VOLTAGE TRANSFER CHARACTERISTICS

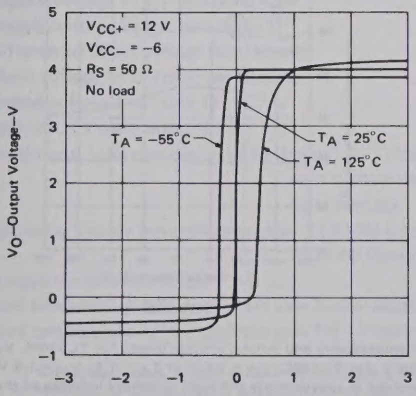


FIGURE 5

TL510C
VOLTAGE TRANSFER CHARACTERISTICS

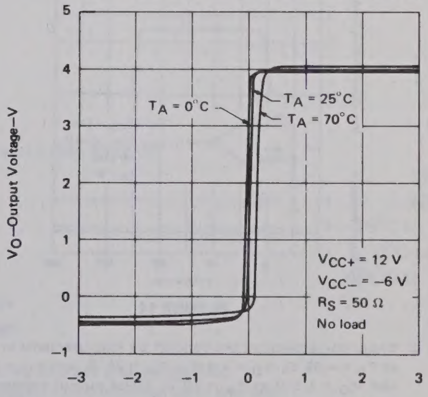


FIGURE 6

TYPES TL510M, TL510C
DIFFERENTIAL COMPARATORS WITH STROBE

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

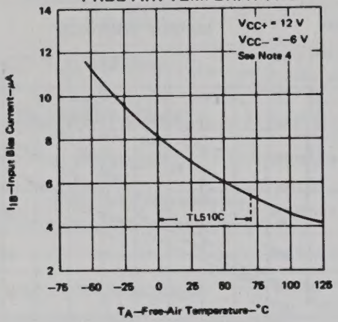


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

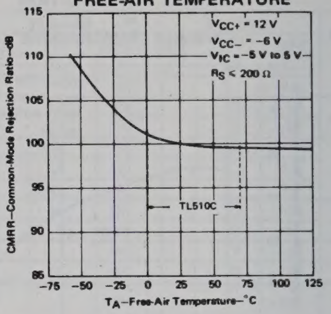


FIGURE 8

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

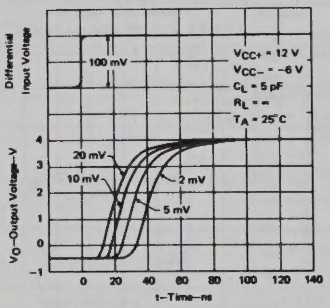


FIGURE 9

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

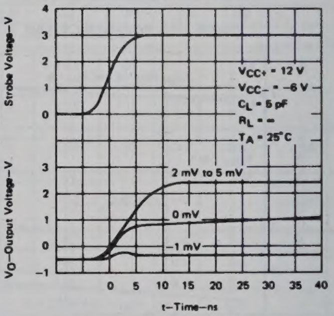


FIGURE 10

COMMON-MODE PULSE RESPONSE

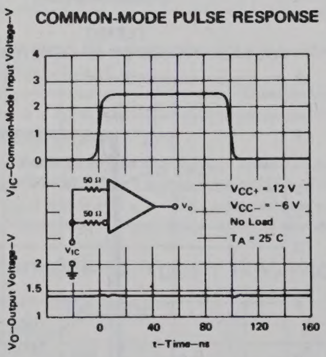


FIGURE 11

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

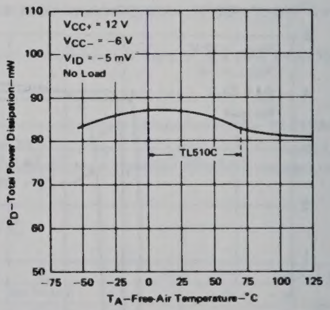


FIGURE 12

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL510M, $V_O = 1.8$ V at $T_A = -55$°C, $V_O = 1.4$ V at $T_A = 25$°C, and $V_O = 1$ V at $T_A = 125$°C; for TL510C, $V_O = 1.5$ V at $T_A = 0$°C, $V_O = 1.4$ V at 25°C, and $V_O = 1.2$ V at $T_A = 70$°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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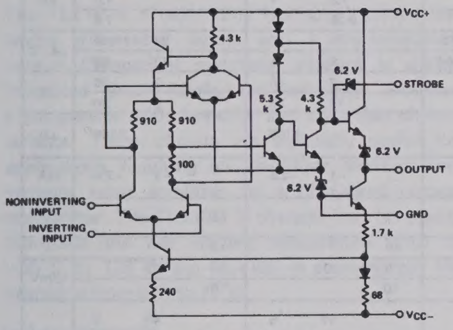
TYPES TL514M, TL514C
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

BULLETIN NO. DL-S 7611451, MARCH 1971–REVISED JUNE 1976

FORMERLY SN52514, SN72514

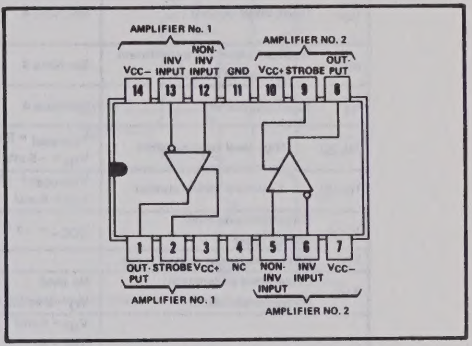
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)


VCC+
4.3 k
6.2 V
STROBE
5.3 k
4.3 k
910
910
100
6.2 V
OUTPUT
6.2 V
NONINVERTING INPUT
INVERTING INPUT
GND
1.7 k
240
68
VCC–

Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


AMPLIFIER No. 1
AMPLIFIER NO. 2
VCC–
INV INPUT
NON-INV INPUT
GND
VCC+
STROBE
OUTPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT
STROBE
VCC+
NC
NON-INV INPUT
INV INPUT
VCC–
AMPLIFIER NO. 1
AMPLIFIER NO. 2

NC—No internal connection

description

The TL514 is an improved version of the TL720 dual high-speed voltage comparator. When compared with the TL720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage, increased accuracy because of lower offset characteristics, and greater flexibility with the addition of a strobe to each comparator. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input.

These circuits are especially useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The TL514M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL514C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)		14 V
Supply voltage V_{CC-} (see Note 1)		−7 V
Differential input voltage (see Note 2)		±5 V
Input voltage (any input, see Note 1)		±7 V
Strobe voltage (see Note 1)		6 V
Peak output current ($t_w \leqslant 1$ s)		10 mA
Continuous total dissipation at (or below) 70°C free-air temperature (See Note 3):	each comparator	300 mW
	total package	600 mW
Operating free-air temperature range:	TL514M Circuits	−55°C to 125°C
	TL514C Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the TL514M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

TYPES TL514M, TL514C
DUAL DIFFERENTIAL COMPARATORS WITH STROBES

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL514M			TL514C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
$I_{IL(S)}$	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100			±100	μA
$I_{IH(S)}$	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC-} = −7 V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12.5	33		10	33		V/mV
			Full range	10			8			
V_{OH}	High-level output voltage	V_{ID} = 5 mV I_{OH} = 0	Full range		4§	5		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	Full range	−1		0‡	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	V_O = 1.4 V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} ¶	V_{ID} = −5 mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} ¶		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation ¶		Full range		90§	150		90§	150	mW

† Unless otherwise noted, all characteristics are measured with the strobe open. Full range (MIN to MAX) for TL514M is −55°C to 125°C and for the TL514C is 0°C to 70°C.

‡ The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§ These typical values are at T_A = 25°C.

¶ Suppy current and power dissipation limits apply for each comparator.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL514M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for TL514C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Response time	$R_L = \infty$,	C_L = 5 pF,	See Note 5		30	80	ns
Strobe release time	$R_L = \infty$,	C_L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

For typical characteristic curves, see the TL510 data sheet on page 181.

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TYPES TL710M, TL710C DIFFERENTIAL COMPARATORS

BULLETIN NO. DL-S 7611441, FEBRUARY 1971–REVISED JUNE 1976

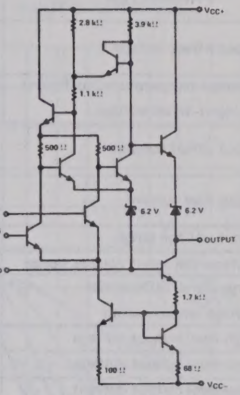
FORMERLY SN52710, SN72710

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The TL710 is a monolithic high-speed comparator having differential inputs and a low-impedance output. Component matching, inherent in silicon integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The TL710M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL710C is characterized for operation from 0°C to 70°C.

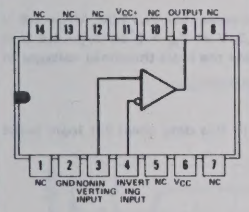
schematic


VCC+
2.8 kΩ
3.9 kΩ
1.1 kΩ
500 Ω
500 Ω
NONINVERTING INPUT
INVERTING INPUT
6.2 V
6.2 V
OUTPUT
GND
1.7 kΩ
100 Ω
68 Ω
VCC−

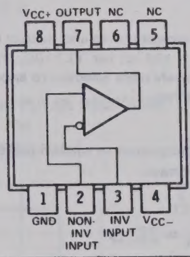
Component values shown are nominal.

terminal assignments

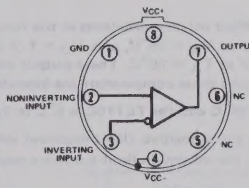
J OR N
DUAL-IN-LINE
PACKAGE (TOP VIEW)


NC
NC
NC
VCC+
NC
OUTPUT
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
GND
NONINVERTING INPUT
INVERTING INPUT
NC
VCC
NC

JG OR P
DUAL-IN-LINE
PACKAGE (TOP VIEW)

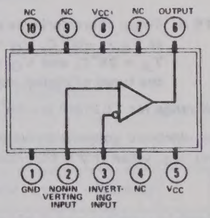

VCC+
OUTPUT
NC
NC
8
7
6
5
1
2
3
4
GND
NON-INV INPUT
INV INPUT
VCC−

L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
8
GND
1
OUTPUT
7
NONINVERTING INPUT
2
6
NC
INVERTING INPUT
3
5
NC
4
VCC−

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE
(TOP VIEW)


NC
NC
VCC+
NC
OUTPUT
10
9
8
7
6
1
2
3
4
5
GND
NONINVERTING INPUT
INVERTING INPUT
NC
VCC

NC–No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL710M	TL710C	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Note 1)		±7	±7	V
Peak output current ($t_w \leqslant 1$ s)		10	10	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the TL710M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TL710M			TL710C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$,	See Note 4	25°C		2	5		2	7.5	mV
				Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$,	See Note 4	Full range		5			7.5		µV/°C
I_{IO}	Input offset current	See Note 4		25°C		1	10		1	15	µA
				Full range			20			25	
I_{IB}	Input bias current	See Note 4		25°C		25	75		25	100	µA
				Full range			150			150	
V_I	Input voltage range	V_{CC-} = −7 V		25°C	±5			±5			V
V_{ID}	Differential input voltage range			25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load,	See Note 4	25°C	750	1500		700	1500		
				Full range	500			500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV,	I_{OH} = −0.5 mA	25°C	2.5	3.2	4	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV,	I_{OL} = 0	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
I_{OL}	Low-level output current	V_{ID} = −15 mV,	V_O = 0	25°C	1.6	2.5					mA
r_o	Output resistance	V_O = 1.4 V		25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$		25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −5 V to 5 V (−10 mV for typ), No load		25°C		5.4	10.1		5.4		mA
I_{CC-}	Supply current from V_{CC-}			25°C		−3.8	−8.9		−3.8		mA
P_D	Total power dissipation			25°C		88	175		88		mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL710M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for TL710C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Full range for TL710M is −55°C to 125°C and for TL710C is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TL710M	TL710C	UNIT
			TYP	TYP	
Response time	No load,	See Note 5	40	40	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

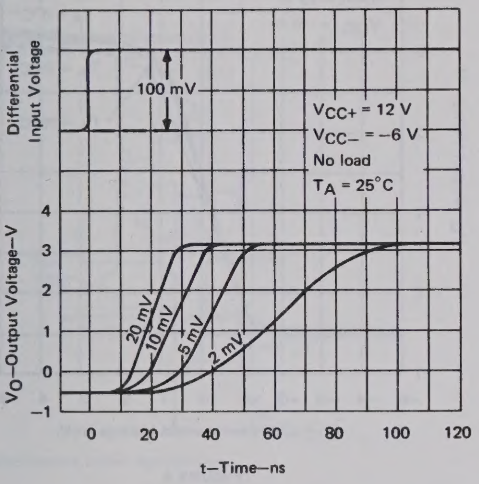


FIGURE 1

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

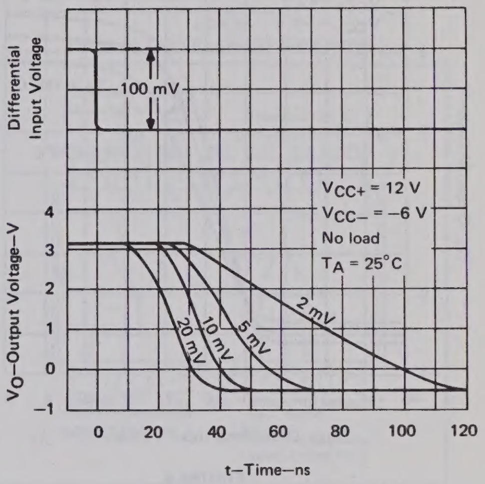


FIGURE 2

COMMON-MODE PULSE RESPONSE
vs
ELAPSED TIME

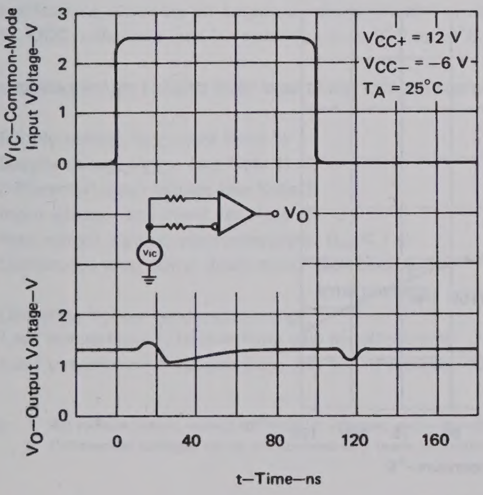


FIGURE 3

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

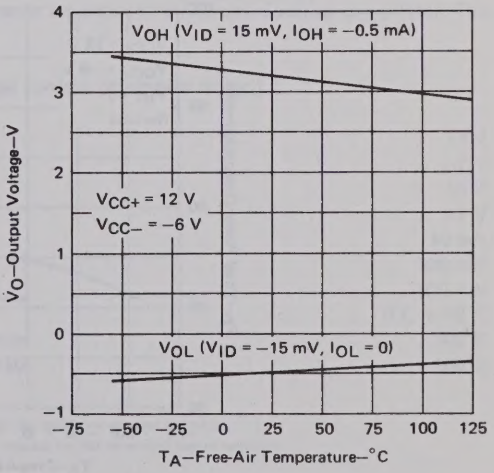


FIGURE 4

TYPICAL CHARACTERISTICS

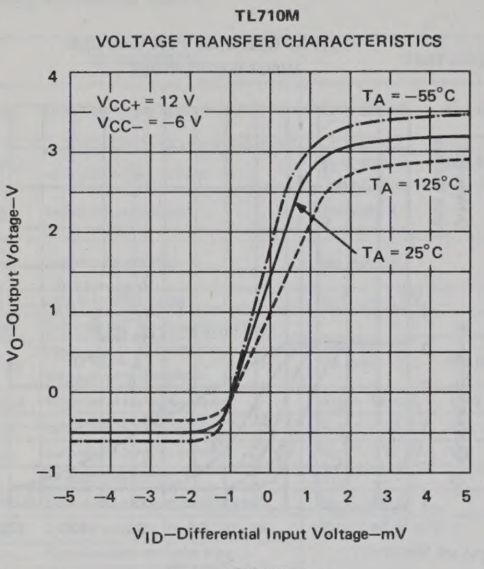


FIGURE 5

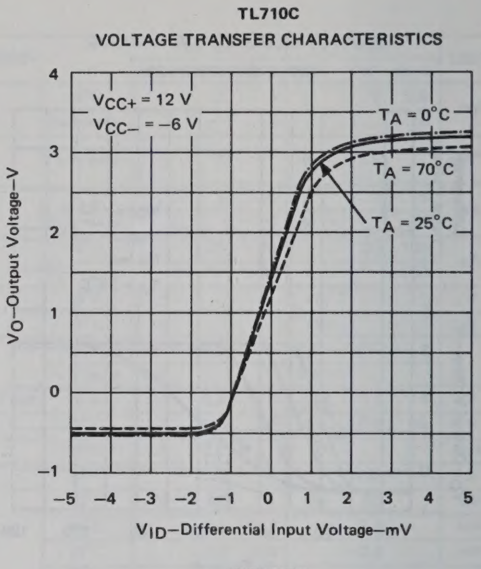


FIGURE 6

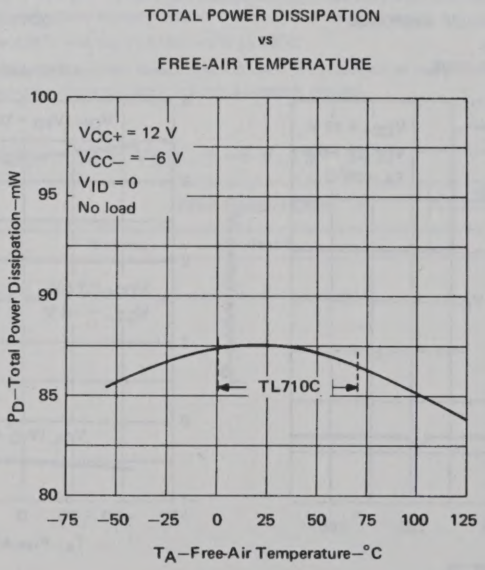


FIGURE 7

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LINEAR
INTEGRATED CIRCUIT

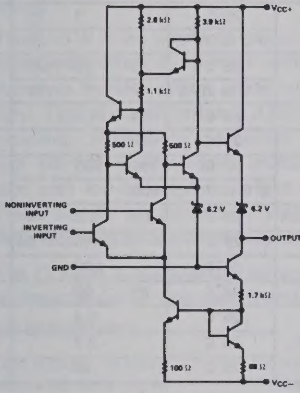
TYPE TL720C
DUAL DIFFERENTIAL COMPARATOR

BULLETIN NO. DL-S 7611440, MARCH 1971–REVISED JUNE 1976

FORMERLY SN72720

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

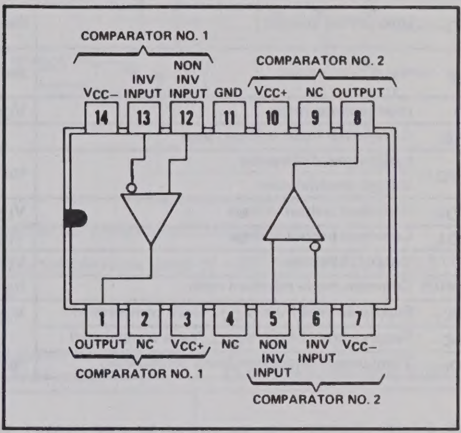
schematic (each comparator)



V_{CC+}
2.8 kΩ
3.9 kΩ
1.1 kΩ
500 Ω
500 Ω
NONINVERTING INPUT
INVERTING INPUT
6.2 V
6.2 V
OUTPUT
GND
1.7 kΩ
100 Ω
V_{CC-}

Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



COMPARATOR NO. 1
V_{CC-}
INV INPUT
NON INV INPUT
GND
COMPARATOR NO. 2
V_{CC+}
NC
OUTPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT
NC
V_{CC+}
NC
NON INV INPUT
INV INPUT
V_{CC-}
COMPARATOR NO. 1
COMPARATOR NO. 2

NC–No internal connection

description

The TL720 is two high-speed comparators in a single package, each electrically identical to the TL710 and having differential inputs and a low-impedance output. Component matching, inherent in silicon monolithic circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. This circuit is especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The TL720C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	–7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (any input, see Note 1)	±7 V
Peak output current, each comparator ($t_w \leqslant 1$ s)	10 mA
Continuous total power dissipation: each comparator	300 mW
total package	600 mW
Operating free-air temperature range	0°C to 70°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

TYPE TL720C
DUAL DIFFERENTIAL COMPARATOR

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	25°C		2	7.5	mV
			0°C to 70°C			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, See Note 3	0°C to 70°C		7.5		µV/°C
I_{IO}	Input offset current	See Note 3	25°C		1	15	µA
			0°C to 70°C			25	
I_{IB}	Input bias current	See Note 3	25°C		25	100	µA
			0°C to 70°C			150	
V_I	Input voltage range	V_{CC-} = −7 V	25°C	±5			V
V_{ID}	Differential input voltage range		25°C	±5			V
A_{VD}	Large-signal differential voltage amplification	No load, See Note 3	25°C	700	1500		
			0°C to 70°C	500			
V_{OH}	High-level output voltage	V_{ID} = 15 mV, I_{OH} = −0.5 mA	25°C	2.5	3.2	4	V
V_{OL}	Low-level output voltage	V_{ID} = −15 mV, I_{OL} = 0	25°C	−1	−0.5	0‡	V
r_o	Output resistance	V_O = 1.4 V	25°C		200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	65	90		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	V_{ID} = −5 V to 5 V (−10 mV for typ), No load	25°C		5.4		mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		25°C		−3.8		mA
P_D	Total power dissipation (each comparator)		25°C		88		mW

NOTE 3: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
Response time	No load, See Note 4	40	ns

NOTE 4: The response time specified is for a 100-mV input step with 5-mV overdrive.

Typical characteristic curves on the TL710 data sheet, pages 187 and 188, are applicable for the TL720.

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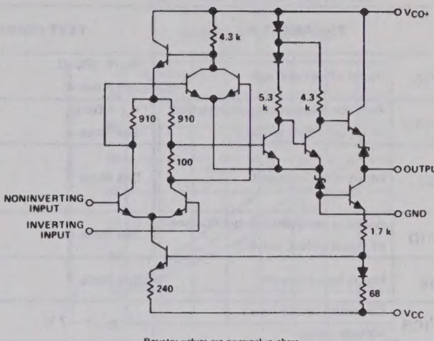
TYPES TL810M, TL810C
DIFFERENTIAL COMPARATORS

BULLETIN NO. DL-S 7611449, MARCH 1971–REVISED JUNE 1976

FORMERLY SN52810, SN72810

- Low Offset Characteristics
- High Differential Voltage Amplification
- Fast Response Times
- Output Compatible with Most TTL and DTL Circuits

schematic


VCC+
4.3 k
5.3 k
4.3 k
910
910
100
OUTPUT
GND
NONINVERTING INPUT
INVERTING INPUT
1.7 k
240
68
VCC–

Resistor values are nominal in ohms

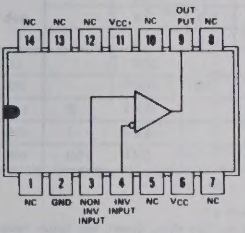
description

The TL810 is an improved version of the TL710 high-speed voltage comparator with an extra stage added to increase voltage amplification and accuracy. Typical amplification is 33,000. Component matching, inherent in monolithic integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. These circuits are particularly useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector.

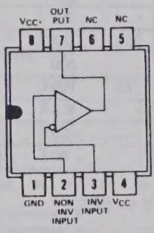
The TL810M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL810C is characterized for operation from 0°C to 70°C.

terminal assignments

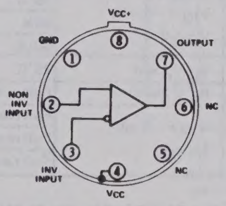
J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)


NC
NC
NC
VCC+
NC
OUT PUT
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
GND
NON INV INPUT
INV INPUT
NC
VCC
NC

JG OR P
DUAL-IN-LINE
PACKAGE (TOP VIEW)

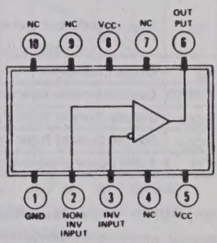

VCC+
OUT PUT
NC
NC
8
7
6
5
1
2
3
4
GND
NON INV INPUT
INV INPUT
VCC

L PLUG-IN PACKAGE
(TOP VIEW)


VCC+
GND
OUTPUT
8
1
7
NON INV INPUT
2
6
NC
3
5
4
INV INPUT
NC
VCC

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

U
FLAT PACKAGE (TOP VIEW)


NC
NC
VCC+
NC
OUT PUT
10
9
8
7
6
1
2
3
4
5
GND
NON INV INPUT
INV INPUT
NC
VCC

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leqslant 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: TL810M Circuits	−55°C to 125°C
TL810C Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, JG, L, or U package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the TL810M above 70°C free-air temperature, refer to Dissipating Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL810M			TL810C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 4	MIN to 25°C		3	10		3	20	µV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	µA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	µA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	$V_{CC-} = -7$ V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, $V_O = 0$ to 2.5 V	25°C	12.5	33		10	33		V/mA
			Full range	10			8			
V_{OH}	High-level output voltage	$V_{ID} = 5$ mV $I_{OH} = 0$	Full range		4§	5		4§	5	V
		$V_{ID} = 5$ mV, $I_{OH} = -5$ mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	$V_{ID} = -5$ mV, $I_{OL} = 0$	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	$V_{ID} = -5$ mV, $V_O = 0$	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	$V_O = 1.4$ V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -5$ mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-}		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation		Full range		90§	150		90§	150	mW

† Full range (MIN to MAX) for TL810M is −55°C to 125°C and for the TL810C is 0°C to 70°C.

‡ The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§ These typical values are at T_A = 25°C.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL810M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for TL810C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	$R_L = \infty$, $C_L = 5$ pF, See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

TYPES TL810M, TL810C
DIFFERENTIAL COMPARATORS

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

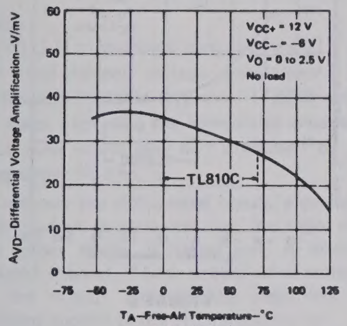


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

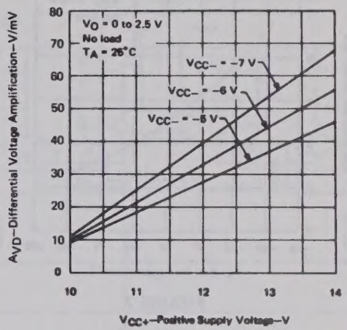


FIGURE 2

OUTPUT VOLTAGE LEVELS vs FREE-AIR TEMPERATURE

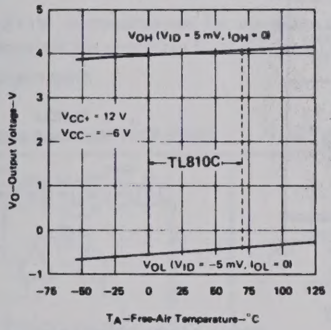


FIGURE 3

LOW-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

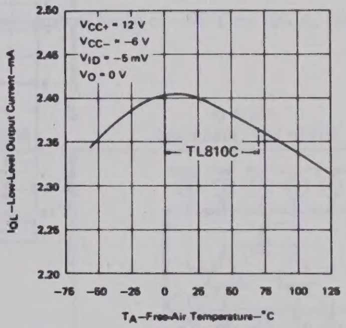


FIGURE 4

TL810M
VOLTAGE TRANSFER CHARACTERISTICS

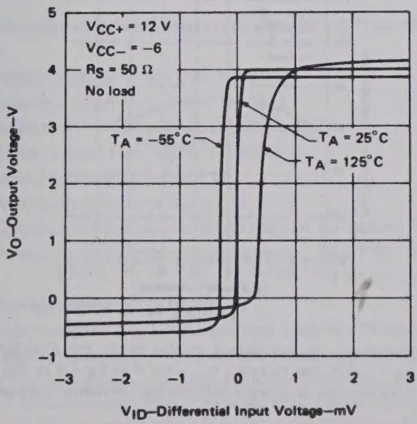


FIGURE 5

TL810C
VOLTAGE TRANSFER CHARACTERISTICS

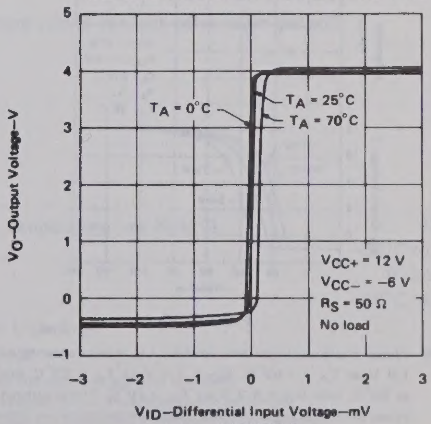


FIGURE 6

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

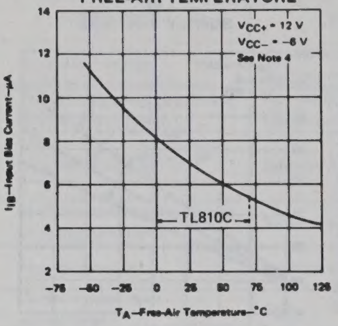


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

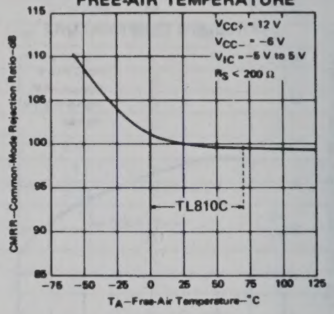


FIGURE 8

COMMON-MODE PULSE RESPONSE

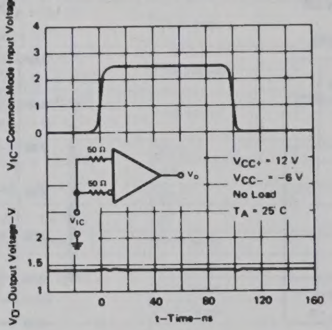


FIGURE 9

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

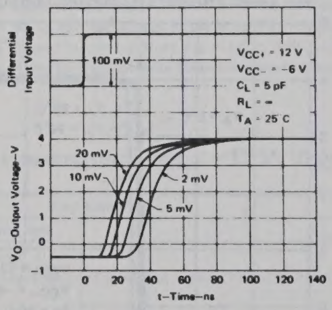


FIGURE 10

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

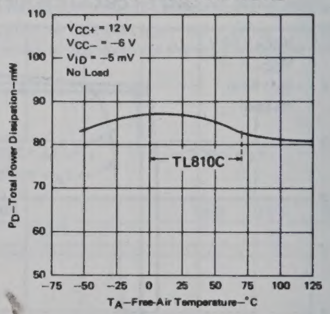


FIGURE 11

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL810M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for TL810C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at 25°C, and V_O = 1.2 V at T_A = 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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TYPES TL811M, TL811C
DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

BULLETIN NO. DL-S 7611464, MARCH 1971–REVISED JUNE 1976

FORMERLY SN52811, SN72811

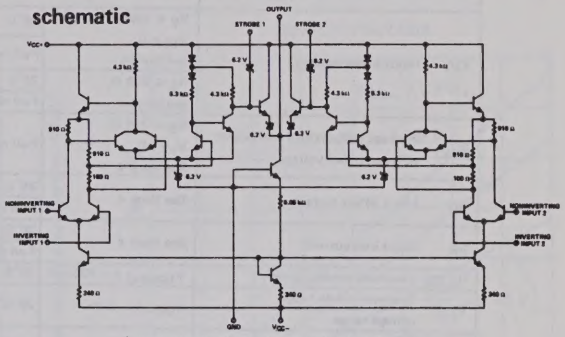
- Fast Response Times
- Improved Voltage Amplification and Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits

description

The TL811 is an improved version of the TL711 high-speed dual-channel voltage comparator. Voltage amplification is higher (typically 17,500) due to an extra stage, increasing the comparator accuracy. The output pulse width may be "stretched" by varying the capacitive loading.

Each channel has differential inputs, a strobe input, and an output in common with the other channel. When either strobe is taken low, it inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs.

schematic


OUTPUT
STROBE 1
STROBE 2
VCC+
4.3 kΩ
6.2 V
6.3 kΩ
910 Ω
100 Ω
6.8 kΩ
240 Ω
NONINVERTING INPUT 1
INVERTING INPUT 1
NONINVERTING INPUT 2
INVERTING INPUT 2
GND
VCC−

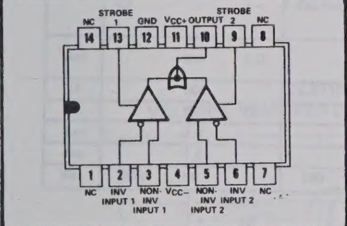
Component values shown are nominal.

These dual-channel voltage comparators are particularly attractive for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage.

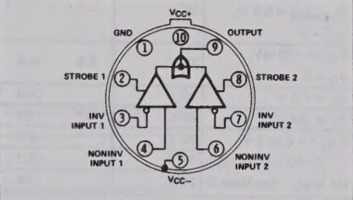
The TL811M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL811C is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

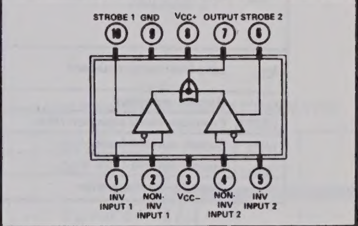

NC
STROBE 1
GND
VCC+
OUTPUT
STROBE 2
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
INV INPUT 1
NON-INV INPUT 1
VCC−
NON-INV INPUT 2
INV INPUT 2
NC

L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
GND
OUTPUT
STROBE 1
STROBE 2
INV INPUT 1
INV INPUT 2
NONINV INPUT 1
NONINV INPUT 2
VCC−
1
2
3
4
5
6
7
8
9
10

PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT
PACKAGE (TOP VIEW)


STROBE 1
GND
VCC+
OUTPUT
STROBE 2
10
9
8
7
6
1
2
3
4
5
INV INPUT 1
NON-INV INPUT 1
VCC−
NON-INV INPUT 2
INV INPUT 2

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (any input, see Note 1)	±7 V
Strobe Voltage (see Note 1)	6 V
Peak output current ($t_w \leq 1$ s)	50 mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	300 mW
Operating free-air temperature range: TL811M Circuits	−55°C to 125°C
TL811C Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J, L, or U package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the TL811M above 70°C free-air temperature, refer to Dissipating Derating Curves, Section 2.

TYPES TL811M, TL811C
DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

electrical characteristics at specified free-air temperature, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL811M			TL811C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, $V_{IC} = 0$, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, $V_{IC} = 0$, See Note 4	Full range		5			5		µV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	3		0.5	5	µA
			Full range			5			10	
I_{IB}	Input bias current	See Note 4	25°C		7	20		7	30	µA
			Full range			30			50	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)} = -100$ mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_{ICR}	Common-mode input voltage range	$V_{CC-} = -7$ V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	$V_O = 0$ to 2.5 V, No load	25°C	12.5	17.5		10	17.5		V/mV
			Full range	8			5			
V_{OH}	High-level output voltage	$V_{ID} = 10$ mV, $I_{OH} = 0$	25°C		4	5		4	5	V
		$V_{ID} = 10$ mV, $I_{OH} = -5$ mA	25°C	2.5	3.6		2.5	3.6		
V_{OL}	Low-level output voltage	$V_{ID} = -10$ mV, $I_{OL} = 0$	25°C	−1	−0.4	0‡	−1	−0.4	0‡	V
		$V_{ID} = 10$ mV, $V_{(strobe)} = 0.3$ V, $I_{OL} = 0$	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	$V_{ID} = -10$ mV, $V_O = 0$	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	$V_O = 1.4$ V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -5$ to 5 V (−10 mV for typ), No load, See Note 5	25°C		6.5			6.5		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−2.7			−2.7		mA
P_D	Total power dissipation		25°C		94	150		94	200	mW

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open, the strobe of the other channel is grounded. Full range for TL811M is −55°C to 125°C and for the TL811C is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

NOTES: 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL811M, $V_O = 1.8$ V at $T_A = -55°C$, $V_O = 1.4$ V at $T_A = 25°C$, and $V_O = 1$ V at $T_A = 125°C$; for TL811C, $V_O = 1.5$ V at $T_A = 0°C$, $V_O = 1.4$ V at $T_A = 25°C$, and $V_O = 1.2$ V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

5. The strobes are alternately grounded.

switching characteristics, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	TL811M			TL811C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Response time	$R_L = \infty$, $C_L = 5$ pF, See Note 6		33	80		33		ns
Strobe release time	$R_L = \infty$, $C_L = 5$ pF, See Note 7		5	25		5		ns

NOTES: 6. The response time specified is for a 100-mV input step with 5-mV overdrive.

7. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

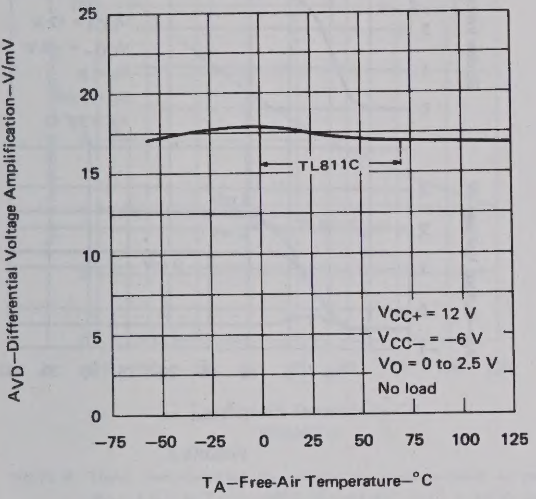


FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

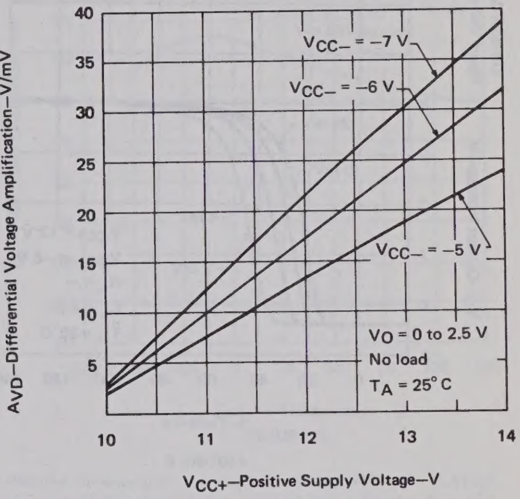


FIGURE 2

TL811M VOLTAGE TRANSFER CHARACTERISTICS

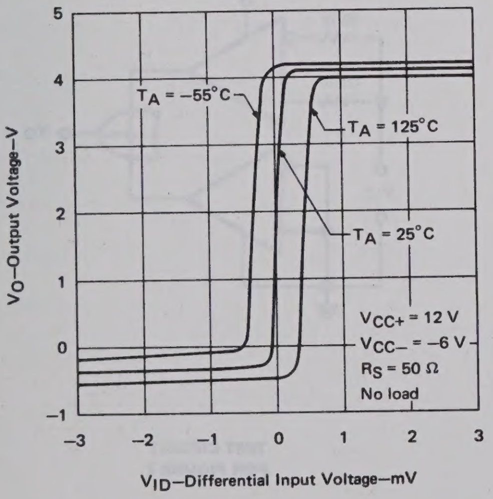


FIGURE 3

TL811C VOLTAGE TRANSFER CHARACTERISTICS

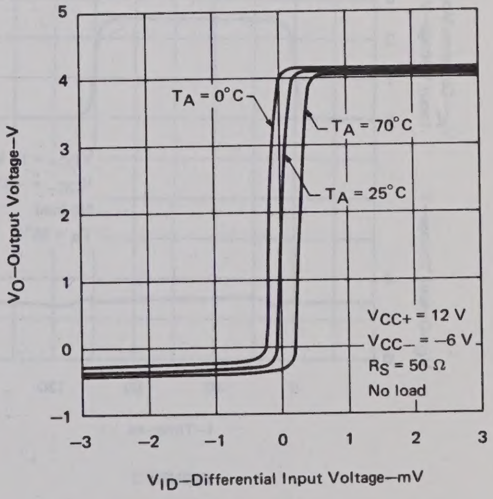


FIGURE 4

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

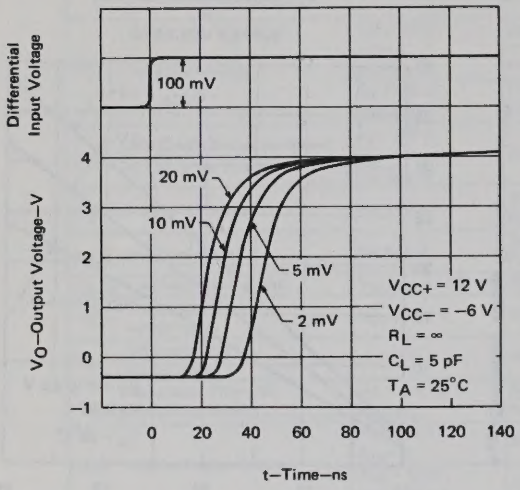


FIGURE 5

STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

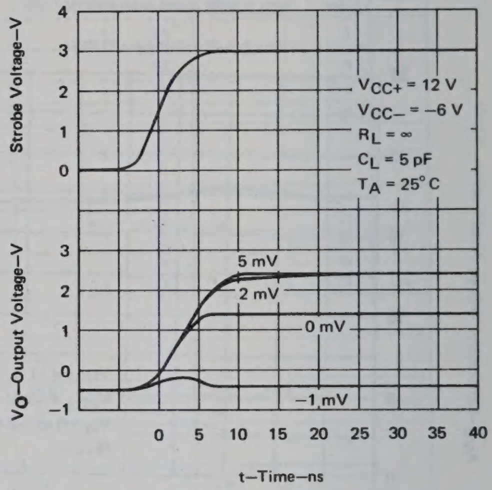


FIGURE 6

COMMON-MODE PULSE RESPONSE

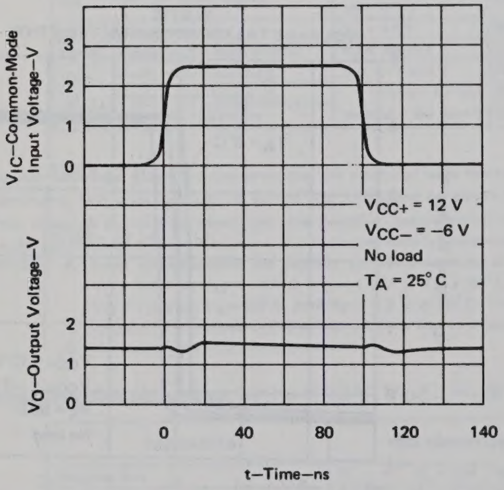
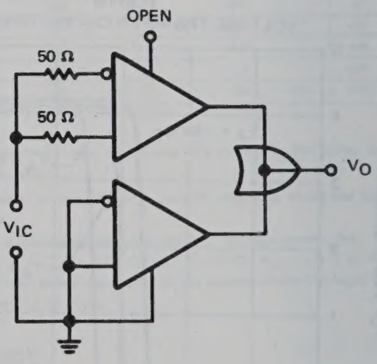


FIGURE 7



TEST CIRCUIT FOR FIGURE 7

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

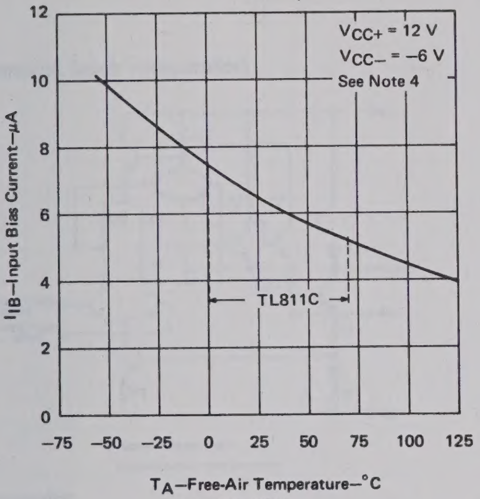


FIGURE 8

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

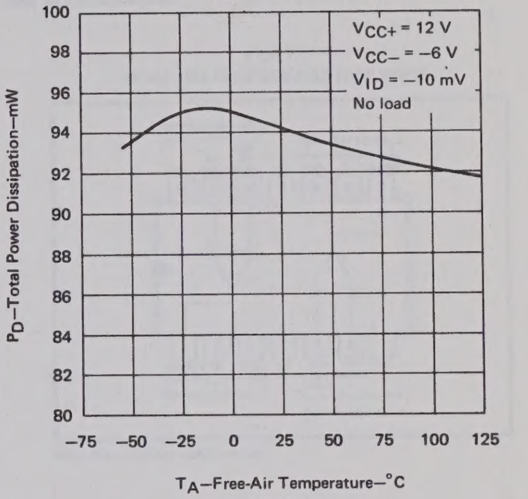


FIGURE 9

NOTE 4. These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL811M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for TL811C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

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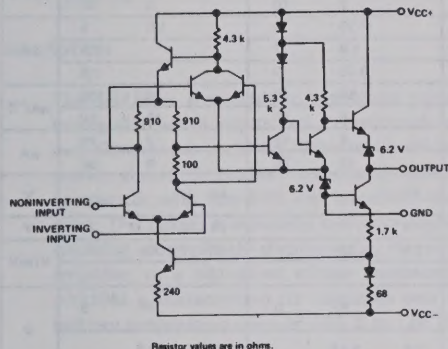
TYPES TL820M, TL820C
DUAL DIFFERENTIAL COMPARATORS

BULLETIN NO. DL-S 7611450, MARCH 1971–REVISED JUNE 1976

FORMERLY SN52820, SN72820

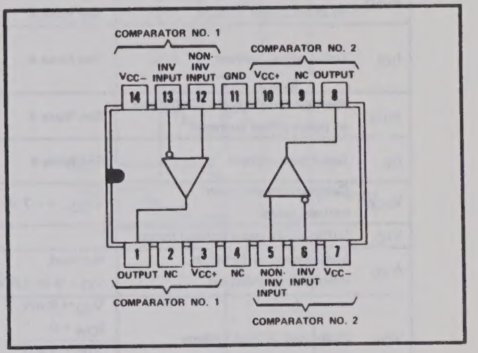
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL and DTL Circuits

schematic (each comparator)


VCC+
4.3 k
910
910
100
5.3 k
4.3 k
6.2 V
OUTPUT
6.2 V
NONINVERTING INPUT
INVERTING INPUT
GND
1.7 k
240
68
VCC−

Resistor values are in ohms.
Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


COMPARATOR NO. 1
COMPARATOR NO. 2
VCC−
INV INPUT
NON-INV INPUT
GND
VCC+
NC
OUTPUT
14
13
12
11
10
9
8
1
2
3
4
5
6
7
OUTPUT
NC
VCC+
NC
NON-INV INPUT
INV INPUT
VCC−
COMPARATOR NO. 1
COMPARATOR NO. 2

NC—No internal connection

description

The TL820 is an improved version of the TL720 dual high-speed voltage comparator. Each comparator has differential inputs and a low-impedance output. When compared with the TL720, these circuits feature high amplification (typically 33,000) due to an extra amplification stage and increased accuracy because of lower offset characteristics. They are particularly useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The TL820M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL820C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	−7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (any input, see Note 1)	±7 V
Peak output current ($t_w \leq 1$ s)	10 mA
Continuous total power dissipation at (or below) 70°C free-air temperature: each comparator	300 mW
total package, (see Note 3)	600 mW
Operating free-air temperature range: TL820M Circuits	−55°C to 125°C
TL820C Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of the TL820M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL820M			TL820C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S < 200\ \Omega$, See Note 4	25°C		0.6	2		1.6	3.5	mV
			Full range			3			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 4	MIN to 25°C		3	10		3	20	μV/°C
			25°C to MAX		3	10		3	20	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3		1.8	5	μA
			MIN		1.8	7			7.5	
			MAX		0.25	3			7.5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	MIN to 25°C		15	75		24	100	nA/°C
			25°C to MAX		5	25		15	50	
I_{IB}	Input bias current	See Note 4	25°C		7	15		7	20	μA
			MIN		12	25		9	30	
V_{ICR}	Common-mode input voltage range	$V_{CC-} = -7$ V	Full range	±5			±5			V
V_{ID}	Differential input voltage range		Full range	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, $V_O = 0$ to 2.5 V	25°C	12.5	33		10	33		V/mV
			Full range	10			8			
V_{OH}	High-level output voltage	$V_{ID} = 5$ mV $I_{OH} = 0$	Full range		4§	5		4§	5	V
		$V_{ID} = 5$ mV, $I_{OH} = -5$ mA	Full range	2.5	3.6§		2.5	3.6§		
V_{OL}	Low-level output voltage	$V_{ID} = -5$ mV, $I_{OL} = 0$	Full range	−1	−0.5§	0‡	−1	−0.5§	0‡	V
I_{OL}	Low-level output current	$V_{ID} = -5$ mV, $V_O = 0$	25°C	2	2.4		1.6	2.4		mA
			MIN	1	2.3		0.5	2.4		
			MAX	0.5	2.3		0.5	2.4		
r_o	Output resistance	$V_O = 1.4$ V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S < 200\ \Omega$	Full range	80	100§		70	100§		dB
I_{CC+}	Supply current from V_{CC+} (each comparator)	$V_{ID} = -5$ mV, No load	Full range		5.5§	9		5.5§	9	mA
I_{CC-}	Supply current from V_{CC-} (each comparator)		Full range		−3.5§	−7		−3.5§	−7	mA
P_D	Total power dissipation (each comparator)		Full range		90§	150		90§	150	mW

† Full range (MIN to MAX) for TL820M is −55°C to 125°C and for the TL820C is 0°C to 70°C.

‡ The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

§ These typical values are at $T_A = 25°C$.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for TL820M, $V_O = 1.8$ V at $T_A = -55°C$, $V_O = 1.4$ V at $T_A = 25°C$, and $V_O = 1$ V at $T_A = 125°C$; for TL820C, $V_O = 1.5$ V at $T_A = 0°C$, $V_O = 1.4$ V at 25°C, and $V_O = 1.2$ V at $T_A = 70°C$. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

switching characteristics, $V_{CC+} = 12$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	$R_L = \infty$, $C_L = 5$ pF, See Note 5		30	80	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

For typical characteristic curves, see the TL810 data sheet on page 193.

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IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

TYPE uA710M
DIFFERENTIAL COMPARATOR

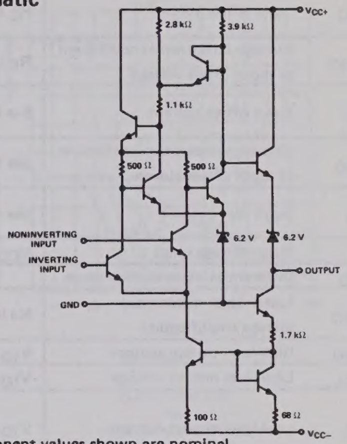
BULLETIN NO. DL-S 7612415, JUNE 1976

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with Fairchild μA710

description

The uA710 is a monolithic high-speed comparator having differential inputs and a low-impedance output. Component matching, inherent in silicon integrated circuit fabrication techniques, produces a comparator with low-drift and low-offset characteristics. This circuit is especially useful for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The uA710M is characterized for operation over the full military temperature range of –55°C to 125°C.

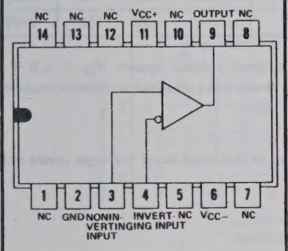
schematic


VCC+
2.8 kΩ
3.9 kΩ
1.1 kΩ
500 Ω
500 Ω
NONINVERTING INPUT
INVERTING INPUT
6.2 V
6.2 V
OUTPUT
GND
1.7 kΩ
100 Ω
68 Ω
VCC–

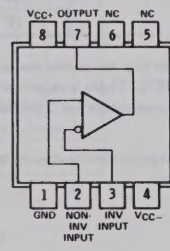
Component values shown are nominal.

terminal assignments

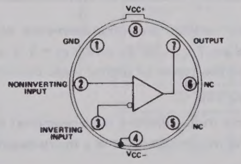
J
DUEL-IN-LINE
PACKAGE (TOP VIEW)


NC 14
NC 13
NC 12
VCC+ 11
NC 10
OUTPUT 9
NC 8
1 NC
2 GND
3 NONINVERTING INPUT
4 INVERT INPUT
5 NC
6 VCC–
7 NC

JG
DUEL-IN-LINE
PACKAGE (TOP VIEW)

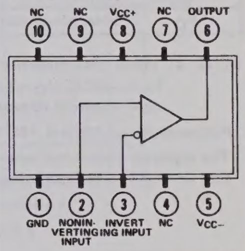

VCC+ 8
OUTPUT 7
NC 6
NC 5
1 GND
2 NON-INV INPUT
3 INV INPUT
4 VCC–

L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
8
GND
1
OUTPUT
7
NONINVERTING INPUT
2
6
NC
INVERTING INPUT
3
5
NC
4
VCC–

PIN ④ IS IN ELECTRICAL CONTACT WITH CASE.

U FLAT PACKAGE
(TOP VIEW)


NC ⑩
NC ⑨
VCC+ ⑧
NC ⑦
OUTPUT ⑥
① GND
② NONINVERTING INPUT
③ INVERT INPUT
④ NC
⑤ VCC–

NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	14 V
Supply voltage V_{CC-} (see Note 1)	–7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input, see Note 1)	±7 V
Peak output current ($t_w \leqslant 1$ s)	10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature	300 mW
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds	300°C

NOTES:
1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$,	See Note 4	25°C		0.6	2	mV
				Full range			3	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 50\ \Omega$,	See Note 4	Full range		3	10	μV/°C
I_{IO}	Input offset current	See Note 4		25°C		0.75	3	μA
				Full range			7	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4		−55°C to 25°C		5	25	nA/°C
				25°C to 125°C		15	75	
I_{IB}	Input bias current	See Note 4		25°C		13	20	μA
				Full range			45	
V_I	Input voltage range	$V_{CC-} = -7$ V		25°C	±5			V
V_{ID}	Differential input voltage range			25°C	±5			V
A_{VD}	Large-signal differential voltage amplification	No load,	See Note 4	25°C	1250	1700		
				Full range	1000			
V_{OH}	High-level output voltage	V_{ID} = 5 mV,	$I_{OH} = -5$ mA	25°C	2.5	3.2	4	V
V_{OL}	Low-level output voltage	$V_{ID} = -5$ mV,	$I_{OL} = 0$	25°C	−1	−0.5	6‡	V
I_{OL}	Low-level output current	$V_{ID} = -5$ mV,	$V_O = 0$	25°C	2	2.5		mA
				−55°C	1	2.3		
				125°C	0.5	1.7		
r_o	Output resistance	$V_O = 1.4$ V		25°C		200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$		25°C	80	100		dB
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -5$ V to 5 V		25°C		5.2	9	mA
I_{CC-}	Supply current from V_{CC-}	(−10 mV for typ),		25°C		−4.6	−7	mA
P_D	Total power dissipation	No load		25°C		90	150	mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Full range for uA710M is −55°C to 125°C.

‡The algebraic convention where the more-positive (less-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	No load,	See Note 5	40	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

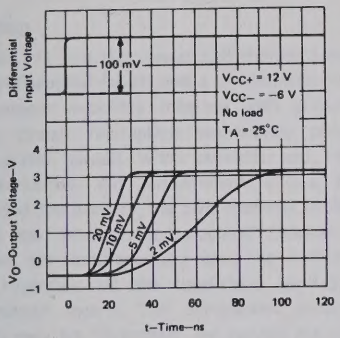


FIGURE 1

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

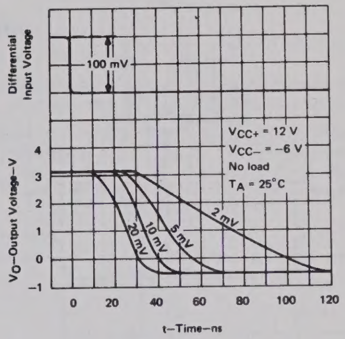


FIGURE 2

COMMON-MODE PULSE RESPONSE
vs
ELAPSED TIME

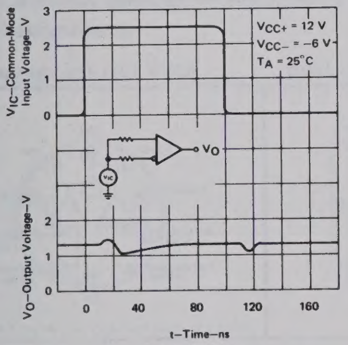


FIGURE 3

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

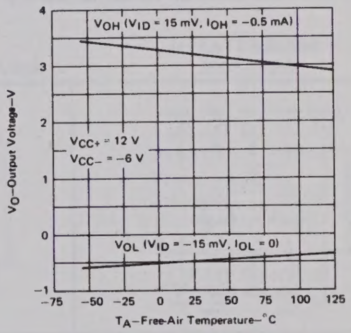


FIGURE 4

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

VOLTAGE TRANSFER CHARACTERISTICS

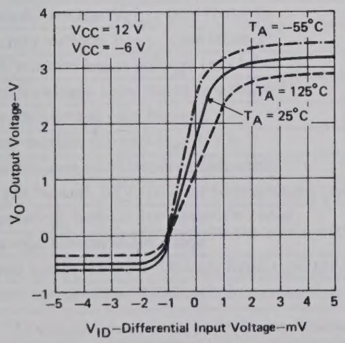


FIGURE 5

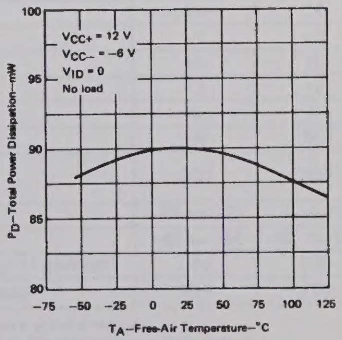


FIGURE 6

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TYPES uA711M, uA711C DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

BULLETIN NO. DL-S 7611442, FEBRUARY 1971—REVISED JUNE 1976

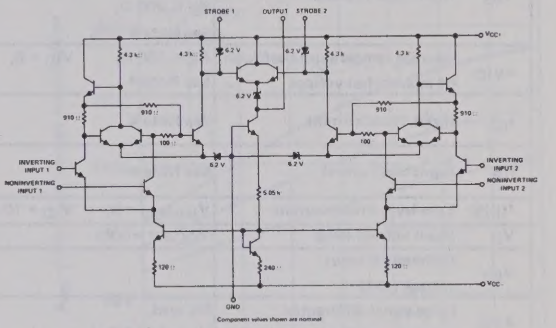
FORMERLY SN52711, SN72711

- Fast Response Times
- Low Offset Characteristics
- Output Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with Fairchild μA711 and μA711C

description

The uA711 is a high-speed dual-channel comparator with differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low-drift and low-offset characteristics. An independent strobe input is provided for each of the two channels, which when taken low, inhibits the associated channel. If both strobes are simultaneously low, the output will be low regardless of the conditions applied to the differential inputs. The comparator output pulse width may be "stretched" by varying the capacitive loading. These dual comparators are particularly useful for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage. The uA711M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA711C is characterized for operation from 0°C to 70°C.

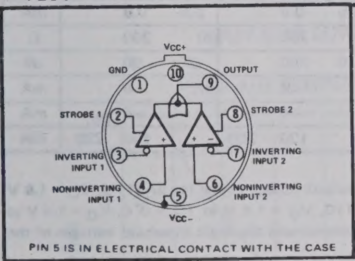
schematic


STROBE 1
OUTPUT
STROBE 2
VCC+
4.3 kΩ
4.3 kΩ
6.2 V
6.2 V
4.3 k
4.3 k
6.2 V
910 Ω
910 Ω
910
910 Ω
100 Ω
100
6.2 V
6.2 V
INVERTING INPUT 1
NONINVERTING INPUT 1
INVERTING INPUT 2
NONINVERTING INPUT 2
5.05 k
120 Ω
240 Ω
120 Ω
VCC−
GND

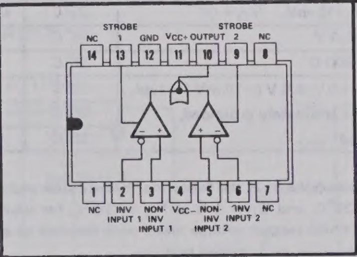
Component values shown are nominal

terminal assignments

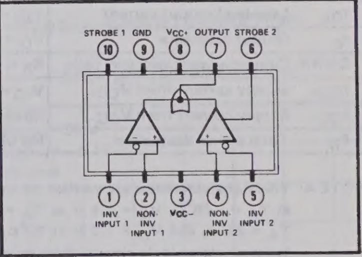
L
PLUG-IN PACKAGE (TOP VIEW)


VCC+
GND
OUTPUT
STROBE 1
STROBE 2
INVERTING INPUT 1
INVERTING INPUT 2
NONINVERTING INPUT 1
NONINVERTING INPUT 2
VCC−
1
2
3
4
5
6
7
8
9
10
PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
STROBE 1
GND
VCC+
OUTPUT
STROBE 2
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
INV INPUT 1
NON-INV INPUT 1
VCC−
NON-INV INPUT 2
INV INPUT 2
NC

U FLAT PACKAGE
(TOP VIEW)


STROBE 1
GND
VCC+
OUTPUT
STROBE 2
10
9
8
7
6
1
2
3
4
5
INV INPUT 1
NON-INV INPUT 1
VCC−
NON-INV INPUT 2
INV INPUT 2

NC—No Internal Connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA711M	uA711C	UNIT
Supply voltage V_{CC+} (see Note 1)		14	14	V
Supply voltage V_{CC-} (see Note 1)		−7	−7	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (any input, see Note 1)		±7	±7	V
Strobe voltage (see Note 1)		6	6	V
Peak output current ($t_w \leq 1$ s)		50	50	mA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)		300	300	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, L, or U package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. For operation of uA711M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

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TYPES uA711M, uA711C
DUAL-CHANNEL DIFFERENTIAL COMPARATORS WITH STROBES

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		uA711M			uA711C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \leq 200\ \Omega$, $V_{IC} = 0$, See Note 4	25°C		1	3.5		1	5	mV
			Full range			4.5			6	
		$R_S \leq 200\ \Omega$, See Note 4	25°C		1	5		1	7.5	
			Full range			6			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S \leq 200\ \Omega$, $V_{IC} = 0$, See Note 4	Full range		5			5		µV/°C
I_{IO}	Input offset current	See Note 4	25°C		0.5	10		0.5	15	µA
			Full range			20			25	
I_{IB}	Input bias current	See Note 4	25°C		25	75		25	100	µA
			Full range			150			150	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)} = 0$, $V_{ID} = 10$ mV	25°C		−1.2	−2.5		−1.2	−2.5	mA
V_I	Input voltage range	$V_{CC-} = -7$ V	25°C	±5			±5			V
V_{ID}	Differential input voltage range		25°C	±5			±5			V
A_{VD}	Large-signal differential voltage amplification	No load, $V_O = 0$ to 2.5 V	25°C	750	1500		700	1500		
			Full range	500			500			
V_{OH}	High-level output voltage	$V_{ID} = 10$ mV, $I_{OH} = 0$	25°C		4.5	5		4.5	5	V
		$V_{ID} = 10$ mV, $I_{OH} = -5$ mA	25°C	2.5	3.5		2.5	3.5		
V_{OL}	Low-level output voltage	$V_{ID} = -10$ mV, $I_{OL} = 0$	25°C	−1	−0.5	0‡	−1	−0.5	0‡	V
		$V_{ID} = 10$ mV, $V_{(strobe)} = 0.3$ V, $I_{OL} = 0$	25°C	−1		0‡	−1		0‡	
I_{OL}	Low-level output current	$V_{ID} = -10$ mV, $V_O = 0$	25°C	0.5	0.8		0.5	0.8		mA
r_o	Output resistance	$V_O = 1.4$ V	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 200\ \Omega$	25°C	70	90		65	90		dB
I_{CC+}	Supply current from V_{CC+}	$V_{ID} = -5$ V to 5 V (−10 mV for typ), Strobes alternately grounded, No load	25°C		9			9		mA
I_{CC-}	Supply current from V_{CC-}		25°C		−4			−4		mA
P_D	Total power dissipation		25°C		130	200		130	230	mW

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for uA711M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for uA711C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

†Unless otherwise noted, all characteristics are measured with the strobe of the channel under test open. The strobe of the other channel is grounded. Full range for uA711M is −55°C to 125°C and for the uA711C is 0°C to 70°C.

‡The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		uA711M			uA711C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Response time	No load,	See Note 5		40	80		40		ns
Strobe release time	No load,	See Note 6		7	25		7		ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4 V level.

TYPICAL CHARACTERISTICS

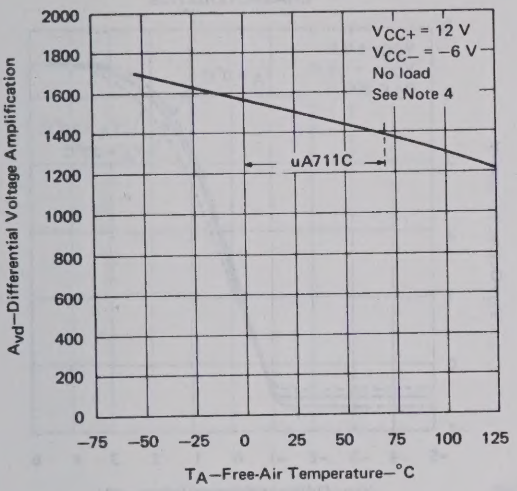
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

FIGURE 1

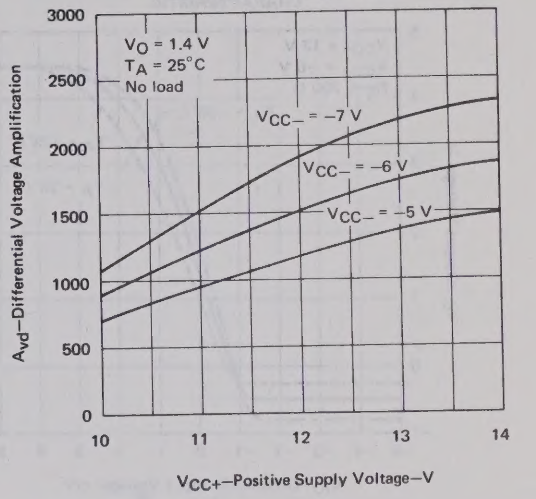
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

FIGURE 2

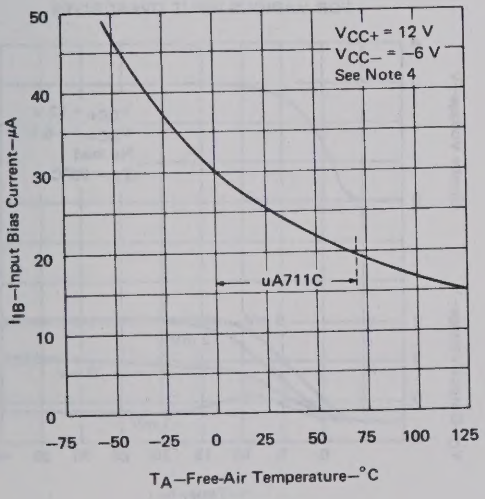
INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

FIGURE 3

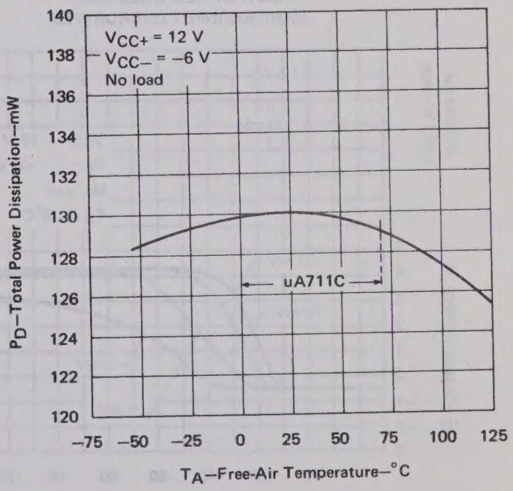
TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

FIGURE 4

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: for uA711M, V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C; for uA711C, V_O = 1.5 V at T_A = 0°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1.2 V at 70°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits these comparators are intended to drive.

TYPICAL CHARACTERISTICS

uA711M

VOLTAGE TRANSFER CHARACTERISTIC

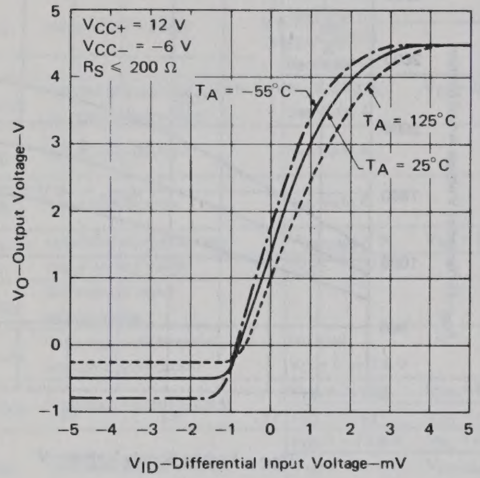

FIGURE 5

uA711C

VOLTAGE TRANSFER CHARACTERISTICS

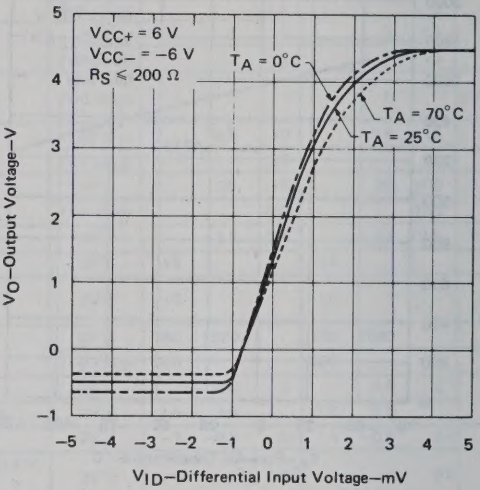

FIGURE 6

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

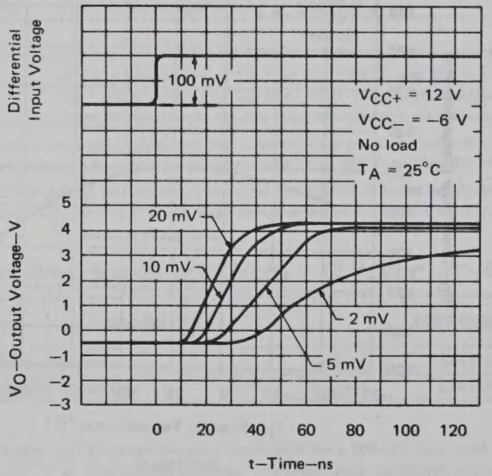

FIGURE 7

STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

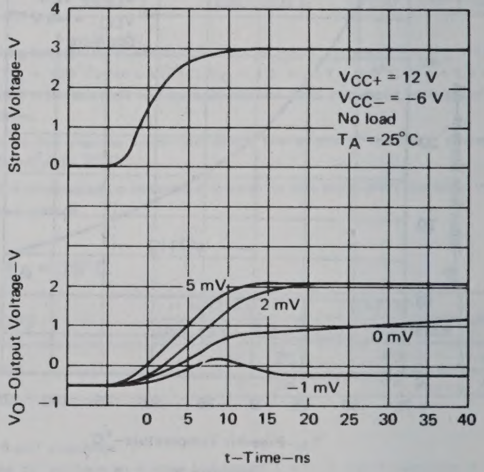

FIGURE 8

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Voltage Regulators

VOLTAGE REGULATOR SELECTION GUIDE

VOLTAGE REGULATORS

adjustable voltage regulators

		POSITIVE				NEGATIVE	SWITCHING	UNIT
		LM105	uA723	LM117	LM376	LM104	TL497	
Output voltage	MIN	4.5	2	1.2	5	−0.15	±1.2	V
	MAX	40	37	40	37	−40	+30, −25	
Input voltage	MIN	8.5	9.5	3.7	9	−8	4.5	V
	MAX	50	40	40	40	−50	15	
Input-to-output voltage difference, minimum		3	3	2.5	3	−0.5	0	V
Output current, maximum		12	150	1500	25	20	500	mA
Standby current, maximum		2	3.5	5	2.5	5	11	mA

adjustable shunt regulator

	Reference Input Voltage TYP	Temperature Coefficient of V_{ref} TYP	Differential Regulator Resistance TYP	Reference Input Current MAX	Regulator Current Range
TL430	2.75 V	100 ppm/°C	1.5 Ω	10 μA	0.5 mA to 100 mA

fixed voltage regulators

		POSITIVE				NEGATIVE		UNIT
		LM109	uA78XX SERIES	uA78MXX SERIES	uA78LXX SERIES	uA79XX SERIES	uA79MXX SERIES	
Nominal output voltage		5	SEE LISTING BELOW FOR OUTPUT VOLTAGES AVAILABLE					V
Input voltage	MIN	8	SEE INDIVIDUAL DATA SHEETS					V
	MAX	50						
Input-to-output voltage differential, minimum		2	2	2	1.7	1.1	1.1	V
Output current, maximum		500	1500	500	100	1500	500	mA
Standby current		10	8	6	6.5	3	†	mA

†2 mA to 3.5 mA, depending on individual type

AVAILABLE OUTPUT VOLTAGES	2.6 V	5 V	6 V	6.2 V	8 V	8.5 V	12 V	15 V	18 V	20 V	24 V
uA78XX SERIES		●	●		●	●	●	●	●		●
uA78MXX SERIES		●	●		●		●	●		●	●
uA78LXX SERIES	●	●		●	●		●	●			
uA79XX SERIES (−)		●	●		●	●	●	●	●		●
uA79MXX SERIES (−)		●	●		●		●	●		●	●

GLOSSARY
VOLTAGE-REGULATOR TERMS AND DEFINITIONS

SERIES REGULATORS

Input Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in input voltage from one level to another level.

NOTE: Sometimes this characteristic is normalized with respect to the input voltage change.

Ripple Rejection

The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

NOTE: This is the reciprocal of ripple sensitivity.

Ripple Sensitivity

The ratio of the peak-to-peak output ripple voltage, sometimes expressed as a percentage of output voltage, to the peak-to-peak input ripple voltage.

NOTE: This is the reciprocal of ripple rejection.

Output Regulation

The change in output voltage, often expressed as a percentage of output voltage, for a change in load current from one level to another level.

Output Resistance

The output resistance under small-signal conditions.

Temperature Coefficient of Output Voltage (α_{VO})

The ratio of the change in output voltage, usually expressed as a percentage of output voltage, to the change in temperature. This is the average value for the total temperature change.

$$\alpha_{VO} = \pm \left[\frac{V_O \text{ at } T_2 - V_O \text{ at } T_1}{V_O \text{ at } 25^\circ\text{C}}\right] \frac{100\%}{T_2 - T_1}$$

Output Voltage Change with Temperature

The percentage change in the output voltage for a change in temperature. This is the net change over the total temperature range.

Output Voltage Long-Term Drift

The change in output voltage over a long period of time.

Output Noise Voltage

The rms output noise voltage, sometimes expressed as a percentage of the dc output voltage, with constant load and no input ripple.

Current-Limit Sense Voltage

The current-sense voltage at wich current limiting occurs.

GLOSSARY
VOLTAGE-REGULATOR TERMS AND DEFINITIONS

Current-Sense Voltage

The voltage that is a function of the load current and is normally used for control of the current-limiting circuitry.

Dropout Voltage

The low input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage

The voltage that is a function of the output voltage and is used for feedback control of the regulator.

Reference Voltage

The voltage that is compared with the feedback sense voltage to control the regulator.

Bias Current

The differance between input and output current.
NOTE: This is sometimes referred to as quiescent current.

Standby Current

The input current drawn by the regulator with no output load and no reference voltage load.

Short-Circuit Output Current

The output current of the regulator with the output shorted to ground.

Peak Output Current

The maximum output current that can be obtained from the regulator due to limiting circuitry within the regulator.

SHUNT REGULATORS

NOTE: These terms and symbols are based on JEDEC and IEC standards for voltage regulator diodes.

Shunt Regulator

A device having a voltage-current characteristic similar to that of a voltage-regulator diode; normally biased to operate in a region of low differential resistance (corresponding to the breakdown region of a regulator diode) to develop across its terminals an essentially constant voltage throughout a specified current range.

Anode

The electrode to which the regulator current flows within the regulator when it is biased for regulation.

Cathode

The electrode from which the regulator current flows within the regulator when it is biased for regulation.

GLOSSARY
VOLTAGE-REGULATOR TERMS AND DEFINITIONS

Reference Input Voltage (V_{ref}) (of an adjustable shunt regulator)

The voltage at the reference input terminal with respect to the anode terminal.

Temperature Coefficient of Reference Voltage (αV_{ref})

The ratio of the change in reference voltage to the change in temperature. This is the average value for the total temperature change.

To obtain a value in ppm/°C:

$$\alpha V_{ref} = \left[\frac{V_{ref} \text{ at } T_2 - V_{ref} \text{ at } T_1}{V_{ref} \text{ at } 25^\circ C} \right] \frac{10^6}{T_2 - T_1}$$

Regulator Voltage (V_Z)

The dc voltage across the regulator.

Regulator Current (I_Z)

The dc current through the regulator when it is biased for regulation.

Regulator Current near Lower Knee of Regulation Range (I_{ZK})

The regulator current near the lower limit of the region within which regulation occurs; this corresponds to the breakdown knee of a regulator diode.

Regulator Current at Maximum Limit of Regulation Range (I_{ZM})

The regulator current above which the differential resistance of the regulator significantly increases.

Differential Regulator Resistance (r_z)

The quotient of a change in voltage across the regulator and the corresponding change in current through the regulator when it is biased for regulation.

Noise Volage (V_{nz})

The rms noise voltage with the regulator biased for regulation and with no input ripple.

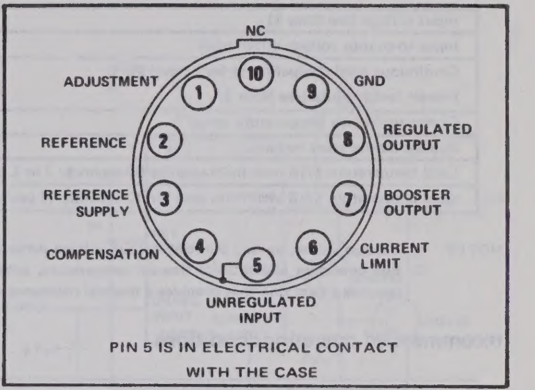
TYPES LM104, LM204, LM304
NEGATIVE-VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612052, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52104, SN72104

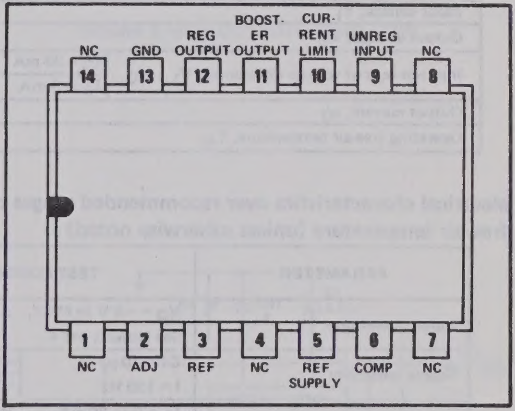
- Typical Load Regulation . . . 1 mV
- Typical Input Regulation . . . 0.06%
- Designed to be Interchangeable with National Semiconductor LM104, LM204, and LM304 Respectively

L PLUG-IN PACKAGE
(TOP VIEW)


NC
10
ADJUSTMENT
1
GND
9
REFERENCE
2
8
REGULATED OUTPUT
REFERENCE SUPPLY
3
7
BOOSTER OUTPUT
COMPENSATION
4
6
CURRENT LIMIT
5
UNREGULATED INPUT

PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
GND
REG OUTPUT
BOOSTER OUTPUT
CURRENT LIMIT
UNREG INPUT
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
ADJ
REF
NC
REF SUPPLY
COMP
NC

NC—No internal connection

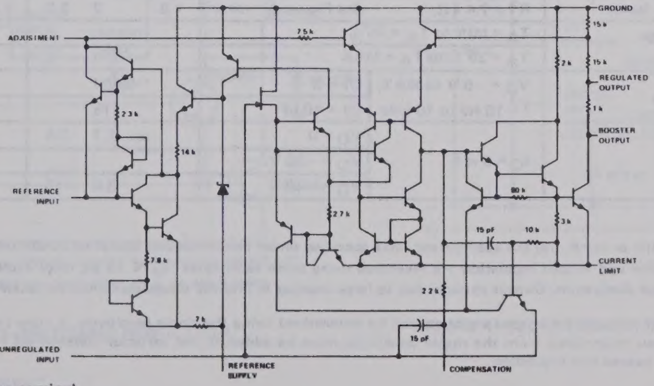
description

The LM104, LM204, and LM304 are monolithic integrated circuit voltage regulators that can be programmed with a single external resistor to provide any voltage between −40 volts and approximately 0 volts while operating from a single unregulated negative supply. When used with a separate floating bias supply, these devices can provide regulation with the output voltage limited only by the breakdown characteristics of the external pass transistors.

Although designed primarily for application as linear series regulators at output currents up to 25 milliamperes, the LM104, LM204, and LM304 can be used as current regulators, switching regulators, or control elements with the output current limited by the capability of the external pass transistors. The improvement factor for load regulation is approximately equal to the composite current gain of the added transistors. The devices can be used in either constant-current or fold-back current-limiting applications.

The LM104 is characterized for operation over the full military temperature range of −55°C to 125°C; the LM204 is characterized for operation from −25°C to 85°C; and the LM304 is characterized for operation from 0°C to 70°C.

schematic


ADJUSTMENT
REFERENCE INPUT
UNREGULATED INPUT
REFERENCE SUPPLY
COMPENSATION
GROUND
REGULATED OUTPUT
BOOSTER OUTPUT
CURRENT LIMIT
7.5 k
2.3 k
14 k
7.8 k
7 k
2.7 k
2.2 k
15 pF
15 pF
10 k
80 k
3 k
2 k
15 k
15 k
1 k

Component values shown are nominal.
Resistor values are in ohms.

TYPES LM104, LM204, LM304 NEGATIVE-VOLTAGE REGULATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM104	LM204	LM304	UNIT
Input voltage (see Note 1)		−50	−50	−40	V
Input-to-output voltage differential		−50	−50	−40	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J or N package	1000	1000	1000	mW
	L package	800	800	800	
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J or L package		300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260	260	260	°C

NOTES: 1. Voltage values, except input-to-output voltage differential, are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

recommended operating conditions

		LM104		LM204		LM304		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I		−8	−50	−8	−50	−8	−40	V
Output voltage, V_O		−0.015	−40	−0.015	−40	−0.035	−30	V
Input-to-output voltage differential, $V_I - V_O$	I_O = 20 mA	−2	−50	−2	−50	−2	−40	V
	$I_O \leq$ 5 mA	−0.5	−50	−0.5	−50	−0.5	−40	
Output current, I_O			20		20		20	mA
Operating free-air temperature, T_A		−55	125	−25	85	0	70	°C

electrical characteristics over recommended ranges of input and output voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		LM104, LM204			LM304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	V_O = −5 V to MAX, ΔV_I = 0.1 V_I, See Notes 3 and 4			0.06	0.1		0.06	0.1	%
Ripple sensitivity	C1 = 10 μF,	V_I = −15 V to MAX		0.2	0.5		0.2	0.5	mV/V
	f = 120 Hz	V_I = −7 V to −15 V		0.5	1		0.5	1	
Output regulation	I_O = 0 to 20 mA, R_{SC} = 15 Ω, See Note 3			1	5		1	5	mV
Output voltage scale factor	R1 = 2.4 kΩ,	See Figure 2	1.8	2	2.2	1.8	2	2.2	V/kΩ
Output voltage change with temperature	T_A = MIN to T_A = 25°C				1			1	%
	T_A = 25°C to T_A = MAX				1			1	
Output noise voltage	V_O = −5 V to MAX,	C1 = 0		0.007			0.007		%
	f = 10 Hz to 10 kHz	C1 = 10 μF		15			15		μV
Bias current	I_O = 5 mA	V_O = 0		1.7	2.5		1.7	2.5	mA
		V_O = −30 V					3.6	5	
		V_O = −40 V		3.6	5				

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Input regulation and output regulation are measured using pulse techniques ($t_w \leq 10\ \mu s$, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltages due to large changes in internal dissipation must be taken into account separately.

4. At zero output voltage, the output variation can be determined using the ripple sensitivity. At low voltages (i.e., 0 to −5 V), the output variation determined from the ripple sensitivity must be added to the variation determined from the input regulation to determine the overall line regulation.

TYPICAL APPLICATION DATA

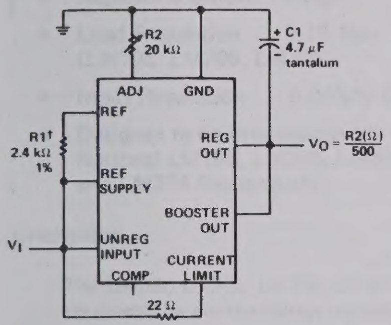

R2
20 kΩ
+ C1
4.7 μF
tantalum
ADJ
GND
REF
R1†
2.4 kΩ
1%
REG
OUT
$V_O = \frac{R2(\Omega)}{500}$
REF
SUPPLY
BOOSTER
OUT
V_I
UNREG
INPUT
CURRENT
COMP
LIMIT
22 Ω

FIGURE 1–BASIC REGULATOR CIRCUIT

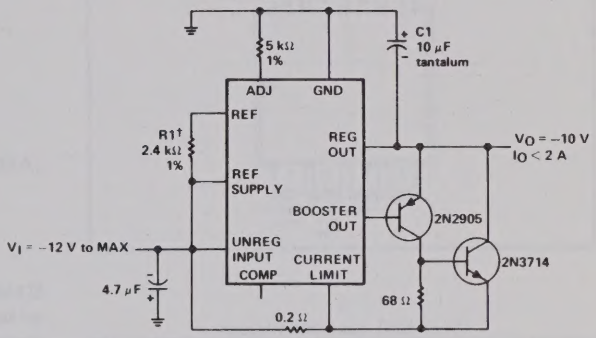
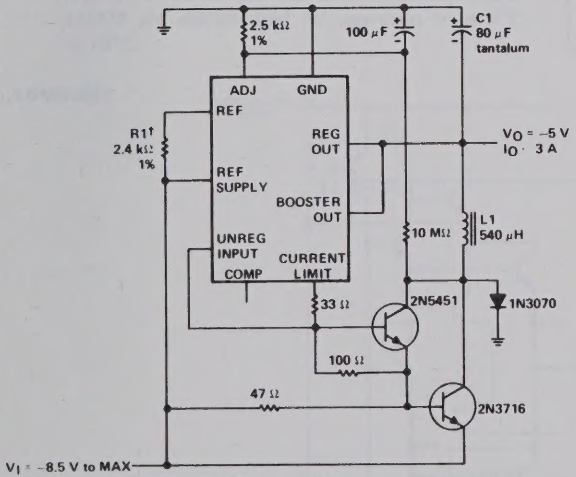

5 kΩ
1%
+ C1
10 μF
tantalum
ADJ
GND
REF
R1†
2.4 kΩ
1%
REG
OUT
$V_O = -10$ V
$I_O < 2$ A
REF
SUPPLY
BOOSTER
OUT
2N2905
UNREG
INPUT
$V_I = -12$ V to MAX
CURRENT
2N3714
COMP
LIMIT
4.7 μF
68 Ω
0.2 Ω

FIGURE 2–HIGH-CURRENT REGULATOR


2.5 kΩ
1%
100 μF
C1
80 μF
tantalum
ADJ
GND
REF
R1†
2.4 kΩ
1%
REG
OUT
$V_O = -5$ V
$I_O \cdot 3$ A
REF
SUPPLY
BOOSTER
OUT
L1
540 μH
10 MΩ
UNREG
INPUT
CURRENT
COMP
LIMIT
33 Ω
2N5451
1N3070
100 Ω
47 Ω
2N3716
$V_I = -8.5$ V to MAX

L1: 60 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core, or equivalent

FIGURE 3–SWITCHING REGULATOR

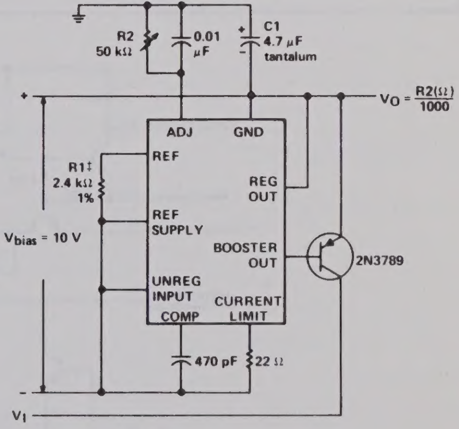

R2
50 kΩ
0.01
μF
C1
4.7 μF
tantalum
+
$V_O = \frac{R2(\Omega)}{1000}$
ADJ
GND
REF
R1‡
2.4 kΩ
1%
REG
OUT
REF
SUPPLY
$V_{bias} = 10$ V
BOOSTER
OUT
2N3789
UNREG
INPUT
CURRENT
COMP
LIMIT
470 pF
22 Ω
–
V_I

FIGURE 4–OPERATING WITH SEPARATE BAIS SUPPLY

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†Trim R1 for exact scale factor.

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ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

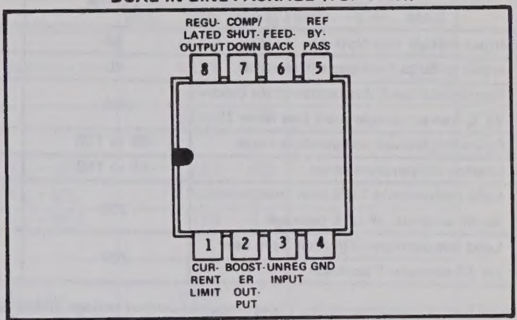
TYPES LM105, LM205, LM305, LM305A, LM376
POSITIVE-VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612057, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52105, SN72305, SN72305A, SN72376

- Low Standby Current . . . 0.8 mA Typ
- Adjustable Output Voltage
- Load Regulation . . . 0.1% Max (LM105, LM205, LM305)
- Input Regulation . . . 0.06%/V Max
- Designed to be Interchangeable with National LM105, LM205, LM305, LM305A, and LM376 Respectively

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)

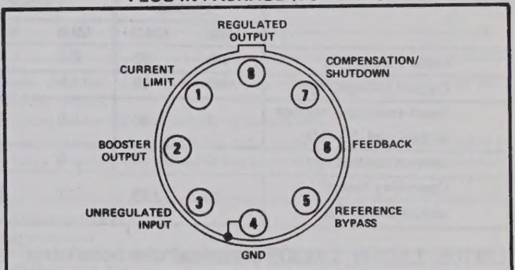

REGU-LATED OUTPUT
COMP/SHUT-DOWN
FEED-BACK
REF BY-PASS
8
7
6
5
1
2
3
4
CUR-RENT LIMIT
BOOST-ER OUT-PUT
UNREG INPUT
GND

description

The LM105, LM205, LM305, LM305A and LM376 are monolithic positive-voltage regulators designed for a wide range of applications from digital power supplies to precision regulators for analog systems. These devices will not oscillate under conditions of varying resistive and reactive loads and will start reliably with any load within the rating of the circuits.

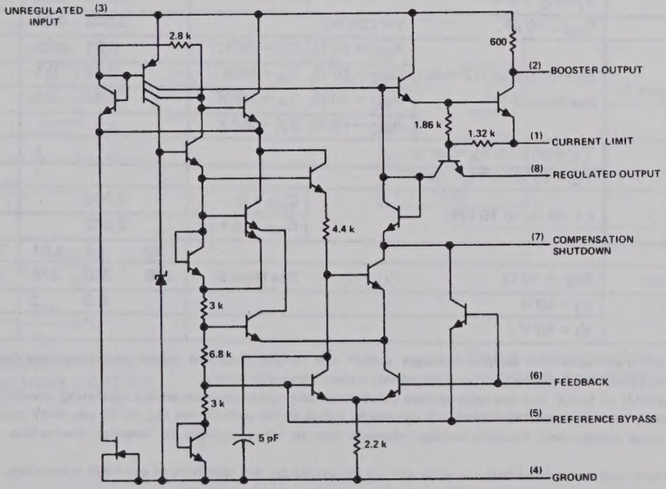
The LM105 is characterized for operation over the full military temperature range of −55°C to 125°C; the LM205 is characterized for operation from −25°C to 85°C, and the LM305, LM305A, and LM376 are characterized for operation from 0°C to 70°C.

L
PLUG-IN PACKAGE (TOP VIEW)


REGULATED OUTPUT
COMPENSATION/ SHUTDOWN
CURRENT LIMIT
BOOSTER OUTPUT
FEEDBACK
UNREGULATED INPUT
REFERENCE BYPASS
GND
1
2
3
4
5
6
7
8

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

schematic


UNREGULATED INPUT (3)
2.8 k
600
(2) BOOSTER OUTPUT
1.86 k
1.32 k
(1) CURRENT LIMIT
(8) REGULATED OUTPUT
4.4 k
(7) COMPENSATION SHUTDOWN
3 k
6.8 k
3 k
5 pF
2.2 k
(6) FEEDBACK
(5) REFERENCE BYPASS
(4) GROUND

Component values shown are nominal.
Resistor values are in ohms.

TYPES LM105, LM205, LM305, LM305A, LM376
POSITIVE-VOLTAGE REGULATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM105	LM205	LM305A	LM305 LM376	UNIT
Input voltage (see Note 1)	50	50	50	40	V
Input-to-output voltage differential	40	40	40	40	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800	800	800	800	mW
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: JP or L package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260	260	260	260	°C

NOTES: 1. Voltage values, except input-to-output voltage differential, are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

recommended operating conditions

	LM105		LM205		LM305A		LM305		LM376		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	8.5	50	8.5	50	8.5	50	8.5	40	9	40	V
Output voltage, V_O	4.5	40	4.5	40	4.5	40	4.5	30	5	37	V
Input-to-output voltage differential, V_I-V_O	3	30	3	30	3	30	3	30	3	30	V
Output current, I_O	0	12	0	12	0	45	0	12	0	25	mA
Operating free-air temperature, T_A	−55	125	−25	85	0	70	0	70	0	70	°C

LM105, LM205, LM305 electrical characteristics† at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		LM105, LM205			LM305			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	$V_I-V_O \leqslant 5$ V	See Note 3		0.025	0.06		0.025	0.06	%/V
	$V_I-V_O > 5$ V			0.015	0.03		0.015	0.03	
Ripple sensitivity	C_{ref} = 10 μF,	f = 120 Hz		0.003	0.01		0.003	0.01	%/V
Output regulation (see Note 4)	I_O = 0 to I_O = 12 mA, See Note 3	R_{SC} = 10 Ω, T_A = 25°C		0.02	0.05		0.02	0.05	%
		R_{SC} = 10 Ω, T_A = MIN		0.03	0.1		0.03	0.1	
		R_{SC} = 10 Ω, T_A = MAX		0.03	0.1				
		R_{SC} = 15 Ω, T_A = MAX					0.03	0.1	
Output voltage change with temperature	T_A = MIN to T_A = 25°C				1			1	%
	T_A = 25°C to T_A = MAX				1			1	
Output noise voltage	f = 10 Hz to 10 kHz	C_{ref} = 0		0.005			0.005		%
		C_{ref} > 0.1 μF		0.002			0.002		
Feedback sense voltage			1.63	1.7	1.81	1.63	1.7	1.81	V
Current-limit sense voltage	R_{SC} = 10 Ω, V_O = 0,	See Note 5	225	300	375	225	300	375	mV
Standby current	V_I = 50 V			0.8	2				mA
	V_I = 40 V						0.8	2	

†These specifications apply for input and output voltages within the ranges specified under recommended operating conditions and for a divider impedance of 2 kΩ presented to the feedback terminal, unless otherwise noted.

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Input regulation and output regulation are measured using pulse techniques ($t_W \leqslant 10$ μs, duty cycle $\leqslant 5\%$) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

4. Load regulation and output current capacity can be improved by the addition of external transistors. The improvement factor will be approximately equal to the composite current gain of the added transistors.

5. Current-limit sense voltage is measured without an external pass transistor.

LM305A, LM376 electrical characteristics[†] at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS[‡]			LM305A MIN	LM305A TYP	LM305A MAX	LM376 MIN	LM376 TYP	LM376 MAX	UNIT
Input regulation	$V_I - V_O \leq 5$ V		See Note 3		0.025	0.06			0.03	%/V
	$V_I - V_O > 5$ V				0.015	0.03			0.03	
	T_A = 0°C to 70°C								0.1	
Ripple sensitivity	C_{ref} = 10 µF,	f = 120 Hz			0.003					%/V
	f = 120 Hz								0.1	
Output regulation (see Note 4)	I_O = 0 to I_O = MAX, See Note 3	R_{SC} = 0 Ω, T_A = 25°C			0.02	0.2			0.2	%
		R_{SC} = 0 Ω, T_A = 0°C			0.03	0.4			0.5	
		R_{SC} = 0 Ω, T_A = 70°C			0.03	0.4			0.5	
Output voltage change with temperature	T_A = 0°C to T_A = 25°C					1			1	%
	T_A = 25°C to T_A = 70°C					1			1	
Output noise voltage	f = 10 Hz to 10 kHz		C_{ref} = 0		0.005					%
			$C_{ref} > 0.1$ µF		0.002					
Feedback sense voltage				1.55	1.7	1.85				V
	T_A = 0°C to T_A = 70°C						1.6	1.7	1.8	
Current limit sense voltage	R_{SC} = 10 Ω,	V_O = 0 V,	See Note 5	225	300	375		300		mV
Standby current	V_I = 50 V				0.8	2				mA
	V_I = 30 V								2.5	

[†] These specifications apply for input and output voltages within the ranges specified under recommended operating conditions, and for a divider impedance of 2 kΩ presented to the feedback terminal, unless otherwise noted.

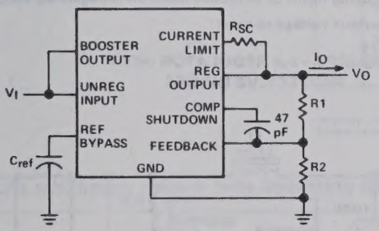
[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Input regulation and output regulation are measured using pulse techniques ($t_w \leq 10$ µs, duty cycle ≤ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

4. Load regulation and output current capacity can be improved by the addition of external transistors. The improvement factor will be approximately equal to the composite current gain of the added transistors.

5. Current-limit sense voltage is measured without an external pass transistor.

TYPICAL APPLICATION DATA


BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
RSC
IO
VO
VI
Cref
47 pF
R1
R2

$$V_O \approx 1.7 \frac{R1+R2}{R2} \text{ V}$$

$$I_{SC} \approx \frac{325}{R_{SC}} \text{ mA}$$

FIGURE 1–BASIC REGULATOR WITH CURRENT LIMITING

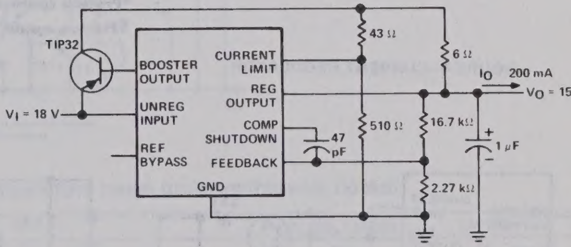

TIP32
VI = 18 V
BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
47 pF
43 Ω
6 Ω
510 Ω
16.7 kΩ
2.27 kΩ
1 µF
IO 200 mA
VO = 15 V

FIGURE 2–LINEAR REGULATOR WITH FOLDBACK CURRENT LIMITING

TYPICAL APPLICATION DATA

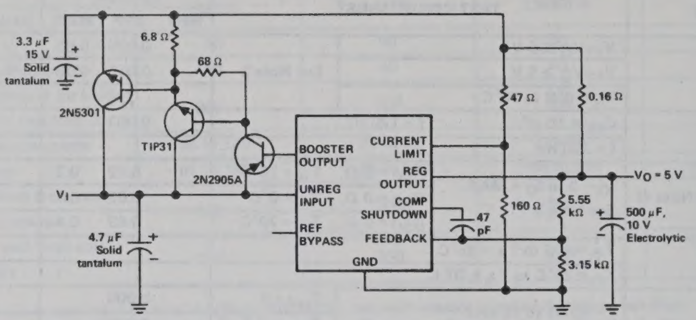

3.3 μF
15 V
Solid
tantalum
6.8 Ω
68 Ω
2N5301
TIP31
2N2905A
V_I
4.7 μF
Solid
tantalum
BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
47 pF
47 Ω
0.16 Ω
160 Ω
5.55 kΩ
3.15 kΩ
500 μF, 10 V Electrolytic
V_O = 5 V

FIGURE 3–10-A REGULATOR WITH FOLDBACK CURRENT LIMITING

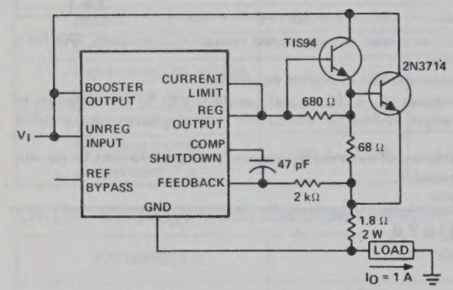
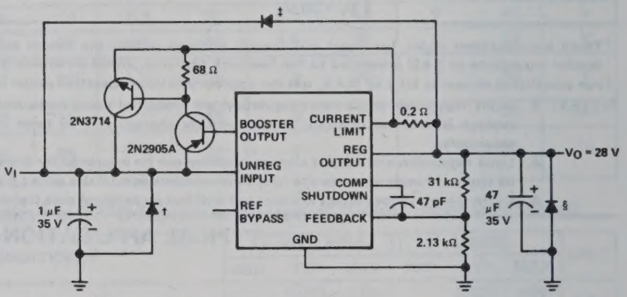

TIS94
2N3714
BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
V_I
680 Ω
68 Ω
47 pF
2 kΩ
1.8 Ω
2 W
LOAD
I_O = 1 A

FIGURE 4–CURRENT REGULATOR


‡
68 Ω
2N3714
2N2905A
V_I
1 μF
35 V
†
BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
0.2 Ω
47 pF
31 kΩ
2.13 kΩ
47 μF 35 V
§
V_O = 28 V

†Protects against input voltage reversal.

‡Protects against shorted input or inductive loads on unregulated supply.

§Protects against output voltage reversal.

FIGURE 5–1-A REGULATOR WITH PROTECTIVE DIODES

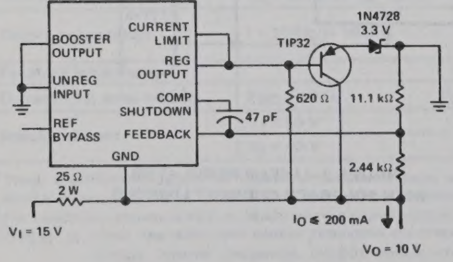

BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
TIP32
1N4728
3.3 V
620 Ω
11.1 kΩ
2.44 kΩ
47 pF
25 Ω
2 W
V_I = 15 V
I_O ≤ 200 mA
V_O = 10 V

FIGURE 6–SHUNT REGULATOR

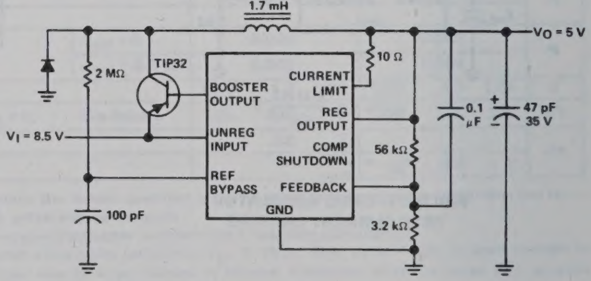

L1
1.7 mH
V_O = 5 V
2 MΩ
TIP32
V_I = 8.5 V
100 pF
BOOSTER OUTPUT
UNREG INPUT
REF BYPASS
CURRENT LIMIT
REG OUTPUT
COMP SHUTDOWN
FEEDBACK
GND
10 Ω
56 kΩ
3.2 kΩ
0.1 μF
47 pF
35 V

FIGURE 7–SWITCHING REGULATOR

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LINEAR INTEGRATED CIRCUITS

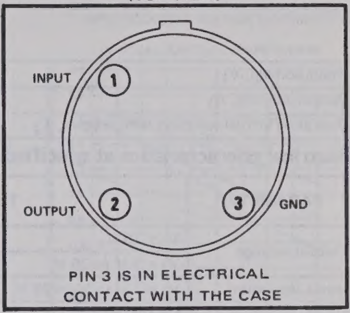
TYPES LM109, LM209, LM309 5-VOLT REGULATORS

BULLETIN NO. DL-S 7612056, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52109, SN72309

- No External Components Required for Most Applications
- Output Current . . . 500 mA Max
- Satisfies 5-V Supply Requirements of TTL and DTL
- Virtually Blow-Out Proof Due to Internal Current Limiting, Thermal Shutdown, and Safe-Operating-Area Compensation
- Designed to be Interchangeable with National LM109, LM209, and LM309 Respectively

LA PLUG-IN PACKAGE
(TOP VIEW)

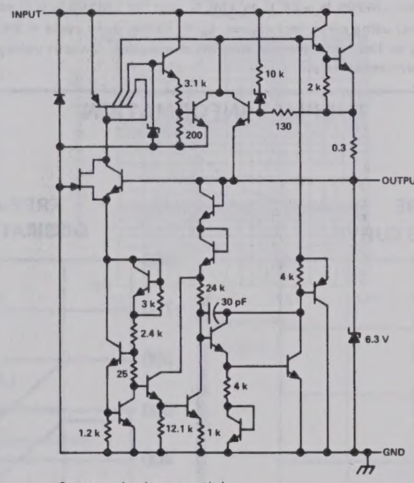


PIN 3 IS IN ELECTRICAL CONTACT WITH THE CASE

description

These monolithic 5-volt regulators are designed for use as local regulators to eliminate noise and distribution problems inherent with single-point regulation. They are specified under worst-case conditions to match the power supply requirements of TTL and DTL logic families. In other applications, these devices can be used with external components to obtain adjustable output voltages and currents or as the series-pass element in precision regulators.

schematic



Component values shown are nominal.
Resistor values are in ohms.

absolute maximum ratings over operating temperature range (unless otherwise noted)

	LM109, LM209	LM309	UNIT
Input voltage	35	35	V
Output current	500	500	mA
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	5	4	W
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	600	480	mW
Operating case or virtual junction temperature range	–55 to 150	0 to 125	°C
Storage temperature range	–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	300	300	°C

NOTES: 1. Above 25°C case temperature, derate lineary at the rate of 40 mW/° C, or refer to Dissipation Derating Curve, Figure 1.
2. Above 25°C free-air temperature, derate linearly at the rate of 4.8 mW/°C, refer to Dissipation Derating Curve, Figure 2.

recommended operating conditions

	LM109		LM209		LM309		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	7	25	7	25	7	25	V
Output current, I_O	0	500	0	500	0	500	mA
Operating virtual-junction temperature, T_J	−55	150	−25	150	0	125	°C

electrical characteristics at specified virtual junction temperature

PARAMETER	TEST CONDITIONS†			LM109, LM209			LM309			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	$V_I = 10$ V,	$I_O = 100$ mA	25°C	4.7	5.0	5.3	4.8	5.0	5.2	V
	$V_I = 7$ V to 25 V,	$I_O = 5$ mA to 200 mA	Full range	4.6		5.4	4.75		5.25	
Input regulation	$V_I = 7$ V to $V_I = 25$ V		25°C		4	50		4	50	mV
Ripple rejection	f = 120 Hz		25°C		85			85		dB
Output regulation	$I_O = 5$ mA to $I_O = 500$ mA,	See Note 3	25°C		20	50		20	50	mV
Output noise voltage	f = 10 Hz to 100 kHz		25°C		40			40		μV
Standby current	$V_I = 7$ V to 25 V		Full range		5	10		5	10	mA
Bias current change	$V_I = 7$ V to $V_I = 25$ V,	$I_O = 100$ mA	Full range			0.5			0.5	mA
	$I_O = 5$ mA to $I_O = 200$ mA					0.8			0.8	

†Full range for LM109 is −55°C to 150°C, for LM209 is −25°C to 150°C, and for LM309 is 0°C to 125°C. All characteristics, except output noise voltage and ripple rejection, are measured using pulse techniques. $t_w \leq 10$ ms, duty cycle $\leq 5\%$.

NOTE 3: Pulse techniques are used in testing to limit the average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

THERMAL INFORMATION

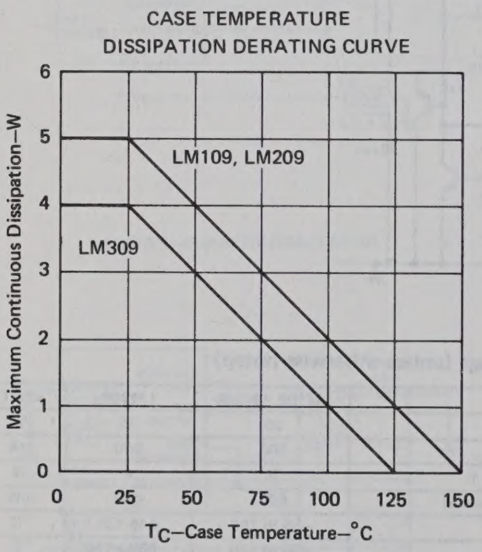


FIGURE 1

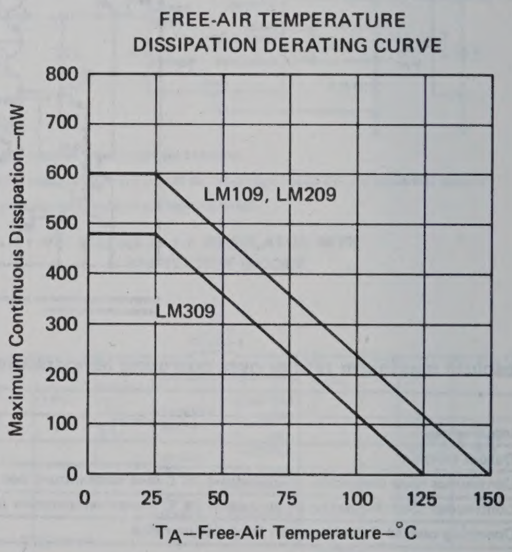


FIGURE 2

TYPICAL CHARACTERISTICS[†]

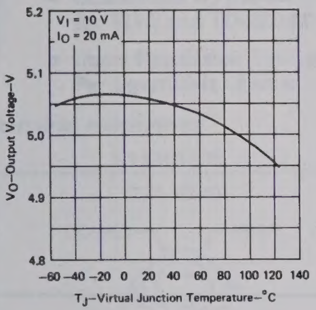

OUTPUT VOLTAGE vs VIRTUAL JUNCTION TEMPERATURE

FIGURE 3

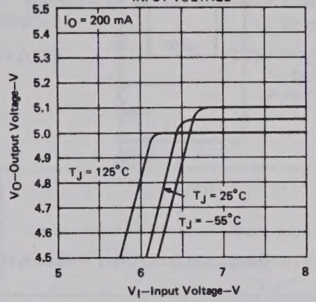

OUTPUT VOLTAGE vs INPUT VOLTAGE

FIGURE 4

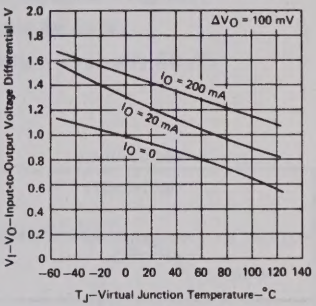

INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL vs VIRTUAL JUNCTION TEMPERATURE

FIGURE 5

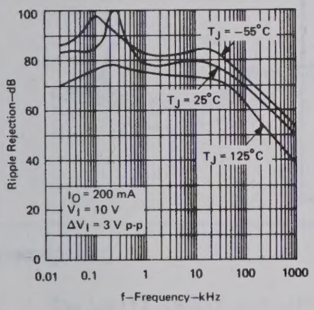

RIPPLE REJECTION vs FREQUENCY

FIGURE 6

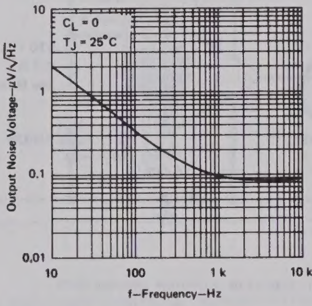

OUTPUT NOISE VOLTAGE vs FREQUENCY

FIGURE 7

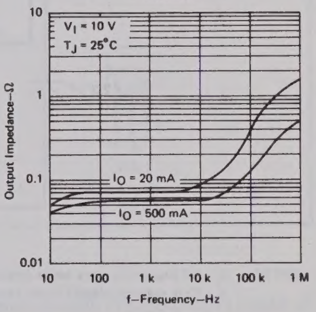

OUTPUT IMPEDANCE vs FREQUENCY

FIGURE 8

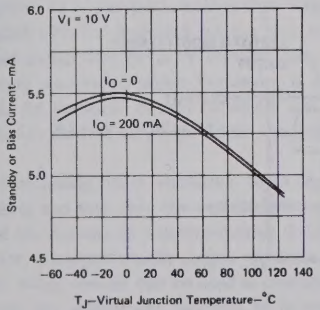

STANDBY OR BIAS CURRENT vs VIRTUAL JUNCTION TEMPERATURE

FIGURE 9

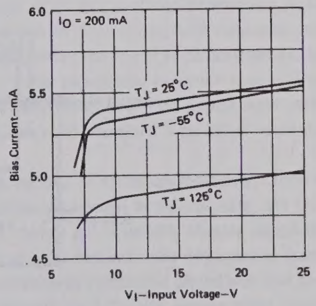
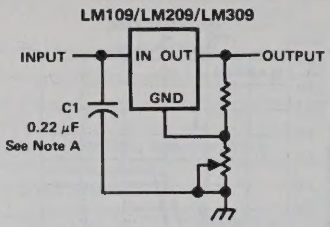

BIAS CURRENT vs INPUT VOLTAGE

FIGURE 10

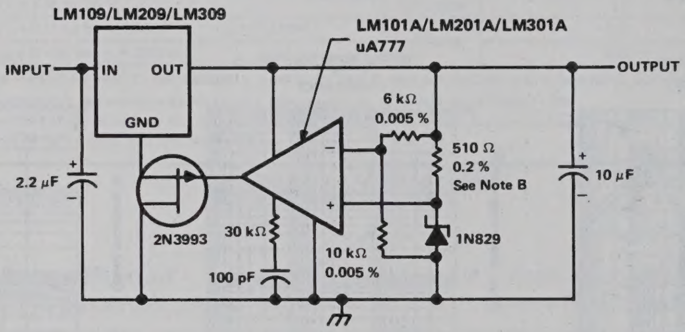
[†] **Data for virtual junction temperatures outside the ranges specified in the recommended operating conditions for LM209 or LM309 is not applicable for those types.**

TYPICAL APPLICATION DATA


LM109/LM209/LM309
INPUT
IN
OUT
OUTPUT
GND
C1
0.22 μF
See Note A

NOTE A: C1 is required if regulator is not located in close proximity to power supply filter.

FIGURE 11–ADJUSTABLE OUTPUT REGULATOR


LM109/LM209/LM309
LM101A/LM201A/LM301A
uA777
INPUT
IN
OUT
OUTPUT
GND
6 kΩ
0.005 %
510 Ω
0.2 %
See Note B
2.2 μF
10 μF
2N3993
30 kΩ
100 pF
10 kΩ
0.005 %
1N829

NOTES: A. All capacitors are solid tantalum.
B. This resistor determines zener current. Adjust to minimize thermal drift.

FIGURE 12–HIGH-STABILITY REGULATOR

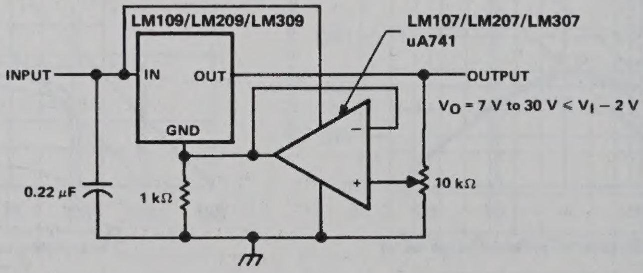

LM109/LM209/LM309
LM107/LM207/LM307
uA741
INPUT
IN
OUT
OUTPUT
$V_O = 7\ V\ to\ 30\ V < V_I - 2\ V$
GND
0.22 μF
1 kΩ
10 kΩ

FIGURE 13–HIGH-STABILITY REGULATOR WITH ADJUSTABLE OUTPUT

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FUTURE PRODUCT
TO BE ANNOUNCED

TYPES LM117, LM217, LM317
3-TERMINAL ADJUSTABLE REGULATORS

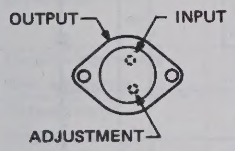
JUNE 1976

- Output Voltage Range Adjustable from 1.2 V to 37 V
- Guaranteed I_O Capability of 1.5 A for TO-3 and TO-220AB Packages
- Input Regulation Typically 0.01% Per Input-Volt Change
- Output Regulation Typically 0.1%
- Peak Output Current Constant Over Temperature Range of Regulator
- Popular 3-Lead Packages
- Ripple Rejection Typically 80 dB

terminal assignments

KA PACKAGE

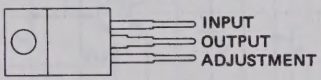
(TOP VIEW)



TO-3

KC PACKAGE

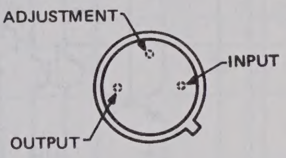
(TOP VIEW)

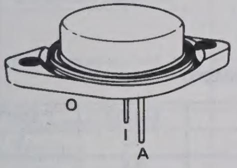


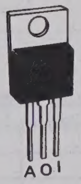
TO-220AB

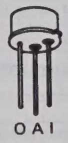
LA PACKAGE

(TOP VIEW)









description

The LM117, LM217, and LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 amperes over a range of output voltage of 1.2 volts to 37 volts. They are exceptionally easy to use and require only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators. The devices are packaged in standard transistor packages that are easily mounted and handled.

In addition to higher performance than fixed regulators, these regulators offer full overload protection available only in integrated circuits. Included on the chip are current limit, thermal overload protection, and safe-area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, these regulators are useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. It makes an especially simple adjustable switching regulator, a programmable output regulator, or, by connecting a fixed resistor between the adjustment terminal and the output, these devices can be used as precision current regulators. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2 volts where most loads draw little current.

The LM117 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM217 and LM317 are characterized for operation from −25°C to 150°C and from 0°C to 125°C respectively.

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TENTATIVE DATA SHEET
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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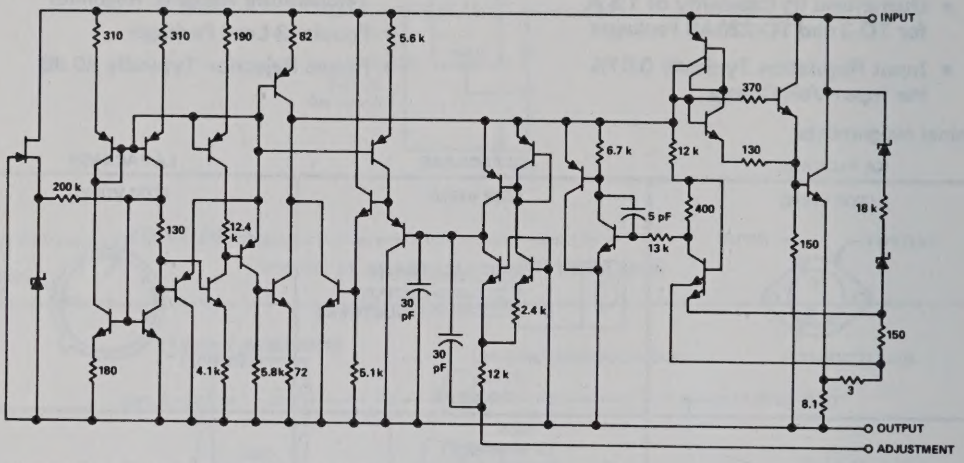
TYPES LM117, LM217, LM317
3-TERMINAL ADJUSTABLE REGULATORS

schematic



All resistors values shown are nominal and in ohms.

absolute maximum ratings over operating temperature range (unless otherwise noted)

		LM117	LM217	LM317	UNIT
Input-to-output differential voltage, $V_I - V_O$		40	40	40	V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	KA (TO-3) package	3.5	3.5	3.5	W
	KC (TO-220AB) package		2	2	
	LA package	0.6	0.6	0.6	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	KA package	20	20	20	W
	KC package		20	20	
	LA package	2	2	2	
Operating free-air, case, or virtual junction temperature range		−55 to 150	−25 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	KA and LA packages	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	KC package		260	260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Curves, Figures 1 through 4.

recommended operating conditions

		LM117		LM217		LM317		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Output current, I_O	All packages	5		5		10		mA
	KA package		1500		1500		1500	
	KC package				1500		1500	
	LA package		500		500		500	
Operating virtual junction temperature, T_J		−55	150	−25	150	0	125	°C

electrical characteristics over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		LM117, LM217			LM317			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation‡	T_J = 25°C	See Note 2		0.01	0.02		0.01	0.04	%/V
	I_O = 10 mA to MAX			0.02	0.05		0.02	0.07	
Ripple rejection	V_O = 10 V, f = 120 Hz			65			65		dB
	V_O = 10 V, f = 120 Hz, 10-μF capacitor between ADJ and ground		66	80		66	80		
Output regulation	I_O = 10 mA to MAX, T_J = 25°C, See Note 2	$V_O \leqslant 5$ V		5	15		5	25	mV
		$V_O \geqslant 5$ V		0.1	0.3		0.1	0.5	%
	I_O = 10 mA to MAX, See Note 2	$V_O \leqslant 5$ V		20	50		20	70	mV
		$V_O \geqslant 5$ V		0.3	1		0.3	1.5	%
Output voltage change with temperature	T_J = MIN to MAX			1			1		%
Output voltage long-term drift (see Note 3)	After 1000 h at T_J = MAX and $V_I - V_O$ = 40 V			0.3	1		0.3	1	%
Output noise voltage	f = 10 Hz to 10 kHz, T_J = 25°C			0.003			0.003		%
Minimum output current to maintain regulation	$V_I - V_O$ = 40 V			3.5	5		3.5	10	mA
Peak output current	$V_I - V_O \leqslant 15$ V	KA and KC packages	1.5	2.2		1.5	2.2		A
		LA package	0.5	0.8		0.5	0.8		
	$V_I - V_O \leqslant 40$ V	KA and KC packages		0.4			0.4		
		LA package		0.07			0.07		
Adjustment-terminal current				50	100		50	100	μA
Change in adjustment-terminal current	$V_I - V_O$ = 2.5 V to 40 V, I_O = 10 mA to MAX			0.2	5		0.2	5	μA
Reference voltage (output to ADJ)	$V_I - V_O$ = 3 V to 40 V, I_O = 10 mA to MAX, P ⩽ rated dissipation		1.2	1.25	1.3	1.2	1.25	1.3	V

†Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O$ = 5 V and I_O = 0.5 A for the KA (TO-3) and KC (TO-220AB) packages and I_O = 0.1 A for the LA package. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡Input regulation is expressed here as the percentage change in output voltage per 1-volt change at the input.

NOTES: 2. Input regulation and output regulation are measured using pulse techniques ($t_w \leqslant 10$ μs, duty cycle ⩽ 5%) to limit changes in average internal dissipation. Output voltage changes due to large changes in internal dissipation must be taken into account separately.

3. Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

thermal characteristics

PARAMETER	KA	KC	LA	UNIT
	MAX	MAX	MAX	
$R_{\theta JC}$ Junction-to-case thermal resistance	3	4	15	°C/W

THERMAL INFORMATION

TO-3 AND TO-220AB FREE-AIR TEMPERATURE DISSIPATION DERATING CURVES

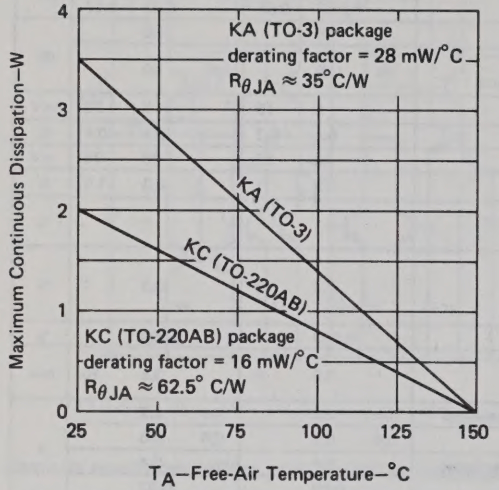


FIGURE 1

TO-3 AND TO-220AB CASE TEMPERATURE DISSIPATION DERATING CURVES

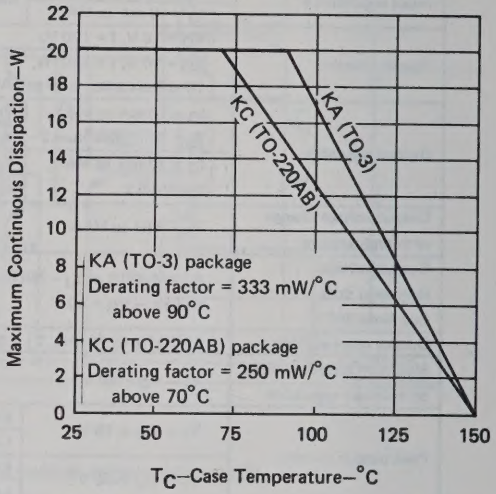


FIGURE 2

LA PACKAGE FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

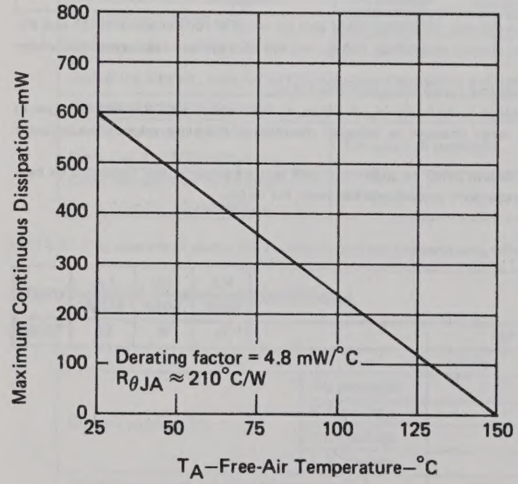


FIGURE 3

LA PACKAGE CASE TEMPERATURE DISSIPATION DERATING CURVE

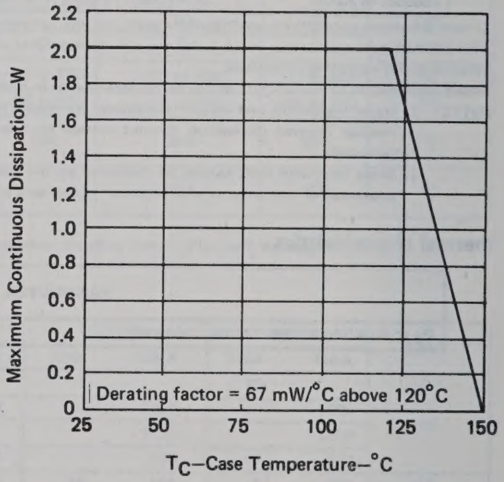


FIGURE 4

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

TYPE TL430C
ADJUSTABLE SHUNT REGULATOR

BULLETIN NO. DL-S 7612414, JUNE 1976

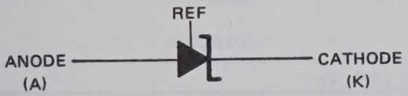
- Temperature Compensated
- Programmable Output Voltage
- Low Output Resistance
- Low Output Noise
- Sink Capability to 100 mA

description

The TL430 is a three-terminal adjustable shunt regulator featuring excellent stability over temperature, wide operating current range, and low output noise. The output voltage may be set by two external resistors to any desired value between 3 volts and 30 volts. The TL430 can replace zener diodes in many applications providing improved performance.

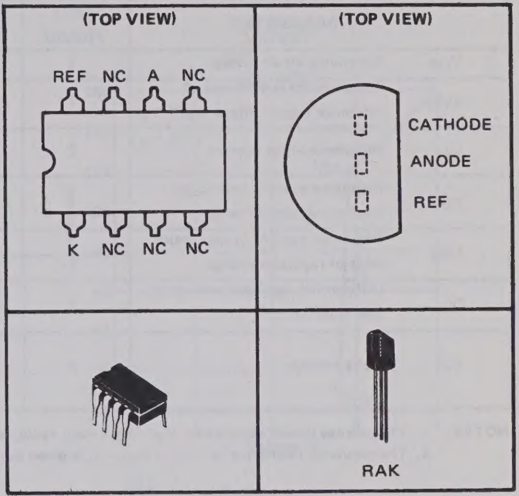
The TL430 is characterized for operation from 0°C to 70°C.

functional block diagram



JG
DUAL-IN-LINE PACKAGE

LP
SILECT† PACKAGE



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Regulator voltage (see Note 1)	30 V
Continuous regulator current	100 mA
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 2)	775 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: LP package	260°C

recommended operating conditions

	MIN	MAX	UNIT
Regulator voltage, V_Z	V_{ref}	30	V
Regulator current, I_Z	2	100	mA
Operating free-air temperature, T_A	0	70	°C

NOTES: 1. All voltage values are with respect to the anode terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

† Trademark of Texas Instruments

TENTATIVE DATA SHEET
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TYPE TL430C
ADJUSTABLE SHUNT REGULATOR

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference input voltage	1	$V_Z = V_{ref}$,	$I_Z = 10$ mA	2.5	2.75	3	V
αV_{ref}	Temperature coefficient of reference input voltage	1	$V_Z = V_{ref}$, $T_A = 0°C$ to $70°C$	$I_Z = 10$ mA,		±50		ppm/°C
I_{ref}	Reference input current	2	$I_Z = 10$ mA, $R2 = \infty$	$R1 = 10$ kΩ,		3	10	µA
I_{ZK}	Regulator current near lower knee of regulation range	1	$V_Z = V_{ref}$			0.6	2	mA
I_{ZM}	Regulator current at maximum limit of regulation range	1	$V_Z = V_{ref}$		50			mA
		2	$V_Z = 5$ V to 30 V, See Note 3		100			
r_z	Differential regulator resistance (see Note 4)	1	$V_Z = V_{ref}$, $\Delta I_Z = (52–2)$ mA			1.5	3	Ω
V_{nz}	Noise voltage	2	f = 0.1 Hz to 10 Hz	$V_Z = 3$ V		50		µV
				$V_Z = 12$ V		200		
				$V_Z = 30$ V		650		

NOTES: 3. The average power dissipation, $V_Z \cdot I_Z \cdot$ duty cycle, must not exceed 775 mW in any 10-ms interval.

4. The regulator resistance for $V_Z > V_{ref}$, r_z', is given by:

$$r_z' = r_z \left(1 + \frac{R1}{R2}\right).$$

PARAMETER MEASUREMENT INFORMATION

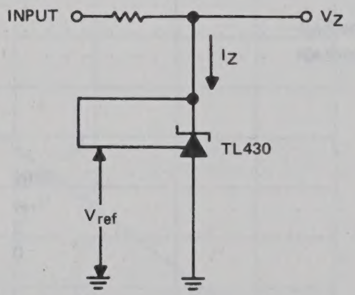
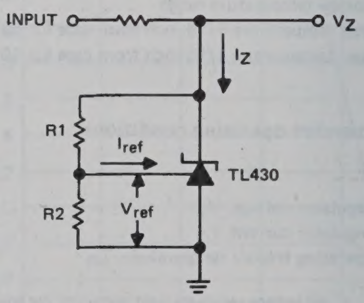


FIGURE 1–TEST CIRCUIT FOR $V_Z = V_{ref}$



$$V_Z = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \bullet R1$$

FIGURE 2–TEST CIRCUIT FOR $V_Z > V_{ref}$

TYPICAL CHARACTERISTICS

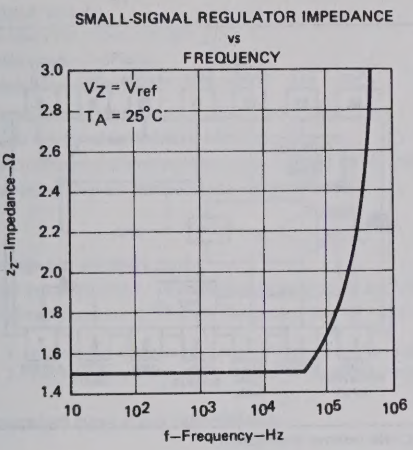


FIGURE 3

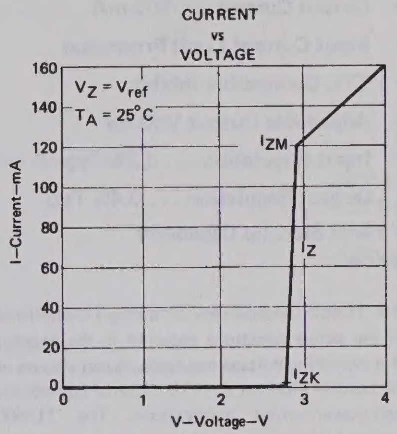
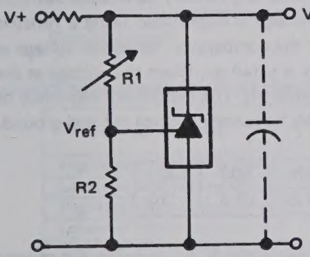


FIGURE 4

TYPICAL APPLICATION DATA


V+
Vout
R1
Vref
R2

$V_{out} \approx (1 + \frac{R1}{R2}) V_{ref}$

FIGURE 5—SHUNT REGULATOR

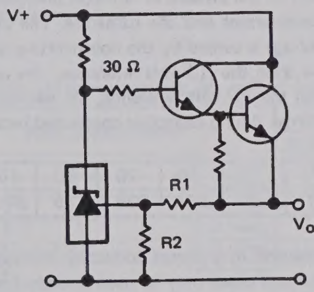
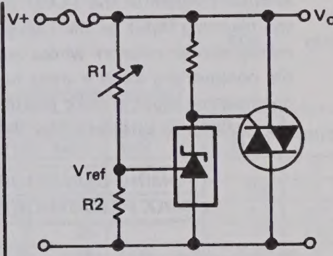

V+
30 Ω
R1
R2
Vout

FIGURE 6—SERIES REGULATOR


V+
Vout
R1
Vref
R2

$V_{out} \approx (1 + \frac{R1}{R2}) V_{ref}$

FIGURE 7—CROW BAR

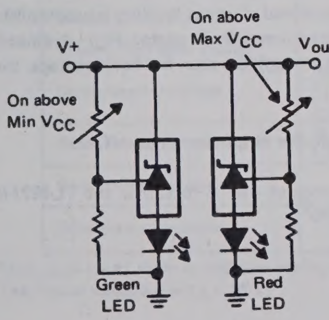
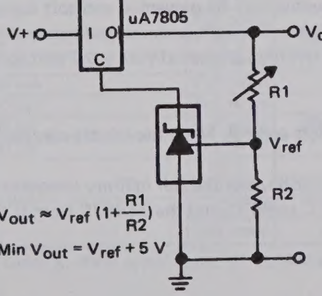

V+
On above Max V_{CC}
Vout
On above Min V_{CC}
Green LED
Red LED

FIGURE 8—SUPPLY MIN/MAX DETECTOR


uA7805
V+
I
O
C
Vout
R1
Vref
R2

$V_{out} \approx V_{ref} (1 + \frac{R1}{R2})$

Min $V_{out} = V_{ref} + 5$ V

FIGURE 9—CONTROLLING OUTPUT VOLTAGE OF FIXED-VOLTAGE REGULATOR

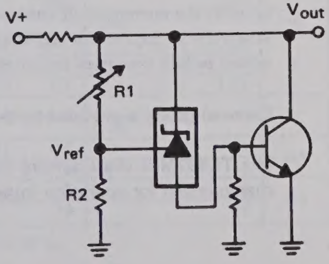

V+
Vout
R1
Vref
R2

FIGURE 10—HIGHER-CURRENT APPLICATIONS

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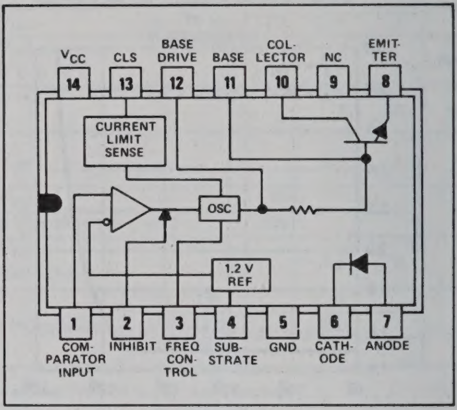
TYPES TL497M, TL497I, TL497C
SWITCHING VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612422, JUNE 1976

- All Monolithic
- High Efficiency . . . 60% or Greater
- Output Current . . . 500 mA
- Input Current Limit Protection
- TTL Compatible Inhibit
- Adjustable Output Voltage
- Input Regulation . . . 0.2% Typ
- Output Regulation . . . 0.4% Typ
- Soft Start-up Capability

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The TL497 incorporates on a single monolithic chip all the active functions required in the construction of a switching voltage regulator. It can also be used as the control element to drive external components for high-power-output applications. The TL497 was designed for ease of use in step-up, step-down, or voltage inversion applications requiring high efficiency.

A block diagram of the TL497 is shown in the pinout. A 1.2-volt precision reference is internally connected between the inverting input of the high-gain comparator and the substrate. The output voltage is established using a resistive voltage-divider network whose node voltage is sensed by the noninverting input of the comparator. When the voltage at the noninverting input is more negative than the 1.2 volt reference, the oscillator is gated on. When the voltage at the noninverting input is more positive than the 1.2-volt reference, the oscillator is gated off. The maximum frequency of the oscillator is established by the external timing capacitor connected between the frequency control pin and ground.

TIMING CAPACITOR (pF)	5	10	20	50	100	200	500	1000
MAX FREQUENCY (kHz)	385	313	238	135	80.6	47.6	19.6	10

The transistor switch is normally connected to external inductive components and a diode to generate the output voltage. The TL497 switching transistor and diode may be used directly for switching currents up to 500 milliamperes, or used to drive an external transistor and diode for higher output-power applications.

The TL497 also provides current limiting for protection of the switching transistor and the load. With proper current limiting, saturation of the power inductor may be prevented and soft start-up achieved. Current limiting is accomplished with the current-limit control provided. The voltage developed across the series current-limit resistor, R_{CL}, is sensed. When the voltage at the current-sense terminal is approximately 0.7 volt (one V_{BE} drop) less than the input voltage, the power switch transistor is turned off.

External gating is provided by the inhibit control. When the inhibit control is high, the output is turned off.

The TL497M is characterized for operation over the full military temperature range of –55°C to 125°C, the TL497I is characterized for operation from –25°C to 85°C, and the TL497C from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage (see Note 1)		15 V
Output voltage		35 V
Comparator input voltage		5 V
Inhibit input voltage		5 V
Diode reverse voltage		35 V
Power switch current		750 mA
Diode continuous forward current		750 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)		1000 mW
Operating free-air temperature range:	TL497M	–55°C to 125°C
	TL497I	–25°C to 85°C
	TL497C	0°C to 70°C
Storage temperature range		–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260°C

NOTES: 1. All voltage values except diode voltages are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I		4.5	12	V
Output voltage:	step-up configuration (see Figure 2)	$V_I + 2$	30	V
	step-down configuration (see Figure 3)	V_{ref}	$V_I - 1$	V
	negative regulator (see Figure 4)	$-V_{ref}$	–25	V
Output current			500	mA

electrical characteristics at specified free-air temperature, V_I = 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL497M, TL497I			TL497C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level inhibit input voltage			Full range	2			2			V
Low-level inhibit input voltage			Full range			0.6			0.8	V
High-level inhibit input current	$V_{I(I)}$ = 5 V		Full range		0.8	1.5		0.8	1.5	mA
Low-level inhibit input current	$V_{I(I)}$ = 0 V		Full range		5	20		5	10	μA
Comparator reference voltage	V_I = 4.5 V to 6 V		Full range	1.14	1.20	1.26	1.08	1.20	1.32	V
Comparator input bias current	V_I = 6 V		Full range		40	100		40	100	μA
Regulator output voltage	See Figure 1 R1 = 11.3 kΩ, R2 = 1 kΩ		25°C	14.25	15	15.75	13.5	15	16.5	V
Switch on-state voltage	V_I = 4.5 V	I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
		I_O = 500 mA	Full range			1			0.85	
Switch off-state current	V_I = 4.5 V		25°C		10	50		10	50	μA
			Full range			500			200	
Current-limit sense voltage	V_{CC} = 6 V		25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA		Full range		0.75	0.95		0.75	0.85	V
	I_O = 100 mA		Full range		0.9	1.1		0.9	1	
	I_O = 500 mA		Full range		1.33	1.7		1.33	1.55	
Diode reverse voltage	I_O = 500 μA		Full range	30						V
	I_O = 200 μA		Full range				30			
On-state supply current			25°C		11	14		11	14	mA
			Full range			16			15	
Off-state supply current			25°C		6	9		6	9	mA
			Full range			11			10	

†Full range for TL497M is –55°C to 125°C, for TL497I is –25°C to 85°C, and for TL497C is 0°C to 70°C.
‡All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

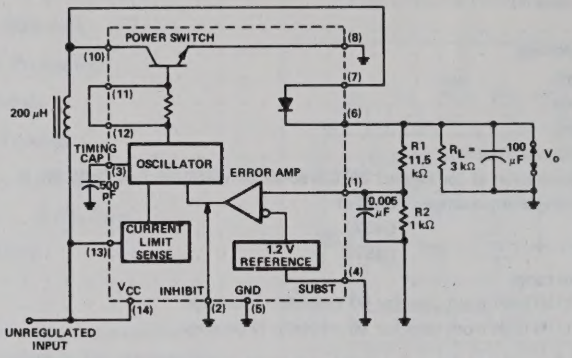

POWER SWITCH
(10)
(8)
(7)
(11)
200 µH
(6)
(12)
TIMING CAP
(3)
OSCILLATOR
ERROR AMP
500 pF
R1 11.5 kΩ
R$_L$ = 3 kΩ
100 µF
V$_o$
(1)
0.005 µF
R2 1 kΩ
CURRENT LIMIT SENSE
(13)
1.2 V REFERENCE
(4)
V$_{CC}$
INHIBIT
GND
SUBST
(14)
(2)
(5)
UNREGULATED INPUT

FIGURE 1—TEST CIRCUIT

TYPICAL APPLICATION DATA

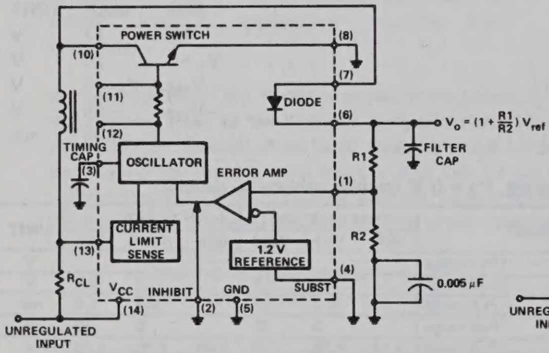

POWER SWITCH
(8)
(10)
(7)
(11)
DIODE
(6)
(12)
V$_o$ = (1 + $\frac{R1}{R2}$) V$_{ref}$
TIMING CAP
(3)
OSCILLATOR
R1
FILTER CAP
ERROR AMP
(1)
CURRENT LIMIT SENSE
R2
(13)
1.2 V REFERENCE
(4)
R$_{CL}$
V$_{CC}$
INHIBIT
GND
SUBST
0.005 µF
(14)
(2)
(5)
UNREGULATED INPUT

FIGURE 2—POSITIVE REGULATOR, STEP-UP CONFIGURATION

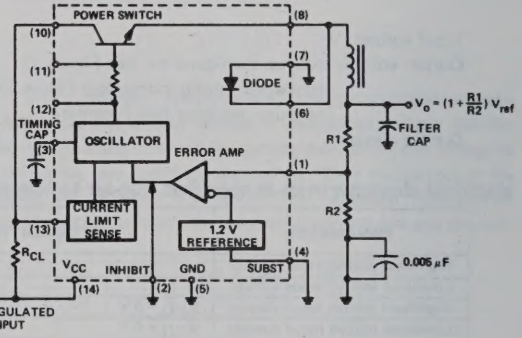
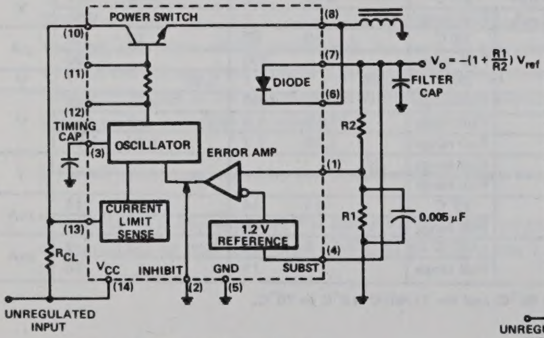

POWER SWITCH
(8)
(10)
(7)
(11)
DIODE
V$_o$ = (1 + $\frac{R1}{R2}$) V$_{ref}$
(6)
(12)
TIMING CAP
R1
FILTER CAP
(3)
OSCILLATOR
ERROR AMP
(1)
R2
CURRENT LIMIT SENSE
(13)
1.2 V REFERENCE
(4)
0.005 µF
R$_{CL}$
V$_{CC}$
INHIBIT
GND
SUBST
(14)
(2)
(5)
UNREGULATED INPUT

FIGURE 3—POSITIVE REGULATOR, STEP-DOWN CONFIGURATION


POWER SWITCH
(8)
(10)
(7)
V$_o$ = −(1 + $\frac{R1}{R2}$) V$_{ref}$
(11)
DIODE
FILTER CAP
(6)
(12)
TIMING CAP
R2
(3)
OSCILLATOR
ERROR AMP
(1)
R1
0.005 µF
CURRENT LIMIT SENSE
(13)
1.2 V REFERENCE
(4)
R$_{CL}$
V$_{CC}$
INHIBIT
GND
SUBST
(14)
(2)
(5)
UNREGULATED INPUT

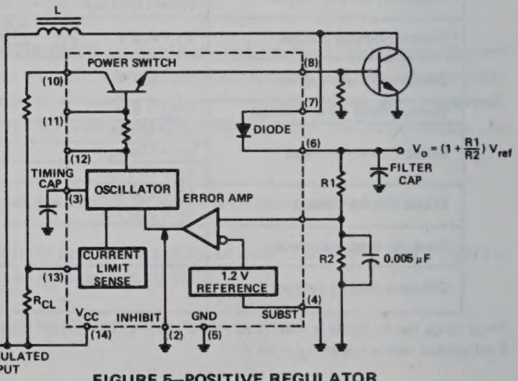

L
POWER SWITCH
(8)
(10)
(7)
(11)
DIODE
(6)
V$_o$ = (1 + $\frac{R1}{R2}$) V$_{ref}$
(12)
FILTER CAP
TIMING CAP
R1
(3)
OSCILLATOR
ERROR AMP
R2
0.005 µF
CURRENT LIMIT SENSE
(13)
1.2 V REFERENCE
(4)
R$_{CL}$
V$_{CC}$
INHIBIT
GND
SUBST
(14)
(2)
(5)
UNREGULATED INPUT

FIGURE 4—NEGATIVE REGULATOR
(e.g., +5 VOLTS INPUT TO −5 VOLTS OUTPUT)
OR
(i.e., POSITIVE INPUT, NEGATIVE OUTPUT)

FIGURE 5—POSITIVE REGULATOR WITH BUFFERED OUTPUT

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LINEAR
INTEGRATED CIRCUITS

TYPES uA723M, uA723C
PRECISION VOLTAGE REGULATORS

BULLETIN NO. DL-S 7611533, AUGUST 1972—REVISED JUNE 1976

FORMERLY SN52723, SN72723

- 150-mA Load Current without External Power Transistor
- Typically 0.02% Input Regulation and 0.03% Load Regulation (uA723M)
- Adjustable Current Limiting Capability
- Input Voltages to 40 Volts
- Output Adjustable from 2 to 37 Volts
- Designed to be Interchangeable with Fairchild μA723 and μA723C Respectively

description

The uA723M and uA723C are monolithic integrated circuit voltage regulators featuring high ripple rejection, excellent input and load regulation, excellent temperature stability, and low standby current. The circuit consists of a temperature-compensated reference voltage amplifier, an error amplifier, a 150-milliampere output transistor, and an adjustable output current limiter.

The uA723M and uA723C are designed for use in positive or negative power supplies as a series, shunt, switching, or floating regulator. For output currents exceeding 150 mA, additional pass elements may be connected as shown in Figures 4 and 5.

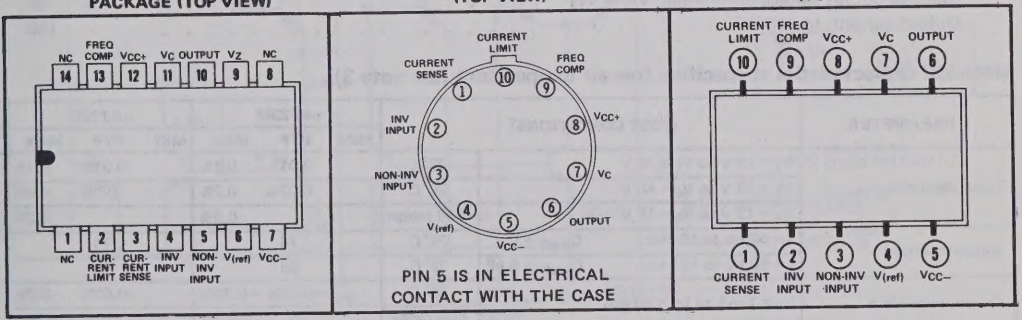
The uA723M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA723C is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

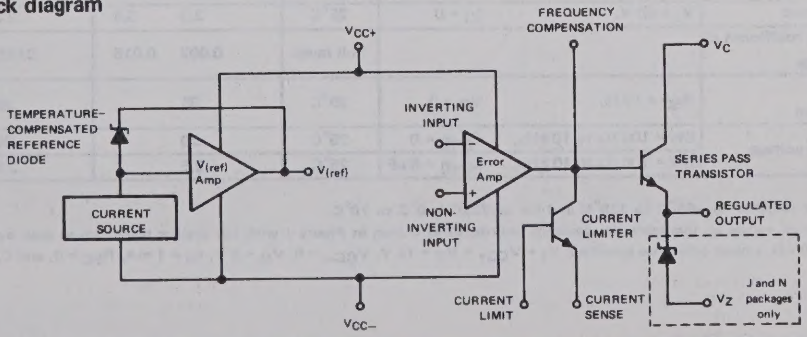
L PLUG-IN PACKAGE (TOP VIEW)

U FLAT PACKAGE (TOP VIEW)


NC
FREQ COMP
VCC+
VC
OUTPUT
VZ
NC
14
13
12
11
10
9
8
1
2
3
4
5
6
7
NC
CURRENT LIMIT
CURRENT SENSE
INV INPUT
NON-INV INPUT
V(ref)
VCC−
CURRENT LIMIT
CURRENT SENSE
FREQ COMP
INV INPUT
VCC+
NON-INV INPUT
VC
V(ref)
OUTPUT
VCC−
PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE
CURRENT LIMIT
FREQ COMP
VCC+
VC
OUTPUT
CURRENT SENSE
INV INPUT
NON-INV INPUT
V(ref)
VCC−

NC—No internal connection

functional block diagram


VCC+
TEMPERATURE-COMPENSATED REFERENCE DIODE
CURRENT SOURCE
V(ref) Amp
V(ref)
INVERTING INPUT
NON-INVERTING INPUT
Error Amp
FREQUENCY COMPENSATION
VC
SERIES PASS TRANSISTOR
REGULATED OUTPUT
CURRENT LIMITER
CURRENT LIMIT
CURRENT SENSE
VZ
J and N packages only
VCC−

TYPES uA723M, uA723C
PRECISION VOLTAGE REGULATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Peak voltage from V_{CC+} to V_{CC-} ($t_w \leqslant 50$ ms)	50 V
Continuous voltage from V_{CC+} to V_{CC-}	40 V
Input-to-output voltage differential	40 V
Differential input voltage to error amplifier	±5 V
Voltage between noninverting input and V_{CC-}	8 V
Current from V_Z	25 mA
Current from $V_{(ref)}$	15 mA
Continuous total dissipation at (or below 25°C free-air temperature (see Note 1):	
J or N package	1000 mW
L package (see Note 2)	800 mW
U package	675 mW
Operating free-air temperature range: uA723M Circuits	−55°C to 125°C
uA723C Circuits	0°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds, J, L, or U package	300°C
Lead temperature 1/16 inch from case for 10 seconds, N package	260°C

NOTES: 1. Power dissipation = $[I_{(standby)} + I_{(ref)}]\ V_{CC} + [V_C - V_O]\ I_O$. For operation at elevated temperature, refer to Dissipation Derating Curves, Section 2.

2. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	9.5	40	V
Output voltage, V_O	2	37	V
Input-to-output voltage differential, $V_C - V_O$	3	38	V
Output current, I_O		150	mA

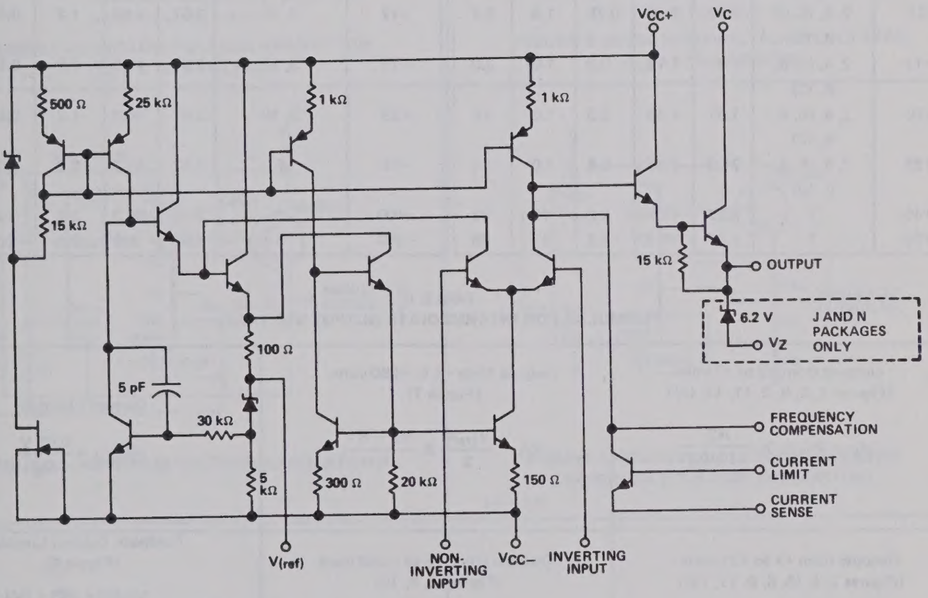
electrical characteristics at specified free-air temperature (see note 3)

PARAMETER	TEST CONDITIONS†		uA723M			uA723C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input regulation	V_I = 12 V to V_I = 15 V	25°C		0.01%	0.1%		0.01%	0.1%	
	V_I = 12 V to V_I = 40 V	25°C		0.02%	0.2%		0.1%	0.5%	
	V_I = 12 V to V_I = 15 V	Full range			0.3%			0.3%	
Ripple rejection	f = 50 Hz to 10 kHz, $C_{(ref)} = 0$	25°C		74			74		dB
	f = 50 Hz to 10 kHz, $C_{(ref)} = 5\ \mu F$	25°C		86			86		
Output regulation	I_O = 1 mA to I_O = 50 mA	25°C		−0.03%	−0.15%		−0.03%	−0.2%	
		Full range			−0.6%			−0.6%	
Reference voltage, $V_{(ref)}$		25°C	6.95	7.15	7.35	6.8	7.15	7.5	V
Standby current	V_I = 30 V, $I_O = 0$	25°C		2.3	3.5		2.3	4	mA
Temperature coefficient of output voltage		Full range		0.002	0.015		0.003	0.015	%/°C
Short-circuit output current	$R_{SC} = 10\ \Omega$, $V_O = 0$	25°C		65			65		mA
Output noise voltage	BW = 100 Hz to 10 kHz, $C_{(ref)} = 0$	25°C		20			20		µV
	BW = 100 Hz to 10 kHz, $C_{(ref)} = 5\ \mu F$	25°C		2.5			2.5		

†Full range for uA723M is −55°C to 125°C and for uA723C is 0°C to 70°C.

NOTE 3: For all values in this table the device is connected as shown in Figure 1 with the divider resistance as seen by the error amplifier $\leqslant 10\ k\Omega$. Unless otherwise specified, $V_I = V_{CC+} = V_C = 12$ V, $V_{CC-} = 0$, $V_O = 5$ V, $I_O = 1$ mA, $R_{SC} = 0$, and $C_{(ref)} = 0$.

schematic


VCC+
VC
500 Ω
25 kΩ
1 kΩ
1 kΩ
15 kΩ
15 kΩ
OUTPUT
6.2 V
VZ
J AND N
PACKAGES
ONLY
100 Ω
5 pF
30 kΩ
5 kΩ
300 Ω
20 kΩ
150 Ω
FREQUENCY
COMPENSATION
CURRENT
LIMIT
CURRENT
SENSE
V(ref)
NON-INVERTING INPUT
VCC−
INVERTING INPUT

TYPES uA723M, uA723C
PRECISION VOLTAGE REGULATORS

TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

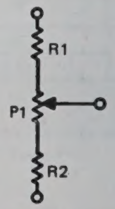
OUTPUT VOLTAGE (V)	APPLICABLE FIGURES (SEE NOTE 4)	FIXED OUTPUT ± 5%		OUTPUT ADJUSTABLE ± 10% (SEE NOTE 5)		
		R1 (kΩ)	R2 (kΩ)	R1 (kΩ)	P1 (kΩ)	R2 (kΩ)
+3.0	1, 5, 6, 9, 11, 12 (4)	4.12	3.01	1.8	0.5	1.2
+3.6	1, 5, 6, 9, 11, 12 (4)	3.57	3.65	1.5	0.5	1.5
+5.0	1, 5, 6, 9, 11, 12 (4)	2.15	4.99	0.75	0.5	2.2
+6.0	1, 5, 6, 9, 11, 12 (4)	1.15	6.04	0.5	0.5	2.7
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0
+45	7	3.57	48.7	2.2	10	39
+75	7	3.57	78.7	2.2	10	68
+100	7	3.57	105	2.2	10	91
+250	7	3.57	255	2.2	10	240
−6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
−9	3, 10	3.48	5.36	1.2	0.5	2.0
−12	3, 10	3.57	8.45	1.2	0.5	3.3
−15	3, 10	3.57	11.5	1.2	0.5	4.3
−28	3, 10	3.57	24.3	1.2	0.5	10
−45	8	3.57	41.2	2.2	10	33
−100	8	3.57	95.3	2.2	10	91
−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAS FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 11, 12, (4)] $V_O = V_{(ref)} \times \frac{R2}{R1 + R2}$	Outputs from +4 to +250 volts [Figure 7] $V_O = \frac{V_{(ref)}}{2} \times \frac{R2 - R1}{R1};$ R3 = R4	Current Limiting $I_{(limit)} \approx \frac{0.65\ V}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 11, 12)] $V_O = V_{(ref)} \times \frac{R1 + R2}{R2}$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_O = -\frac{V_{(ref)}}{2} \times \frac{R1 + R2}{R1};$ R3 = R4	Foldback Current Limiting [Figure 6] $I_{(knee)} \approx \frac{V_O R3 + (R3 + R4)\ 0.65\ V}{R_{sc} R4};$ $I_{OS} \approx \frac{0.65\ V}{R_{sc}} \times \frac{R3 + R4}{R4}$

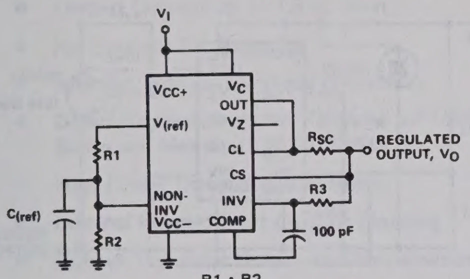
NOTES:

4. Figures 1 through 12 show the R1/R2 divider across either V_O or $V_{(ref)}$. Figure numbers in parentheses may be used if the R1/R2 divider is placed across the other voltage ($V_{(ref)}$ or V_O) that it was not placed across in the figures without parentheses.
5. To make the voltage adjustable, the R1/R2 divider shown in the figures must be replaced by the divider shown at the right.
6. For negative output voltages less than 9 V, V_{CC+} and V_C must be connected to a positive supply such that the voltage between V_{CC+} and V_{CC-} is greater than 9 V.
7. When 10-lead uA723 devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the V_O terminal.



ADJUSTABLE OUTPUT CIRCUITS

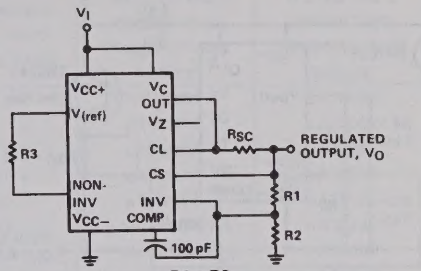
TYPICAL APPLICATION DATA


VI
VCC+
VC
OUT
V(ref)
VZ
CL
CS
NON-INV
INV
VCC–
COMP
R1
R2
C(ref)
RSC
R3
100 pF
REGULATED OUTPUT, VO

NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum α_{V_O}.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

FIGURE 1—BASIC LOW-VOLTAGE REGULATOR (V_O = 2 TO 7 VOLTS)


VI
VCC+
VC
OUT
V(ref)
VZ
CL
CS
NON-INV
INV
VCC–
COMP
R3
RSC
REGULATED OUTPUT, VO
R1
R2
100 pF

NOTES: A. $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum α_{V_O}.

B. R3 may be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

FIGURE 2—BASIC HIGH-VOLTAGE REGULATOR (V_O = 7 TO 37 VOLTS)

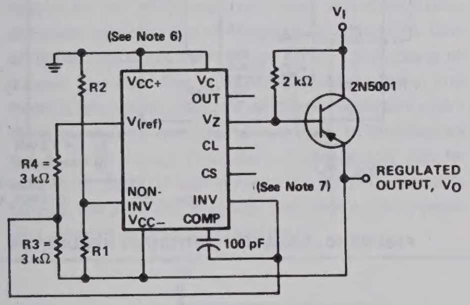

(See Note 6)
VI
R2
VCC+
VC
OUT
V(ref)
VZ
CL
CS
NON-INV
INV
VCC–
COMP
2 kΩ
2N5001
R4 = 3 kΩ
R3 = 3 kΩ
R1
100 pF
(See Note 7)
REGULATED OUTPUT, VO

FIGURE 3—NEGATIVE VOLTAGE REGULATOR

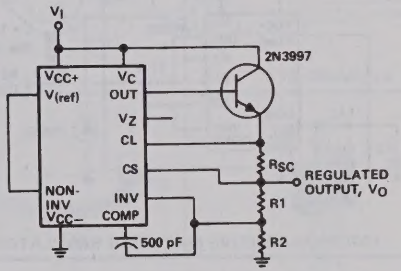

VI
2N3997
VCC+
VC
V(ref)
OUT
VZ
CL
CS
NON-INV
INV
VCC–
COMP
RSC
REGULATED OUTPUT, VO
R1
R2
500 pF

FIGURE 4—POSITIVE VOLTAGE REGULATOR (EXTERNAL N-P-N PASS TRANSISTOR)

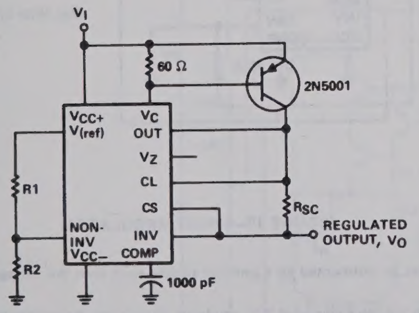

VI
60 Ω
2N5001
VCC+
V(ref)
VC
OUT
VZ
CL
CS
NON-INV
INV
VCC–
COMP
R1
R2
RSC
REGULATED OUTPUT, VO
1000 pF

FIGURE 5—POSITIVE VOLTAGE REGULATOR (EXTERNAL P-N-P PASS TRANSISTOR)

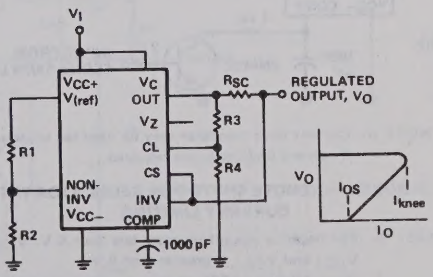

VI
VCC+
V(ref)
VC
OUT
VZ
CL
CS
NON-INV
INV
VCC–
COMP
RSC
REGULATED OUTPUT, VO
R3
R4
R1
R2
1000 pF
VO
IOS
Iknee
IO

FIGURE 6—FOLDBACK CURRENT LIMITING

TYPICAL APPLICATION DATA

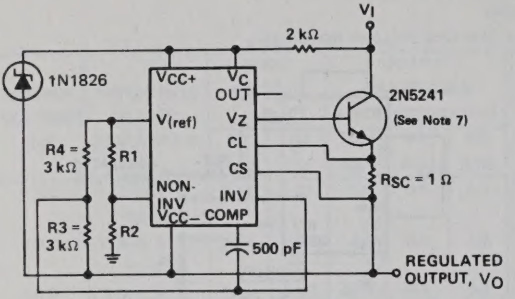

VI
2 kΩ
1N1826
VCC+
VC
OUT
V(ref)
VZ
CL
CS
NON-INV
INV
VCC−
COMP
2N5241
(See Note 7)
R4 = 3 kΩ
R1
RSC = 1 Ω
R3 = 3 kΩ
R2
500 pF
REGULATED OUTPUT, VO

FIGURE 7–POSITIVE FLOATING REGULATOR

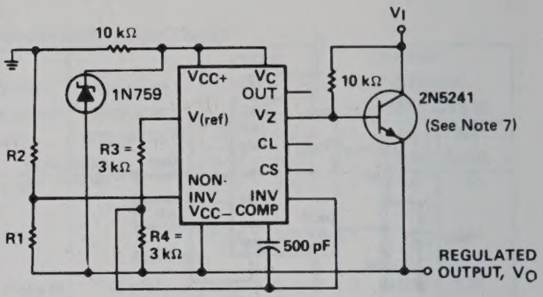

VI
10 kΩ
1N759
VCC+
VC
OUT
V(ref)
VZ
CL
CS
NON-INV
INV
VCC−
COMP
10 kΩ
2N5241
(See Note 7)
R2
R3 = 3 kΩ
R1
R4 = 3 kΩ
500 pF
REGULATED OUTPUT, VO

FIGURE 8–NEGATIVE FLOATING REGULATOR

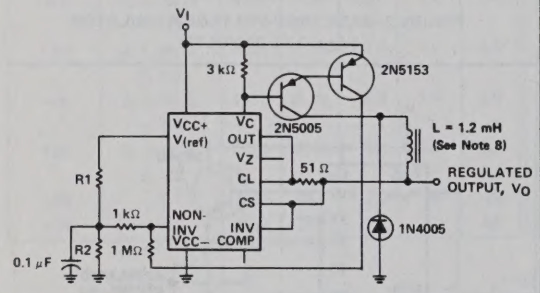

VI
3 kΩ
2N5153
2N5005
VCC+
VC
V(ref)
OUT
VZ
CL
CS
NON-INV
INV
VCC−
COMP
L = 1.2 mH
(See Note 8)
51 Ω
REGULATED OUTPUT, VO
R1
1 kΩ
R2
1 MΩ
0.1 µF
1N4005

FIGURE 9–POSITIVE SWITCHING REGULATOR

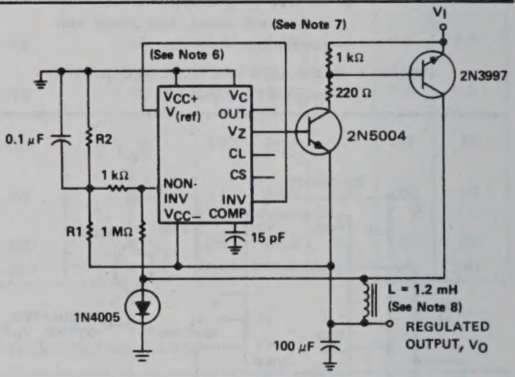
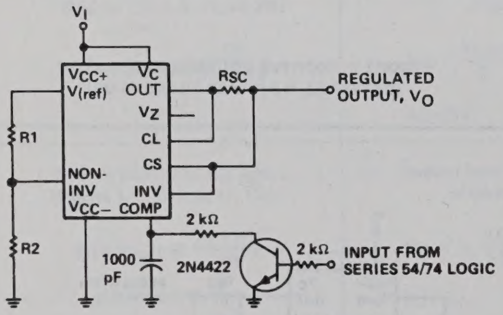

VI
(See Note 7)
(See Note 6)
1 kΩ
2N3997
220 Ω
VCC+
VC
V(ref)
OUT
VZ
CL
CS
NON-INV
INV
VCC−
COMP
2N5004
0.1 µF
R2
1 kΩ
R1
1 MΩ
15 pF
L = 1.2 mH
(See Note 8)
1N4005
REGULATED OUTPUT, VO
100 µF

FIGURE 10–NEGATIVE SWITCHING REGULATOR

6


VI
VCC+
VC
V(ref)
OUT
VZ
CL
CS
NON-INV
INV
VCC−
COMP
RSC
REGULATED OUTPUT, VO
R1
R2
2 kΩ
1000 pF
2N4422
2 kΩ
INPUT FROM SERIES 54/74 LOGIC

NOTE A: Current limit transistor may be used for shutdown if current limiting is not required.

FIGURE 11–REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

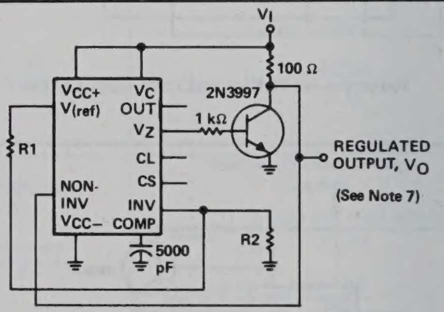

VI
100 Ω
VCC+
VC
V(ref)
OUT
VZ
CL
CS
NON-INV
INV
VCC−
COMP
2N3997
1 kΩ
R1
REGULATED OUTPUT, VO
(See Note 7)
R2
5000 pF

FIGURE 12–SHUNT REGULATOR

NOTES: 6. For negative output voltages less than 9 V, V_{CC+} and V_C must be connected to a positive supply such that the voltage between V_{CC+} and V_{CC-} is greater than 9 V.

7. When 10-lead uA723 devices are used in applications requiring V_Z, an external 6.2-V regulator diode must be connected in series with the V_O terminal.

8. L is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 potted core, or equivalent, with 0.009-inch air gap.

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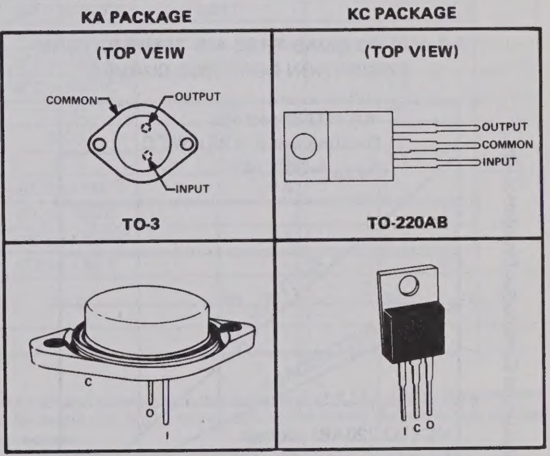
SERIES uA7800
POSITIVE-VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612386, MAY 1976

- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- Direct Replacements for Fairchild µA7800 Series and National LM340 Series
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

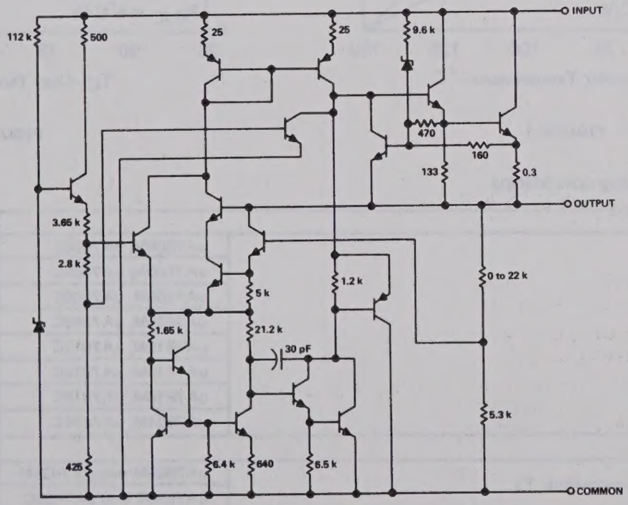
NOMINAL OUTPUT VOLTAGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
5 V	uA7805M	uA7805C
6 V	uA7806M	uA7806C
8 V	uA7808M	uA7808C
8.5 V	uA7885M	uA7885C
12 V	uA7812M	uA7812C
15 V	uA7815M	uA7815C
18 V	uA7818M	uA7818C
24 V	uA7824M	uA7824C
packages	KA	KA and KC


KA PACKAGE
(TOP VEIW)
COMMON
OUTPUT
INPUT
TO-3
KC PACKAGE
(TOP VIEW)
OUTPUT
COMMON
INPUT
TO-220AB
C
O
I
I C O

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. One of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

schematic


INPUT
112 k
500
25
25
9.6 k
470
160
133
0.3
OUTPUT
3.65 k
2.8 k
1.2 k
0 to 22 k
5 k
1.65 k
21.2 k
30 pF
5.3 k
425
6.4 k
640
6.5 k
COMMON

Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78__M	uA78__C	UNIT
Input voltage	uA7824M, uA7824C	40	40	V
	All others	35	35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)	KA (TO-3) package	3.5	3.5	W
	KC (TO-220AB) package		2	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15	15	W
Operating free-air, case, or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	KA (TO-3) package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	KC (TO-220AB) package		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Curves, Figure 1 and Figure 2.

TO-3 AND TO-220AB FREE-AIR TEMPERATURE DISSIPATION DERATING CURVES

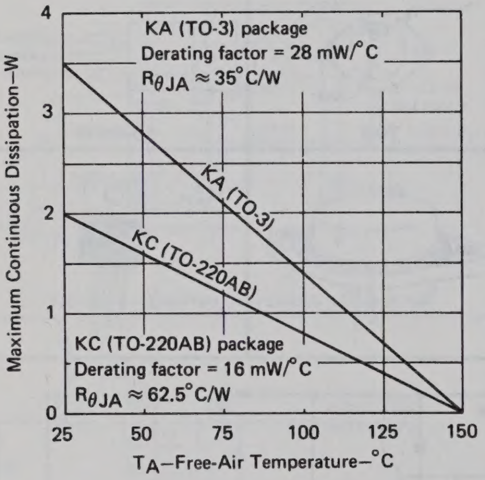


FIGURE 1

TO-3 AND TO-220AB CASE TEMPERATURE DISSIPATION DERATING CURVE

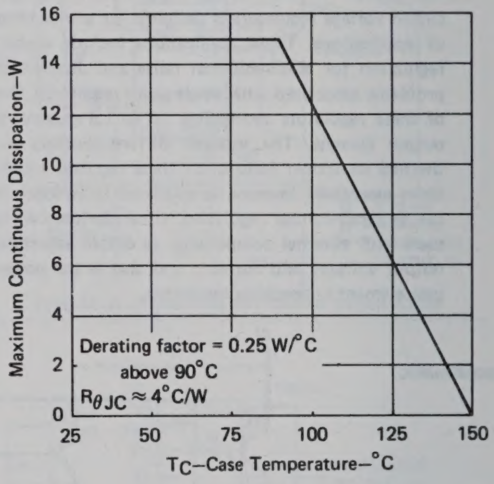


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7805M, uA7805C	7	25	V
	uA7806M, uA7806C	8	25	
	uA7808M, uA7808C	10.5	25	
	uA7885M, uA7885C	10.5	25	
	uA7812M, uA7812C	14.5	30	
	uA7815M, uA7815C	17.5	30	
	uA7818M, uA7818C	21	33	
	uA7824M, uA7824C	27	38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J	uA7805M thru uA7824M	−55	150	°C
	uA7805C thru uA7824C	0	125	

uA7805M, uA7805C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7805M			uA7805C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	4.8	5	5.2	4.8	5	5.2	V
	I_O = 5 mA to 1 A, P ≤ 15 W	V_I = 8 V to 20 V	−55°C to 150°C	4.65		5.35				
		V_I = 7 V to 20 V	0°C to 125°C				4.75		5.25	
Input regulation	V_I = 7 V to 25 V		25°C		3	50		3	100	mV
	V_I = 8 V to 12 V				1	25		1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		−55°C to 150°C	68	78					dB
			0°C to 125°C				62	78		
Output regulation	I_O = 5 mA to 1.5 A		25°C		15	50		15	100	mV
	I_O = 250 mA to 750 mA				5	25		5	50	
Output resistance	f = 1 kHz		−55°C to 150°C		0.017					Ω
			0°C to 125°C					0.017		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−1.1					mV/°C
			0°C to 125°C					−1.1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		40			40		μV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.2	6		4.2	8	mA
Bias current change	V_I = 8 V to 25 V		−55°C to 150°C			0.8				mA
	V_I = 7 V to 25 V		0°C to 125°C						1.3	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		750			750		mA
Peak output current			25°C		2.2			2.2		A

---

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7806M, uA7806C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7806M			uA7806C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	5.75	6	6.25	5.75	6	6.25	V
	I_O = 5 mA to 1 A, P ≤ 15 W	V_I = 9 V to 21 V	−55°C to 150°C	5.65		6.35				
		V_I = 8 V to 21 V	0°C to 125°C				5.7		6.3	
Input regulation	V_I = 8 V to 25 V		25°C		5	60		5	120	mV
	V_I = 9 V to 13 V				1.5	30		1.5	60	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz		−55°C to 150°C	65	75					dB
			0°C to 125°C				59	75		
Output regulation	I_O = 5 mA to 1.5 A		25°C		14	60		14	120	mV
	I_O = 250 mA to 750 mA				4	30		4	60	
Output resistance	f = 1 kHz		−55°C to 150°C		0.019					Ω
			0°C to 125°C					0.019		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−0.8					mV/°C
			0°C to 125°C					−0.8		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		45			45		µV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.3	6		4.3	8	mA
Bias current change	V_I = 9 V to 25 V		−55°C to 150°C			0.8				mA
	V_I = 8 V to 25 V		0°C to 125°C						1.3	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		550			550		mA
Peak output current			25°C		2.2			2.2		A

---

†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7808M, uA7808C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7808M			uA7808C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	7.7	8	8.3	7.7	8	8.3	V
	I_O = 5 mA to 1 A, P ≤ 15 W	V_I = 11.5 V to 23 V	−55°C to 150°C	7.6		8.4				
		V_I = 10.5 V to 23 V	0°C to 125°C				7.6		8.4	
Input regulation	V_I = 10.5 V to 25 V		25°C		6	80		6	160	mV
	V_I = 11 V to 17 V				2	40		2	80	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz		−55°C to 150°C	62	72					dB
			0°C to 125°C				56	72		
Output regulation	I_O = 5 mA to 1.5 A		25°C		12	80		12	160	mV
	I_O = 250 mA to 750 mA				4	40		4	80	
Output resistance	f = 1 kHz		−55°C to 150°C		0.016					Ω
			0°C to 125°C					0.016		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−0.8					mV/°C
			0°C to 125°C					−0.8		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		52			52		µV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.3	6		4.3	8	mA
Bias current change	V_I = 11.5 V to 25 V		−55°C to 150°C			0.8				mA
	V_I = 10.5 to 25 V		0°C to 125°C						1	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		450			450		mA
Peak output current			25°C		2.2			2.2		A

---

†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TYPES uA7885M, uA7885C
POSITIVE-VOLTAGE REGULATORS

uA7885M, uA7885C electrical characteristics at specified virtual junction temperature, V_I = 15 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7885M			uA7885C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	8.15	8.5	8.85	8.15	8.5	8.85	V
	I_O = 5 mA to 1 A, $P \leq 15$ W	V_I = 12 V to 23.5 V	−55°C to 150°C	8.1		8.9				
		V_I = 11 V to 23.5 V	0°C to 125°C				8.1		8.9	
Input regulation	V_I = 10.5 V to 25 V		25°C		6	85		6	170	mV
	V_I = 11 V to 17 V				2	40		2	85	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz		−55°C to 150°C	60	70					dB
			0°C to 125°C				54	70		
Output regulation	I_O = 5 mA to 1.5 A		25°C		12	85		12	170	mV
	I_O = 250 mA to 750 mA				4	40		4	85	
Output resistance	f = 1 kHz		−55°C to 150°C		0.016					Ω
			0°C to 125°C					0.016		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−0.8					mV/°C
			0°C to 125°C					−0.8		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		55			55		μV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.3	6		4.3	8	mA
Bias current change	V_I = 11.5 V to 25 V		−55°C to 150°C			0.8				mA
	V_I = 10.5 to 25 V		0°C to 125°C						1	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		450			450		mA
Peak output current			25°C		2.2			2.2		A

---

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7812M, uA7812C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7812M			uA7812C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	11.5	12	12.5	11.5	12	12.5	V
	I_O = 5 mA to 1 A, P ⩽ 15 W	V_I = 15.5 V to 27 V	−55°C to 150°C	11.4		12.6				
		V_I = 14.5 V to 27 V	0°C to 125°C				11.4		12.6	
Input regulation	V_I = 14.5 V to 30 V		25°C		10	120		10	240	mV
	V_I = 16 V to 22 V				3	60		3	120	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz		−55°C to 150°C	61	71					dB
			0°C to 125°C				55	71		
Output regulation	I_O = 5 mA to 1.5 A		25°C		12	120		12	240	mV
	I_O = 250 mA to 750 mA				4	60		4	120	
Output resistance	f = 1 kHz		−55°C to 150°C		0.018					Ω
			0°C to 125°C					0.018		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−1.0					mV/°C
			0°C to 125°C					−1.0		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		75			75		µV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.3	6		4.3	8	mA
Bias current change	V_I = 15 V to 30 V		−55°C to 150°C			0.8				mA
	V_I = 14.5 V to 30 V		0°C to 125°C						1	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		350			350		mA
Peak output current			25°C		2.2			2.2		A

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†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ⩽ 10 ms, duty cycles ⩽ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7815M, uA7815C electrical characteristics at specified virtual junction temperature, $V_I = 23$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7815M			uA7815C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	14.4	15	15.6	14.4	15	15.6	V
	$I_O = 5$ mA to 1 A, $P \leq 15$ W	$V_I = 18.5$ V to 30 V	−55°C to 150°C	14.25		15.75				
		$V_I = 17.5$ V to 30 V	0°C to 125°C				14.25		15.75	
Input regulation	$V_I = 17.5$ V to 30 V		25°C		11	150		11	300	mV
	$V_I = 20$ V to 26 V				3	75		3	150	
Ripple rejection	$V_I = 18.5$ V to 28.5 V, $f = 120$ Hz		−55°C to 150°C	60	70					dB
			0°C to 125°C				54	70		
Output regulation	$I_O = 5$ mA to 1.5 A		25°C		12	150		12	300	mV
	$I_O = 250$ mA to 750 mA				4	75		4	150	
Output resistance	$f = 1$ kHz		−55°C to 150°C		0.019					Ω
			0°C to 125°C					0.019		
Temperature coefficient of output voltage	$I_O = 5$ mA		0°C to 150°C		−1.0					mV/°C
			0°C to 125°C					−1.0		
Output noise voltage	$f = 10$ Hz to 100 kHz		25°C		90			90		μV
Dropout voltage	$I_O = 1$ A		25°C		2.0			2.0		V
Bias current			25°C		4.4	6		4.4	8	mA
Bias current change	$V_I = 18.5$ V to 30 V		−55°C to 150°C			0.8				mA
	$V_I = 17.5$ V to 30 V		0°C to 125°C						1	
	$I_O = 5$ mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		230			230		mA
Peak output current			25°C		2.1			2.1		A

---

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w < 10$ ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7818M, uA7818C electrical characteristics at specified virtual junction temperature, V_I = 27 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7818M			uA7818C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	17.3	18	18.7	17.3	18	18.7	V
	I_O = 5 mA to 1 A, P ≤ 15 W	V_I = 22 V to 33 V	−55°C to 150°C	17.1		18.9				
		V_I = 21 V to 33 V	0°C to 125°C				17.1		18.9	
Input regulation	V_I = 21 V to 33 V		25°C		15	180		15	360	mV
	V_I = 24 V to 30 V				5	90		5	180	
Ripple rejection	V_I = 22 V to 32 V, f = 120 Hz		−55°C to 150°C	59	69					dB
			0°C to 125°C				53	69		
Output regulation	I_O = 5 mA to 1.5 A		25°C		12	180		12	360	mV
	I_O = 250 mA to 750 mA				4	90		4	180	
Output resistance	f = 1 kHz		−55°C to 150°C		0.022					Ω
			0°C to 125°C					0.022		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−1.0					mV/°C
			0°C to 125°C					−1.0		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		110			110		μV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.5	6		4.5	8	mA
Bias current change	V_I = 22 V to 33 V		−55°C to 150°C			0.8				mA
	V_I = 21 V to 33 V		0°C to 125°C						1	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		200			200		mA
Peak output current			25°C		2.1			2.1		A

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† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7824M, uA7824C electrical characteristics at specified virtual junction temperature, $V_I = 33$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7824M			uA7824C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	23	24	25	23	24	25	V
	I_O = 5 mA to 1 A, P ⩽ 15 W	V_I = 28 V to 38 V	−55°C to 150°C	22.8		25.2				
		V_I = 27 V to 38 V	0°C to 125°C				22.8		25.2	
Input regulation	V_I = 27 V to 38 V		25°C		18	240		18	480	mV
	V_I = 30 V to 36 V				6	120		6	240	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz		−55°C to 150°C	56	66					dB
			0°C to 125°C				50	66		
Output regulation	I_O = 5 mA to 1.5 A		25°C		12	240		12	480	mV
	I_O = 250 mA to 750 mA				4	120		4	240	
Output resistance	f = 1 kHz		−55°C to 150°C		0.028					Ω
			0°C to 125°C					0.028		
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−1.5					mV/°C
			0°C to 125°C					−1.5		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		170			170		μV
Dropout voltage	I_O = 1 A		25°C		2.0			2.0		V
Bias current			25°C		4.6	6		4.6	8	mA
Bias current change	V_I = 28 V to 38 V		−55°C to 150°C			0.8				mA
	V_I = 27 V to 38 V		0°C to 125°C						1	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current			25°C		150			150		mA
Peak output current			25°C		2.1			2.1		A

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†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF and all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ⩽ 10 ms, duty cycles ⩽ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

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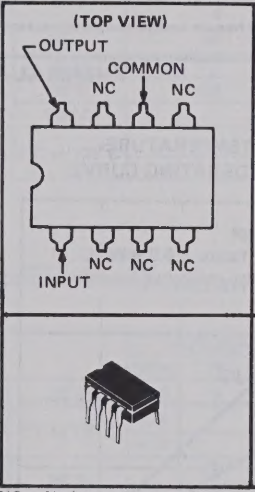
SERIES uA78L00
POSITIVE-VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612353, JANUARY 1976 – REVISED MAY 1976

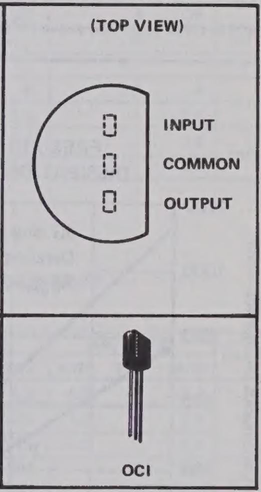
- 3-Terminal Regulators
- Output Current up to 100 mA
- No External Components
- Internal Thermal Overload Protection
- Unusually High Power Dissipation Capability
- Direct Replacement for Fairchild μA78L00 Series
- Internal Short-Circuit Current Limiting

NOMINAL OUTPUT VOLTAGE	5% OUTPUT VOLTAGE TOLERANCE	10% OUTPUT VOLTAGE TOLERANCE
2.6 V	uA78L02AC	uA78L02C
5 V	uA78L05AC	uA78L05C
6.2 V	uA78L06AC	uA78L06C
8 V	uA78L08AC	uA78L08C
12 V	uA78L12AC	uA78L12C
15 V	uA78L15AC	uA78L15C

JG
DUAL-IN-LINE PACKAGE



LP
SILECT† PACKAGE

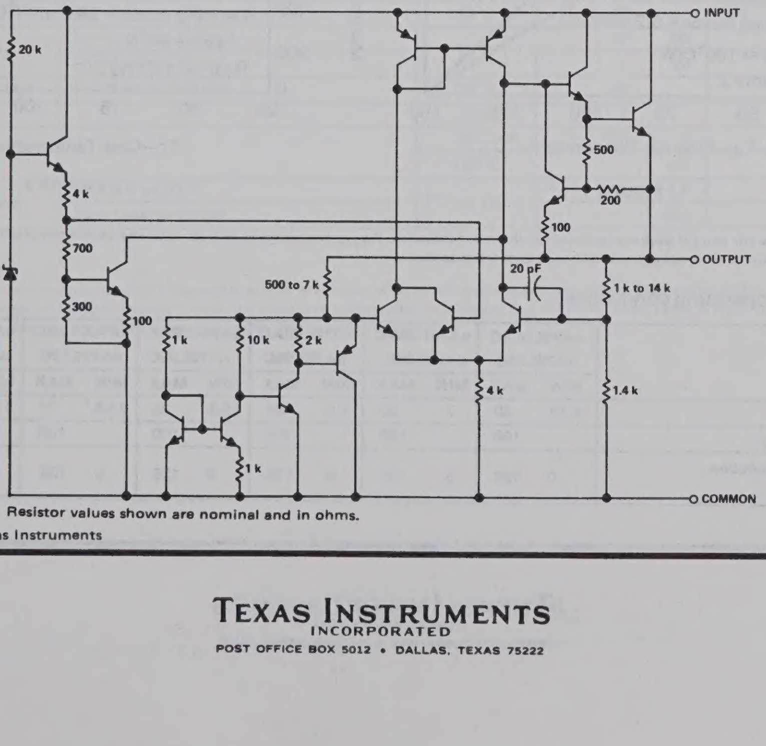


NC – No internal connection

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a Zener-diode–resistor combination, an effective improvement in output impedance of typically two orders of magnitude can be obtained together with lower bias current.

schematic



Resistor values shown are nominal and in ohms.

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†Trademark of Texas Instruments

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78L02AC, uA78L02C uA78L05AC, uA78L05C uA78L06AC, uA78L06C uA78L08AC, uA78L08C	uA78L12AC, uA78L12C uA78L15AC, uA78L15C	UNIT
Input voltage		30	35	V
Continuous total dissipation at 25°C free-air temperature (see Note 1)	JG package	1125	1125	mW
	LP package	775	775	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		1600	1600	mW
Operating free-air, case, or virtual junction temperature range		0 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds		260	260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Curves, Figure 1 and Figure 2.

THERMAL INFORMATION

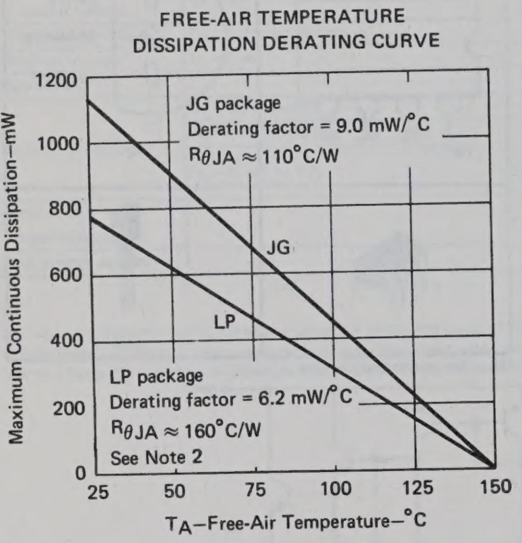

FIGURE 1

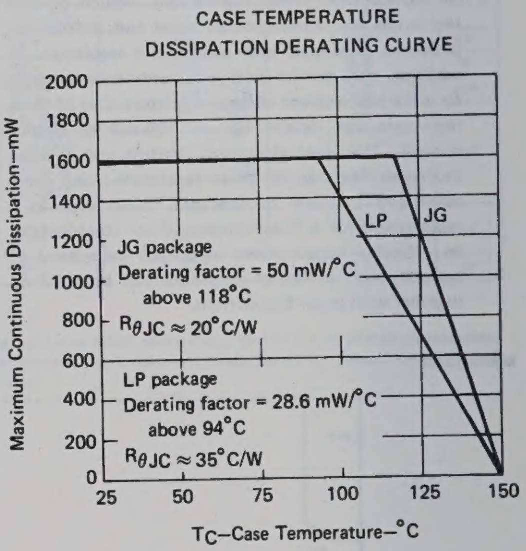

FIGURE 2

NOTE 2: This curve for the LP package is based on thermal resistance, $R_{\theta JA}$, measured in still air with the device mounted in an Augat socket. The bottom of the package was 3/8 inch above the socket.

recommended operating conditions

	uA78L02AC uA78L02C		uA78L05AC uA78L05C		uA78L06AC uA78L06C		uA78L08AC uA78L08C		uA78L12AC uA78L12C		uA78L15AC uA78L15C		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4.75	20	7	20	8.5	20	10.5	23	14.5	27	17.5	30	V
Output current, I_O		100		100		100		100		100		100	mA
Operating virtual junction temperature, T_J	0	125	0	125	0	125	0	125	0	125	0	125	°C

uA78L02AC, uA78L02C electrical characteristics at specified virtual junction temperature, V_I = 9 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L02AC			uA78L02C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage		25°C	2.5	2.6	2.7	2.4	2.6	2.8	V
	V_I = 4.75 V to 20 V, I_O = 1 mA to 40 mA	0°C to 125°C	2.45		2.75	2.35		2.85	
	I_O = 1 mA to 70 mA		2.45		2.75	2.35		2.85	
Input regulation	V_I = 4.75 V to 20 V	25°C		40	100		40	125	mV
	V_I = 5 V to 20 V			30	75		30	100	
Ripple rejection	V_I = 6 V to 16 V, f = 120 Hz	25°C	43	51		42	51		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		10	50		10	50	mV
	I_O = 1 mA to 40 mA			4	25		4	25	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		30			30		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.6	6		3.6	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 5 V to 20 V	0°C to 125°C			2.5			2.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L05AC, uA78L05C electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L05AC			uA78L05C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage		25°C	4.8	5	5.2	4.6	5	5.4	V
	V_I = 7 V to 20 V, I_O = 1 mA to 40 mA	0°C to 125°C	4.75		5.25	4.5		5.5	
	I_O = 1 mA to 70 mA		4.75		5.25	4.5		5.5	
Input regulation	V_I = 7 V to 20 V	25°C		25	150		25	200	mV
	V_I = 8 V to 20 V			20	100		20	150	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	25°C	41	49		40	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		17	60		17	60	mV
	I_O = 1 mA to 40 mA			7	30		7	30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.8	6		3.8	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 8 V to 20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

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†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78L06AC, uA78L06C electrical characteristics at specified virtual junction temperature, V_I = 12 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]		uA78L06AC MIN	uA78L06AC TYP	uA78L06AC MAX	uA78L06C MIN	uA78L06C TYP	uA78L06C MAX	UNIT
Output voltage		25°C	5.95	6.2	6.45	5.7	6.2	6.7	V
	V_I = 8.5 V to 20 V, I_O = 1 mA to 40 mA	0°C to 125°C	5.9		6.5	5.6		6.8	
	I_O = 1 mA to 70 mA		5.9		6.5	5.6		6.8	
Input regulation	V_I = 8.5 V to 20 V	25°C		25	175		25	200	mV
	V_I = 9 V to 20 V			20	125		20	150	
Ripple rejection	V_I = 10 V to 20 V, f = 120 Hz	25°C	40	46		39	46		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		20	80		20	80	mV
	I_O = 1 mA to 40 mA			9	40		9	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		50			50		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		3.9	6		3.9	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 9 V to 20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L08AC, uA78L08C electrical characteristics at specified virtual junction temperature, V_I = 14 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]		uA78L08AC MIN	uA78L08AC TYP	uA78L08AC MAX	uA78L08C MIN	uA78L08C TYP	uA78L08C MAX	UNIT
Output voltage		25°C	7.7	8	8.3	7.36	8	8.64	V
	V_I = 10.5 V to 23 V, I_O = 1 mA to 40 mA	0°C to 125°C	7.6		8.4	7.2		8.8	
	I_O = 1 mA to 70 mA		7.6		8.4	7.2		8.8	
Input regulation	V_I = 10.5 V to 23 V	25°C		25	175		25	200	mV
	V_I = 11 V to 23 V			20	125		20	150	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	25°C	37	44		36	44		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		25	80		25	80	mV
	I_O = 1 mA to 40 mA			10	40		10	40	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		60			60		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4	6		4	6	mA
		125°C			5.5			5.5	
Bias current change	V_I = 11 V to 23 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

[†] All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78L12AC, uA78L12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L12AC			uA78L12C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage		25°C	11.5	12	12.5	11.1	12	12.9	V
	V_I = 14.5 V to 27 V, I_O = 1 mA to 40 mA	0°C to 125°C	11.4		12.6	10.8		13.2	
	I_O = 1 mA to 70 mA		11.4		12.6	10.8		13.2	
Input regulation	V_I = 14.5 V to 27 V	25°C		55	250		55	250	mV
	V_I = 16 V to 27 V			45	200		45	200	
Ripple rejection ratio	V_I = 15 V to 25 V, f = 120 Hz	25°C	37	42		36	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		30	100		30	100	mV
	I_O = 1 mA to 40 mA			12	50		12	50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.2	6.5		4.2	6.5	mA
		125°C			6			6	
Bias current change	V_I = 16 V to 27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

uA78L15AC, uA78L15C electrical characteristics at specified virtual junction temperature, V_I = 23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA78L15AC			uA78L15C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage		25°C	14.4	15	15.6	13.8	15	16.2	V
	V_I = 17.5 V to 30 V, I_O = 1 mA to 40 mA	0°C to 125°C	14.25		15.75	13.5		16.5	
	I_O = 1 mA to 70 mA		14.25		15.75	13.5		16.5	
Input regulation	V_I = 17.5 V to 30 V	25°C		70	300		70	300	mV
	V_I = 20 V to 30 V			55	250		55	250	
Ripple rejection ratio	V_I = 18.5 V to 28.5 V, f = 120 Hz	25°C	34	39		33	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C		30	150		30	150	mV
	I_O = 1 mA to 40 mA			12	75		12	75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		µV
Dropout voltage		25°C		1.7			1.7		V
Bias current		25°C		4.4	6.5		4.4	6.5	mA
		125°C			6			6	
Bias current change	V_I = 20 V to 30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.1			0.2	

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†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME
IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

LINEAR INTEGRATED CIRCUITS

SERIES uA78M00 POSITIVE-VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612403, JUNE 1976

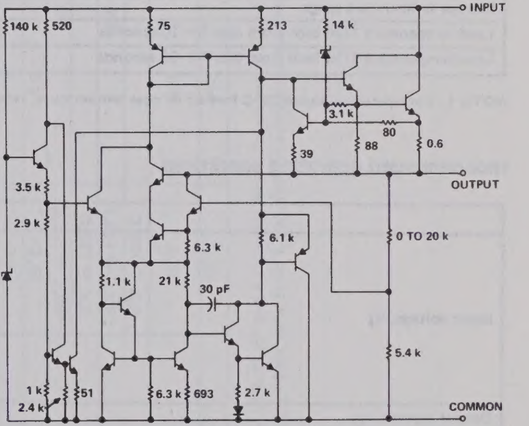
- 3-Terminal Regulators
- Output Current up to 500 mA
- No external components
- Internal Thermal Overload Protection
- Direct Placements for Fairchild μA78M00 Series and National LM341 Series
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

NOMINAL OUTPUT VOLTAGE	–55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
5 V	uA78M05M	uA78M05C
6 V	uA78M06M	uA78M06C
8 V	uA78M08M	uA78M08C
12 V	uA78M12M	uA78M12C
15 V	uA78M15M	uA78M15C
20 V	uA78M20M	uA78M20C
24 V	uA78M24M	uA78M24C
PACKAGES	LA	KC, KD, and LA

description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. One of these regulators can deliver up to 500 milliamperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overlaod. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic

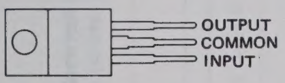


Resistor values shown are nominal and in ohms.

terminal assignments

KC PACKAGE

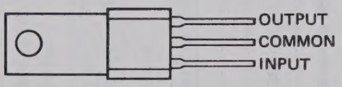
(TOP VIEW)



TO-220AB

KD PACKAGE

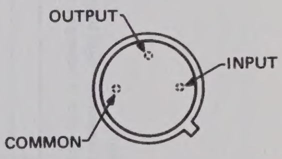
(TOP VIEW)



TO-202AB

LA PACKAGE

(TOP VIEW)



SERIES uA78M00
POSITIVE-VOLTAGE REGULATORS

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA78M05M THRU uA78M24M	uA78M05C THRU uA78M24C	UNIT
Input voltage	uA78M20, uA78M24	40	40	V
	All others	35	35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)	KC (TO-220AB) package	2	2	W
	KD(TO-202AB) package	1.5	1.5	
	LA package	0.6	0.6	
Continuous total dissipation at (or below)25°C case temperature (see Note 1)	KC and KD packages	7.5	7.5	W
	LA package	5	5	
Operating free-air, case, or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	KC and KD packages		260	°C
Lead temperature 1/16 inch from case for 60 seconds	LA package	300	300	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Curves, Figures 1 through 4.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA78M05M, uA78M05C	7	25	V
	uA78M06M, uA78M06C	8	25	
	uA78M08M, uA78M08C	10.5	25	
	uA78M12M, uA78M12C	14.5	30	
	uA78M15M, uA78M15C	17.5	30	
	uA78M20M, uA78M20C	23	35	
	uA78M24M, uA78M24C	27	38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J	uA78M05M thru uA78M24M	−55	150	°C
	uA78M05C thru uA78M24C	0	125	

uA78M05M, uA78M05C electrical characteristics at specified virtual junction temperature, $V_I = 10$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M05M			uA 78M05C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	4.8	5	5.2	4.8	5	5.2	V
	$I_O = 5$ mA to 350 mA	$V_I = 8$ V to 20 V	–55° C to 150°C	4.7		5.3				
		$V_I = 7$ V to 20 V	0°C to 125°C				4.75		5.25	
Input regulation	$I_O = 200$ mA	$V_I = 7$ V to 25 V	25°C		3	50		3	100	mV
		$V_I = 8$ V to 20 V			1	25				
		$V_I = 8$ V to 25 V						1	50	
Ripple rejection	$V_I = 8$ V to 18 V, f = 120 Hz	$I_O = 100$ mA	–55°C to 150°C	62						dB
			0°C to 125°C				62			
		$I_O = 300$ mA	25°C	62	80		62	80		
Output regulation	$I_O = 5$ mA to 500 mA		25°C		20	50		20	100	mV
	$I_O = 5$ mA to 200 mA				10	25		10	50	
Temperature coefficient of output voltage	$I_O = 5$ mA		–55°C to 150°C		–1					mV/°C
			0°C to 125°C					–1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		40			40		μV
Dropout voltage			25°C		2			2		V
Bias current			25°C		4.5	6		4.5	6	mA
Bias current change	$I_O = 200$ mA, $V_I = 8$ V to 25 V		–55°C to 150°C			0.8				mA
			0°C to 125°C						0.8	
	$I_O = 5$ mA to 350 mA		–55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	$V_I = 35$ V		25°C		300			300		mA
Peak output current			25°C		700			700		A

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78M06M, uA78M06C electrical characteristics at specified virtual junction temperature, V_I = 11 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M06M			uA78M06C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	5.75	6	6.25	5.75	6	6.25	V
	I_O = 5 mA to 350 mA	V_I = 9 V to 21 V	−55°C to 150°C	5.7		6.3				
		V_I = 8 V to 21 V	0°C to 125°C				5.7		6.3	
Input regulation	I_O = 200 mA	V_I = 8 V to 25 V	25°C		5	60		5	100	mV
		V_I = 9 V to 20 V			1.5	30				
		V_I = 9 V to 25 V						1.5	50	
Ripple rejection	V_I = 9 V to 19 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	59						dB
			0°C to 125°C				59			
		I_O = 300 mA	25°C	59	80		59	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		20	60		20	120	mV
	I_O = 5 mA to 200 mA				10	30		10	60	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−0.5					mV/°C
			0°C to 125°C					−0.5		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		45			45		µV
Dropout voltage			25°C		2			2		V
Bias current			25°C		4.5	6		4.5	6	mA
Bias current change	I_O = 200 mA, V_I = 9 V to 25 V		−55°C to 150°C			0.8				mA
			0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		270			270		mA
Peak output current			25°C		700			700		A

†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78M08M, uA78M08C electrical characteristics at specified virtual junction temperature, $V_I = 14$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M08M			uA78M08C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	7.7	8	8.3	7.7	8	8.3	V
	I_O = 5 mA to 350 mA	V_I = 11.5 V to 23 V	−55° C to 150°C	7.6		8.4				
		V_I = 10.5 V to 23 V	0°C to 125°C				7.6		8.4	
Input regulation	I_O = 200 mA	V_I = 10.5 V to 25 V	25°C		6	60		6	100	mV
		V_I = 11 V to 20 V			2	30				
		V_I = 11 V to 25 V						2	50	
Ripple rejection	V_I = 11.5 V to 21.5 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	56						dB
			0°C to 125°C				56			
		I_O = 300 mA	25°C	56	80		56	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	80		25	160	mV
	I_O = 5 mA to 200 mA				10	40		10	80	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−0.5					mV/°C
			0°C to 125°C					−0.5		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		52			52		μV
Dropout voltage			25°C		2			2		V
Bias current			25°C		4.6	6		4.6	6	mA
Bias current change	I_O = 200 mA	V_I = 11.5 V to 25 V	−55°C to 150°C			0.8				mA
		V_I = 10.5 V to 25 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		250			250		mA
Peak output current			25°C		700			700		A

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78M12M, uA78M12C electrical characteristics at specified virtual junction temperature, V_I = 19 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]			uA78M12M			uA78M12C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	11.5	12	12.5	11.5	12	12.5	V
	I_O = 5 mA to 350 mA	V_I = 15.5 V to 27 V	−55° C to 150°C	11.4		12.6				
		V_I = 14.5 V to 27 V	0°C to 125°C				11.4		12.6	
Input regulation	I_O = 200 mA	V_I = 14.5 V to 30 V	25°C		8	60		8	100	mV
		V_I = 16 V to 25 V			2	30				
		V_I = 16 V to 30 V						2	50	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	55						dB
			0°C to 125° C				55			
		I_O = 300 mA	25°C	55	80		55	80		
Output regulation	I_O = 5 mA to 500 mA		25°C		25	120		25	240	mV
	I_O = 5 mA to 200 mA				10	60		10	120	
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−1					mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		75			75		μV
Dropout voltage			25°C		2			2		V
Bias current			25°C		4.8	6		4.8	6	mA
Bias current change	I_O = 200 mA	V_I = 15 V to 30 V	−55°C to 150°C			0.8				mA
		V_I = 14.5 V to 30 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		240			240		mA
Peak output current			25°C		700			700		A

[†] All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78M15M, uA78M15C electrical characteristics at specified virtual junction temperature, $V_I = 23$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M15M			uA78M15C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	14.4	15	15.6	14.4	15	15.6	V
	$I_O = 5$ mA to 350 mA	$V_I = 18.5$ V to 30 V	–55° C to 150°C	14.25		15.75				
		$V_I = 17.5$ V to 30 V	0°C to 125°C				14.75		15.75	
Input regulation	$I_O = 200$ mA	$V_I = 17.5$ V to 30 V	25°C		10	60		10	100	mV
		$V_I = 20$ V to 30 V			3	30		3	50	
Ripple rejection	$V_I = 18.5$ V to 28.5 V, f = 120 Hz	$I_O = 100$ mA	–55°C to 150°C	54						dB
			0°C to 125°C				54			
		$I_O = 300$ mA	25°C	54	70		54	70		
Output regulation	$I_O = 5$ mA to 500 mA		25°C		25	150		25	300	mV
	$I_O = 5$ mA to 200 mA				10	75		10	150	
Temperature coefficient of output voltage	$I_O = 5$ mA		–55°C to 150°C		–1					mV/°C
			0°C to 125°C					–1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		90			90		μV
Dropout voltage			25°C		2			2		V
Bias current			25°C		4.8	6		4.8	6	mA
Bias current change	$I_O = 200$ mA	$V_I = 18.5$ V to 30 V	–55°C to 150°C			0.8				mA
		$V_I = 17.5$ V to 30 V	0°C to 125°C						0.8	
	$I_O = 5$ mA to 350 mA		–55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	$V_I = 35$ V		25°C		240			240		mA
Peak output current			25°C		700			700		A

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78M20M, uA78M20C electrical characteristics at specified virtual junction temperature, V_I = 29 V, I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]			uA78M20M MIN	uA78M20M TYP	uA78M20M MAX	uA78M20C MIN	uA78M20C TYP	uA78M20C MAX	UNIT
Output voltage			25°C	19.2	20	20.8	19.2	20	20.8	V
	I_O = 5 mA to 350 mA	V_I = 24 V to 35 V	–55° C to 150°C	19		21				
		V_I = 23 V to 35 V	0°C to 125°C				19		21	
Input regulation	I_O = 200 mA	V_I = 23 V to 35 V	25°C		10	60		10	100	mV
		V_I = 24 V to 35 V			5	30		5	50	
Ripple rejection	V_I = 24 V to 34 V, f = 120 Hz	I_O = 100 mA	–55°C to 150°C	53						dB
			0°C to 125°C				53			
		I_O = 300 mA	25°C	53	70		53	70		
Output regulation	I_O = 5 mA to 500 mA		25°C		30	200		30	400	mV
	I_O = 5 mA to 200 mA				10	100		10	200	
Temperature coefficient of output voltage	I_O = 5 mA		–55°C to 150°C		–1.1					mV/°C
			0°C to 125°C					–1.1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		110			110		µV
Dropout voltage			25°C		2			2		V
Bias current			25°C		4.9	6		4.9	6	mA
Bias current change	I_O = 200 mA	V_I = 24 V to 35 V	–55°C to 150°C			0.8				mA
		V_I = 23 V to 35 V	0°C to 125°C						0.8	
	I_O = 5 mA to 350 mA		–55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Short-circuit output current	V_I = 35 V		25°C		240			240		mA
Peak output current			25°C		700			700		A

[†] All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leqslant$ 10 ms, duty cycle $\leqslant$ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA78M24M, uA78M24C electrical characteristics at specified virtual junction temperature, $V_I = 33$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA78M24M			uA78M24C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	23	24	25	23	24	25	V
	I_O = 5 mA to 350 mA	V_I = 28 V to 38 V	–55° C to 150° C	22.8		25.2				
		V_I = 27 V to 38 V	0° C to 125° C				22.8		25.2	
Input regulation	I_O = 200 mA	V_I = 27 V to 38 V	25° C		10	60		10	100	mV
		V_I = 30 V to 36 V			5	30				
		V_I = 28 V to 38 V						5	50	
Ripple rejection	V_I = 28 V to 38 V, f = 120 Hz	I_O = 100 mA	–55° C to 150° C	50						dB
			0° C to 125° C				50			
		I_O = 300 mA	25° C	50	70		50	70		
Output regulation	I_O = 5 mA to 500 mA		25° C		30	240		30	480	mV
	I_O = 5 mA to 200 mA				10	120		10	240	
Temperature coefficient of output voltage	I_O = 5 mA		–55° C to 150° C		–1.2					mV/°C
			0° C to 125° C					–1.2		
Output noise voltage	f = 10 Hz to 100 kHz		25° C		170			170		µV
Dropout voltage			25° C		2			2		V
Bias current			25° C		5	6		5	6	mA
Bias current change	I_O = 200 mA	V_I = 28 V to 38 V	–55° C to 150° C			0.8				mA
		V_I = 27 V to 38 V	0° C to 125° C						0.8	
	I_O = 5 mA to 350 mA		–55° C to 150° C			0.5				
			0° C to 125° C						0.5	
Short-circuit output current	V_I = 35 V		25° C		240			240		mA
Peak output current			25° C		700			700		A

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† All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

THERMAL INFORMATION

KC AND KD PACKAGES FREE-AIR TEMPERATURE DISSIPATION DERATING CURVES

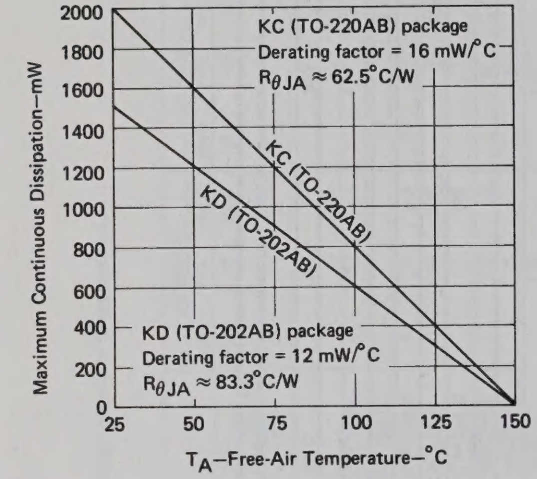


FIGURE 1

KC AND KD PACKAGES CASE TEMPERATURE DISSIPATION DERATING CURVES

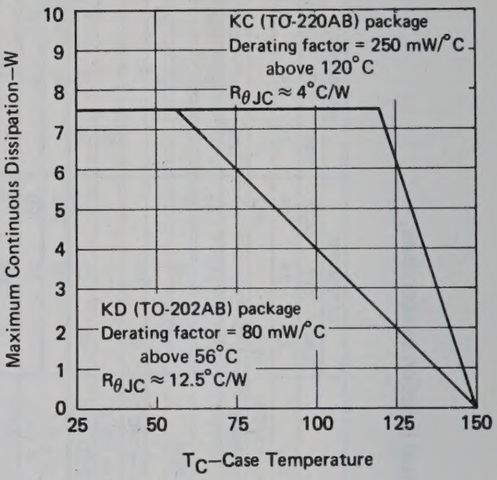


FIGURE 2

LA PACKAGE FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

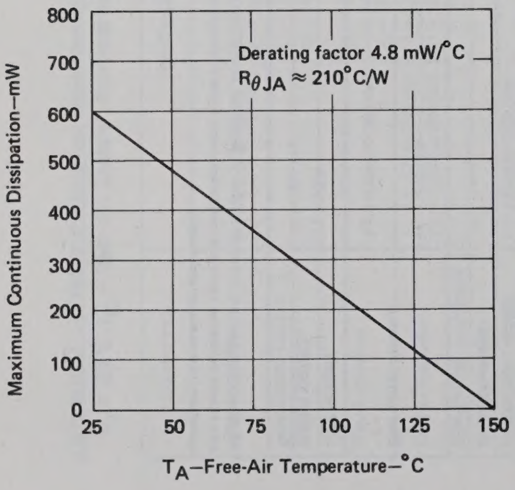


FIGURE 3

LA PACKAGE CASE TEMPERATURE DISSIPATION DERATING CURVE

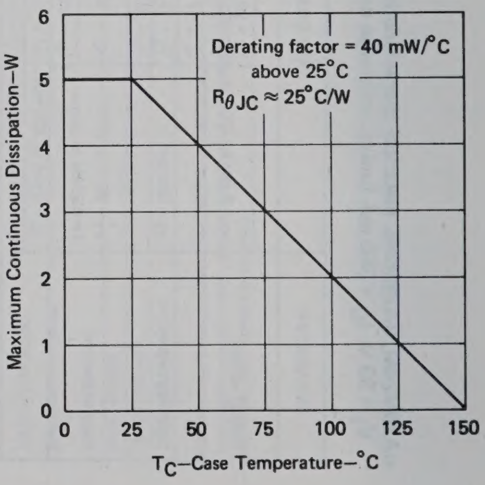


FIGURE 4

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

SERIES uA7900
NEGATIVE-VOLTAGE REGULATORS

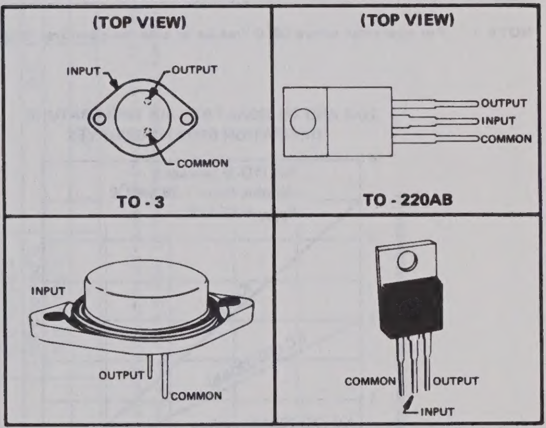
BULLETIN NO. DL-S 7612404, JUNE 1976

- 3-Terminal Regulators
- Output Current up to 1.5 A
- No External Components
- Internal Thermal Overload Protection
- Direct Replacements for Fairchild μA7900 Series
- Essentially Equivalent to National LM 320 Series
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

NOMINAL OUTPUT VOLTAGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
−5 V	uA7905M	uA7905C
−6 V	uA7906M	uA7906C
−8 V	uA7908M	uA7908C
−12 V	uA7912M	uA7912C
−15 V	uA7915M	uA7915C
−18 V	uA7918M	uA7918C
−24 V	uA7924M	uA7924C
PACKAGES	KA	KA and KC

KA PACKAGE
(TOP VIEW)

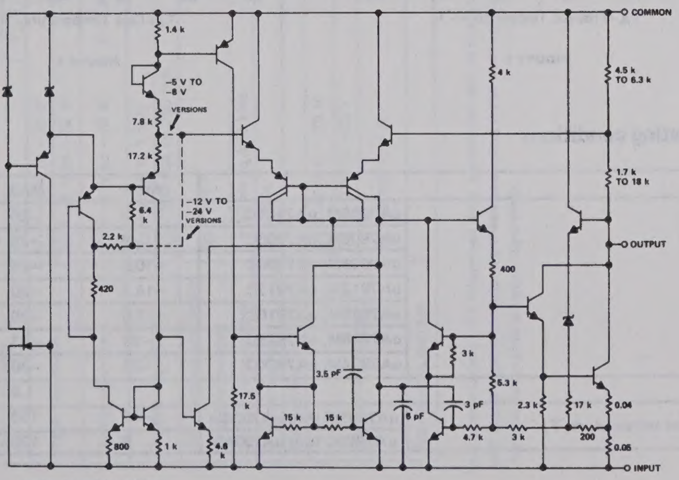
KC PACKAGE
(TOP VIEW)


INPUT
OUTPUT
COMMON
TO-3
OUTPUT
INPUT
COMMON
TO-220AB
INPUT
OUTPUT
COMMON
COMMON
OUTPUT
INPUT

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA7800 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. One of these regulators can deliver up to 1.5 amperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic


COMMON
1.4 k
−5 V TO −8 V VERSIONS
7.8 k
17.2 k
6.4 k
−12 V TO −24 V VERSIONS
2.2 k
420
4 k
4.5 k TO 6.3 k
1.7 k TO 18 k
OUTPUT
400
3 k
3.5 pF
17.5 k
15 k
15 k
6 pF
3 pF
6.3 k
2.3 k
17 k
0.04
4.7 k
3 k
200
0.05
800
1 k
4.6 k
INPUT

Resistor values shown are nominal and in ohms.

SERIES uA7900
NEGATIVE-VOLTAGE REGULATORS

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA7905M THRU uA7924M	uA7905C THRU uA7924C	UNIT
Input voltage	uA7924M, uA7924C	−40	−40	V
	All others	−35	−35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)	KA (TO-3) package	3.5	3.5	W
	KC (TO-220AB) package		2	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)		15	15	W
Operating free-air, case, or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/8 inch from case for 60 seconds	KA (TO-3) package	300	300	°C
Lead temperature 1/8 inch from case for 10 seconds	KC (TO-220AB) package		260	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Curves, Figure 1 and Figure 2.

TO-3 AND TO-220AB FREE-AIR TEMPERATURE DISSIPATION DERATING CURVES

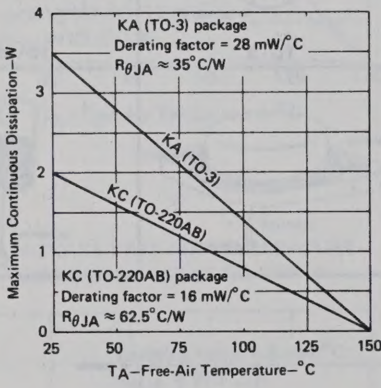


FIGURE 1

TO-3 AND TO-220AB CASE TEMPERATURE DISSIPATION DERATING CURVE

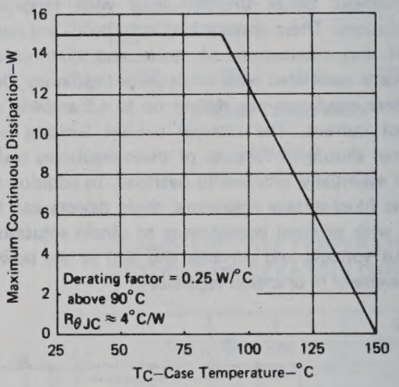


FIGURE 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA7905M, uA7905C	−7	−25	V
	uA7906M, uA7906C	−8	−25	
	uA7908M, uA7908C	−10.5	−25	
	uA7912M, uA7912C	−14.5	−30	
	uA7915M, uA7915C	−17.5	−30	
	uA7918M, uA7918C	−21	−33	
	uA7924M, uA7924C	−27	−38	
Output current, I_O			1.5	A
Operating virtual junction temperature, T_J	uA7905M thru uA7924M	−55	150	°C
	uA7905C thru uA7924C	0	125	

uA7905M, uA7905C electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7905M			uA7905C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	–4.8	–5	–5.2	–4.8	–5	–5.2	V
	$I_O = 5$ mA to 1 A, $P \leq 15$ W	$V_I = -8$ V to -20 V	–55°C to 150°C	–4.7		–5.3				
		$V_I = -7$ V to -20 V	0°C to 125°C				–4.75		–5.25	
Input regulation	$V_I = -7$ V to -25 V		25°C		3	50		3	100	mV
	$V_I = -8$ V to -12 V				1	25		1	50	
Ripple rejection	$V_I = -8$ V to -18 V,	f = 120 Hz	–55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	$I_O = 5$ mA to 1.5 A		25°C		15	50		15	100	mV
	$I_O = 250$ mA to 750 mA				5	25		5	50	
Temperature coefficient of output voltage	$I_O = 5$ mA		0°C to 150°C		–0.4					mV/°C
			0°C to 125°C					–0.4		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		125			125		μV
Dropout voltage	$I_O = 1$ A		25°C		1.1			1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	$V_I = -8$ V to -25 V		–55°C to 150°C			1.3				mA
	$V_I = -7$ V to -25 V		0°C to 125°C						1.3	
	$I_O = 5$ mA to 1 A		–55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

---

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7906M, uA7906C electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[†]			uA7906M			uA7906C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	–5.75	–6	–6.25	–5.75	–6	–6.25	V
	I_O = 5 mA to 1 A, P ⩽ 15 W	V_I = –9 V to –21 V	–55°C to 150°C	–5.65		–6.35				
		V_I = –8 V to –21 V	0°C to 125°C				–5.7		–6.3	
Input regulation	V_I = –8 V to –25 V		25°C		5	60	5		120	mV
	V_I = –9 V to –13 V				1.5	30		1.5	60	
Ripple rejection	V_I = –9 V to –19 V,	f = 120 Hz	–55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	I_O = 5 mA to 1.5 A		25°C		14	60		14	120	mV
	I_O = 250 mA to 750 mA				4	30		4	60	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		–0.4					mV/°C
			0°C to 125°C					–0.4		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		150			150		µV
Dropout voltage	I_O = 1 A		25°C		1.1			1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = –9 V to –25 V		–55°C to 150°C			1.3				mA
	V_I = –8 V to –25 V		0°C to 125°C						1.3	
	I_O = 5 mA to 1 A		–55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

[†] All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leqslant 10$ ms, duty cycle ⩽ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7908M, uA7908C electrical characteristics at specified virtual junction temperature, $V_I = -14$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7908M			uA7908C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
			25°C	−7.7	−8	−8.3	−7.7	−8	−8.3	V
Output voltage	$I_O = 5$ mA to 1 A, $P \leq 15$ W	$V_I = -11.5$ V to −23 V	−55°C to 150°C	−7.6		−8.4				
		$V_I = -10.5$ V to −23 V	0°C to 125°C				−7.6		−8.4	
Input regulation	$V_I = -10.5$ V to −25 V		25°C		6	80		6	160	mV
	$V_I = -11$ V to −17 V				2	40		2	80	
Ripple rejection	$V_I = -11.5$ V to −21.5 V, f = 120 Hz		−55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	$I_O = 5$ mA to 1.5 A		25°C		12	80		12	160	mV
	$I_O = 250$ mA to 750 mA				4	40		4	80	
Temperature coefficient of output voltage	$I_O = 5$ mA		0°C to 150°C		−0.6					mV/°C
			0°C to 125°C					−0.6		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		200			200		μV
Dropout voltage	$I_O = 1$ A		25°C		1.1			1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	$V_I = -11.5$ V to −25 V		−55°C to 150°C			1				mA
	$V_I = -10.5$ V to −25 V		0°C to 125°C						1	
	$I_O = 5$ mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

[†] All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7912M, uA7912C electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7912M			uA7912C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−11.5	−12	−12.5	−11.5	−12	−12.5	V
	$I_O = 5$ mA to 1 A, $P \leq 15$ W	$V_I = -15.5$ V to −27 V	−55°C to 150°C	−11.4		−12.6				
		$V_I = -14.5$ V to −27 V	0°C to 125°C				−11.4		−12.6	
Input regulation	$V_I = -14.5$ V to −30 V		25°C		10	120		10	240	mV
	$V_I = -16$ V to −22 V				3	60		3	120	
Ripple rejection	$V_I = -15$ V to −25 V, f = 120 Hz		−55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	$I_O = 5$ mA to 1.5 A		25°C		12	120		12	240	mV
	$I_O = 250$ mA to 750 mA				4	60		4	120	
Temperature coefficient of output voltage	$I_O = 5$ mA		0°C to 150°C		−0.8					mV/°C
			0°C to 125°C					−0.8		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		300			300		μV
Dropout voltage	$I_O = 1$ A		25°C		1.1			1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	$V_I = -15$ V to −30 V		−55°C to 150°C			1				mA
	$V_I = -14.5$ V to − 30 V		0°C to 125°C						1	
	$I_O = 5$ mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

† All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7915M, uA7915C electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7915M MIN	uA7915M TYP	uA7915M MAX	uA7915C MIN	uA7915C TYP	uA7915C MAX	UNIT
Output voltage			25°C	−14.4	−15	−15.6	−14.4	−15	−15.6	V
	I_O = 5 mA to 1 A, P ≤ 15 W	V_I = −18.5 V to −30 V	−55°C to 150°C	−14.25		−15.75				
		V_I = −17.5 V to −30 V	0°C to 125°C				−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V		25°C		11	150		11	300	mV
	V_I = −20 V to −26 V				3	75		3	150	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz		−55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	I_O = 5 mA to 1.5 A		25°C		12	150		12	300	mV
	I_O = 250 mA to 750 mA				4	75		4	150	
Temperature coefficient of output voltage	I_O = 5 mA		0°C to 150°C		−1					mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		375			375		µV
Dropout voltage	I_O = 1 A		25°C		1.1			1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −18.5 V to − 30 V		−55°C to 150°C			1				mA
	V_I = −17.5 V to −30 V		0°C to 125°C						1	
	I_O = 5 mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

† All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7918M, uA7918C electrical characteristics at specified virtual junction temperature, $V_I = -27$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7918M			uA7918C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−17.3	−18	−18.7	−17.3	−18	−18.7	V
	$I_O = 5$ mA to 1 A, $P \leq 15$ W	$V_I = -22$ V to -33 V	−55°C to 150°C	−17.1		−18.9				
		$V_I = -21$ V to -33 V	0°C to 125°C				−17.1		−18.9	
Input regulation	$V_I = -21$ V to -33 V		25°C		15	180		15	360	mV
	$V_I = -24$ V to -30 V				5	90		5	180	
Ripple rejection	$V_I = -22$ V to -32 V,	f = 120 Hz	−55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	$I_O = 5$ mA to 1.5 A		25°C		12	180		12	360	mV
	$I_O = 250$ mA to 750 mA				4	90		4	180	
Temperature coefficient of output voltage	$I_O = 5$ mA		0°C to 150°C		−1					mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		450			450		μV
Dropout voltage	$I_O = 1$ A		25°C		1.1			1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	$V_I = -22$ V to -33 V		−55°C to 150°C			1				mA
	$V_I = -21$ V to -33 V		0°C to 125°C						1	
	$I_O = 5$ mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

†All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA7924M, uA7924C electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 500$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA7924M			uA7924C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−23	−24	−25	−23	−24	−25	V
	$I_O = 5$ mA to 1 A, $P \leq 15$ W	$V_I = -28$ V to -38 V	−55°C to 150°C	−22.8		−25.2				
		$V_I = -27$ V to -38 V	0°C to 125°C				−22.8		−25.2	
Input regulation	$V_I = -27$ V to -38 V		25°C		18	240		18	480	mV
	$V_I = -30$ V to -36 V				6	120		6	240	
Ripple rejection	$V_I = -28$ V to -38 V,	f = 120 Hz	−55°C to 150°C	54	60					dB
			0°C to 125°C				54	60		
Output regulation	$I_O = 5$ mA to 1.5 A		25°C		12	240		12	480	mV
	$I_O = 250$ mA to 750 mA				4	120		4	240	
Temperature coefficient of output voltage	$I_O = 5$ mA		0°C to 150°C		−1					mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		600			600		µV
Dropout voltage	$I_O = 1$ A		25°C		1.1			1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	$V_I = -28$ V to -38 V		−55°C to 150°C			1				mA
	$V_I = -27$ V to -38 V		0°C to 125°C						1	
	$I_O = 5$ mA to 1 A		−55°C to 150°C			0.5				
			0°C to 125°C						0.5	
Peak output current			25°C		2.1			2.1		A

†All characteristics are measured with a capacitor across the input of 0.33 µF and a capacitor across the output of 0.1 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

SERIES uA79M00
NEGATIVE-VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612405, JUNE 1976

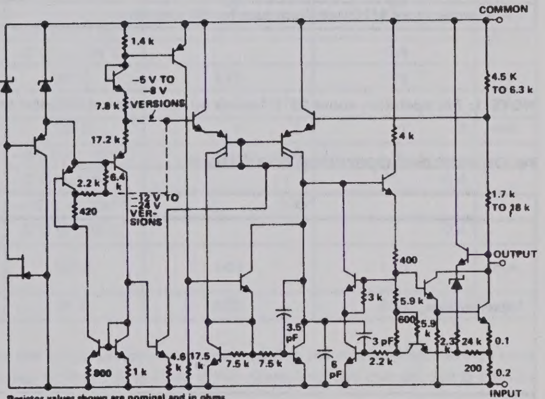
- 3-Terminal Regulators
- Output Current up to 500 mA
- No External Components
- Internal Thermal Overload Protection
- Direct Placements for Fairchild μA79M00 Series
- High Power Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

NOMINAL OUTPUT VOLTAGE	−55°C TO 150°C OPERATING TEMPERATURE RANGE	0°C TO 125°C OPERATING TEMPERATURE RANGE
−5 V	uA79M05M	uA79M05C
−6 V	uA79M06M	uA79M06C
−8 V	uA79M08M	uA79M08C
−12 V	uA79M12M	uA79M12C
−15 V	uA79M15M	uA79M15C
−20 V	uA79M20M	uA79M20C
−24 V	uA79M24M	uA79M24C
PACKAGES	LA	KC, KD, and LA

description

This series of fixed-negative-voltage monolithic integrated-circuit voltage regulators is designed to complement Series uA78M00 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. One of these regulators can deliver up to 500 milliamperes of output current. The internal current limiting and thermal shutdown features of these regulators make them essentially immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

schematic

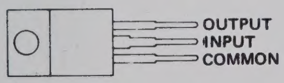

COMMON
1.4 k
−5 V TO −8 V VERSIONS
7.8 k
17.2 k
2.2 k
6.4 k
420
−12 V TO −24 V VERSIONS
4.5 K TO 6.3 k
4 k
1.7 k TO 18 k
OUTPUT
400
3 k
5.9 k
600
5.9 k
3.5 pF
3 pF
2.2 k
2.3 k
24 k
0.1
200
0.2
800
1 k
4.6 k
17.5 k
7.5 k
7.5 k
6 pF
INPUT

Resistor values shown are nominal and in ohms.

terminal assignments

KC PACKAGE

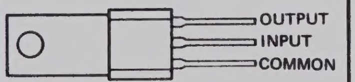
(TOP VIEW)


OUTPUT
INPUT
COMMON

TO-220AB

KD PACKAGE

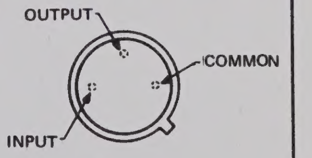
(TOP VIEW)


OUTPUT
INPUT
COMMON

TO-202AB

LA PACKAGE

(TOP VIEW)


OUTPUT
COMMON
INPUT

absolute maximum ratings over operating temperature range (unless otherwise noted)

		uA79M05M THRU uA79M24M	uA79M05C THRU uA79M24C	UNIT
Input voltage	uA79M20, uA79M24	−40	−40	V
	All others	−35	−35	
Continuous total dissipation at 25°C free-air temperature (see Note 1)	KC (TO-220AB) package	2	2	W
	KD TO-202AB package	1.5	1.5	
	LA package	0.6	0.6	
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	KC and KD package	7.5	7.5	W
	LA package	5	5	
Operating free-air, case or virtual junction temperature range		−55 to 150	0 to 150	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	KC and KD packages		260	°C
Lead temperature 1/16 inch from case for 60 seconds	LA package	300	300	°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to Dissipation Derating Curves, Figures 1 through 4.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	uA79M05	−7	−25	V
	uA79M06	−8	−25	
	uA79M08	−10.5	−25	
	uA70M12	−14.5	−30	
	uA79M15	−17.5	−30	
	uA79M18	−23	−35	
	uA79M24	−27	−38	
Output current, I_O			500	mA
Operating virtual junction temperature, T_J	uA79M05M thru uA79M24M	−55	150	°C
	uA79M05C thru uA79M24C	0	125	

uA79M05M, uA79M05C electrical characteristics at specified virtual junction temperature, $V_I = -10$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M05M			uA79M05C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−4.8	−5	−5.2	−4.8	−5	−5.2	V
	I_O = 5 mA to 350 mA, V_I = −7 V to −25 V		−55°C to 150°C	−4.75		−5.25				
			0°C to 125°C				−4.75		−5.25	
Input regulation	V_I = −7 V to −25 V		25°C		7	50		7	50	mV
	V_I = −8 V to −18 V				3	30		3	30	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	100		75	100	mV
	I_O = 5 mA to 350 mA				50			50		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−0.4					mV/°C
			0°C to 125°C					0.4		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		125			125		µV
Dropout voltage			25°C		1.1			1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −8 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V		25°C		140			140		mA
Peak output current			25°C		650			650		A

---

†All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA79M06M, uA79M06C electrical characteristics at specified virtual junction temperature, $V_I = -11$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M06M			uA79M06C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−5.75	−6	−6.25	−5.75	−6	−6.25	V
	I_O = 5 mA to 350 mA, V_I = −8 V to −25 V		−55°C to 150°C	−5.7		−6.3				
			0°C to 125°C				−5.7		−6.3	
Input regulation	V_I = −8 V to −25 V		25°C		7	60		7	60	mV
	V_I = −9 V to −19 V				3	40		3	40	
Ripple rejection	V_I = −9 V to −19 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		80	120		80	120	mV
	I_O = 5 mA to 350 mA				55			55		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−0.4					mV/°C
			0°C to 125°C					−0.4		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		150			150		μV
Dropout voltage			25°C		1.1			1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −9 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V		25°C		140			140		mA
Peak output current			25°C		650			650		A

†All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq$ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA79M08M, uA79M08C electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA (unless noted)

PARAMETER	TEST CONDITIONS†			uA79M08M			uA79M08C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−7.7	−8	−8.3	−7.7	−8	−8.3	V
	I_O = 5 mA to 350 mA, V_I = −10.5 V to −25 V		−55°C to 150°C	−7.6		−8.4				
			0°C to 125°C				−7.6		−8.4	
Input regulation	V_I = −10.5 V to −25 V		25°C		8	80		8	80	mV
	V_I = −11 V to −21 V				4	50		4	50	
Ripple rejection	V_I = −11.5 V to −21.5 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	59		54	59		
Output regulation	I_O = 5 mA to 500 mA		25°C		90	160		90	160	mV
	I_O = 5 mA to 350 mA				60			60		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−0.6					mV/°C
			0°C to 125°C					−0.6		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		200			200		μV
Dropout voltage			25°C		1.1			1.1		V
Bias current			25°C		1	2		1	2	mA
Bias current change	V_I = −10.5 V to −25 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V		25°C		140			140		mA
Peak output current			25°C		650			650		A

---

†All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA79M12M, uA79M12C electrical characteristics at specified virtual junction temperature, $V_I = -19$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M12M			uA79M12C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−11.5	−12	−12.5	−11.5	−12	−12.5	V
	I_O = 5 mA to 350 mA, V_I = −14.5 V to −30 V		−55°C to 150°C	−11.4		−12.6				
			0°C to 125°C				−11.4		−12.6	
Input regulation	V_I = −14.5 V to −30 V		25°C		9	80		9	80	mV
	V_I = −15 V to −25 V				5	50		5	50	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	60		54	60		
Output regulation	I_O = 5 mA to 500 mA		25°C		65	240		65	240	mV
	I_O = 5 mA to 350 mA				45			45		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−0.8					mV/°C
			0°C to 125°C					−0.8		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		300			300		µV
Dropout voltage			25°C		1.1			1.1		V
Bias current			25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −14.5 V to −30 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V		25°C		140			140		mA
Peak output current			25°C		650			650		A

---

†All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA79M15M, uA79M15C electrical characteristics at specified virtual junction temperature, $V_I = -23$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		uA79M15M MIN	uA79M15M TYP	uA79M15M MAX	uA79M15C MIN	uA79M15C TYP	uA79M15C MAX	UNIT
Output voltage		25°C	−14.4	−15	−15.6	−14.4	−15	−15.6	V
	I_O = 5 mA to 350 mA, V_I = −17.5 V to −30 V	−55°C to 150°C	−14.25		−15.75				
		0°C to 125°C				−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C		9	80		9	80	mV
	V_I = −18 V to −28 V			7	50		7	50	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz, I_O = 100 mA	−55°C to 150°C	50						dB
		0°C to 125°C				50			
	I_O = 300 mA	25°C	54	59		54	59		
Output regulation	I_O = 5 mA to 500 mA	25°C		65	240		65	240	mV
	I_O = 5 mA to 350 mA			45			45		
Temperature coefficient of output voltage	I_O = 5 mA	−55°C to 150°C		−1					mV/°C
		0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz	25°C		375			375		µV
Dropout voltage		25°C		1.1			1.1		V
Bias current		25°C		1.5	3		1.5	3	mA
Bias current change	V_I = −17.5 V to −30 V	−55°C to 150°C			0.4				mA
		0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA	−55°C to 150°C			0.4				
		0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V	25°C		140			140		mA
Peak output current		25°C		650			650		A

†All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq$ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA79M20M, uA79M20C electrical characteristics at specified virtual junction temperature, $V_I = -29$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M20M			uA79M20C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−19.2	−20	−20.8	−19.2	−20	−20.8	V
	I_O = 5 mA to 350 mA, V_I = −23 V to −35 V		−55°C to 150°C	−19		−21				
			0°C to 125°C				−19		−21	
Input regulation	V_I = −23 V to −35 V		25°C		12	80		12	80	mV
	V_I = −24 V to −34 V				10	70		10	70	
Ripple rejection	V_I = −24 V to −34 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	58		54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300		75	300	mV
	I_O = 5 mA to 350 mA				50			50		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−1					mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		500			500		µV
Dropout voltage			25°C		1.1			1.1		V
Bias current			25°C		1.5	3.5		1.5	3.5	mA
Bias current change	V_I = −23 V to −35 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V		25°C		140			140		mA
Peak output current			25°C		650			650		A

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† All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

uA79M24M, uA79M24C electrical characteristics at specified virtual junction temperature, $V_I = -33$ V, $I_O = 350$ mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			uA79M24M			uA79M24C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage			25°C	−23	−24	−25	−23	−24	−25	V
	I_O = 5 mA to 350 mA, V_I = −27 V to −38 V		−55°C to 150°C	−22.8		−25.2				
			0°C to 125°C				−22.8		−25.2	
Input regulation	V_I = −27 V to −38 V		25°C		12	80		12	80	mV
	V_I = −28 V to −38 V				12	70		12	70	
Ripple rejection	V_I = −28 V to −38 V, f = 120 Hz	I_O = 100 mA	−55°C to 150°C	50						dB
			0°C to 125°C				50			
		I_O = 300 mA	25°C	54	58		54	58		
Output regulation	I_O = 5 mA to 500 mA		25°C		75	300		75	300	mV
	I_O = 5 mA to 350 mA				50			50		
Temperature coefficient of output voltage	I_O = 5 mA		−55°C to 150°C		−1					mV/°C
			0°C to 125°C					−1		
Output noise voltage	f = 10 Hz to 100 kHz		25°C		600			600		µV
Dropout voltage			25°C		1.1			1.1		V
Bias current			25°C		1.5	3.5		1.5	3.5	mA
Bias current change	V_I = −27 V to −38 V		−55°C to 150°C			0.4				mA
			0°C to 125°C						0.4	
	I_O = 5 mA to 350 mA		−55°C to 150°C			0.4				
			0°C to 125°C						0.4	
Short circuit output current	V_I = −30 V		25°C		140			140		mA
Peak output current			25°C		650			650		A

---

†All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leqslant 10$ ms, duty cycle $\leqslant$ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

THERMAL INFORMATION

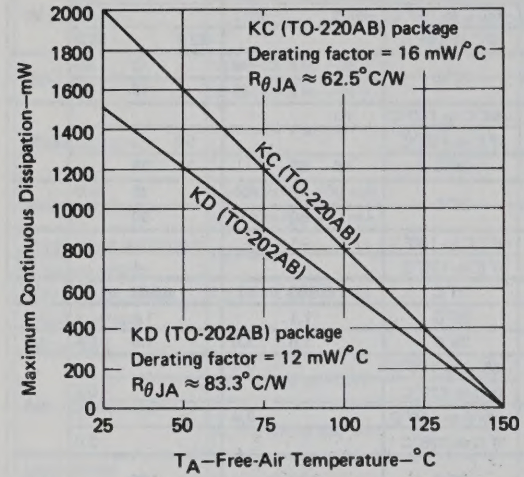

KC AND KD PACKAGES
FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVES

FIGURE 1

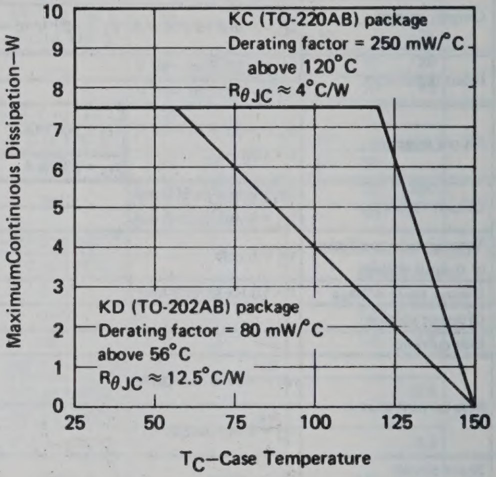

KC AND KD PACKAGES
CASE TEMPERATURE
DISSIPATION DERATING CURVES

FIGURE 2

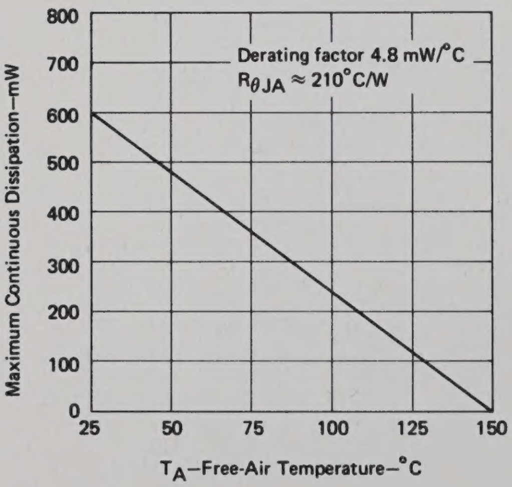

LA PACKAGE FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

FIGURE 3

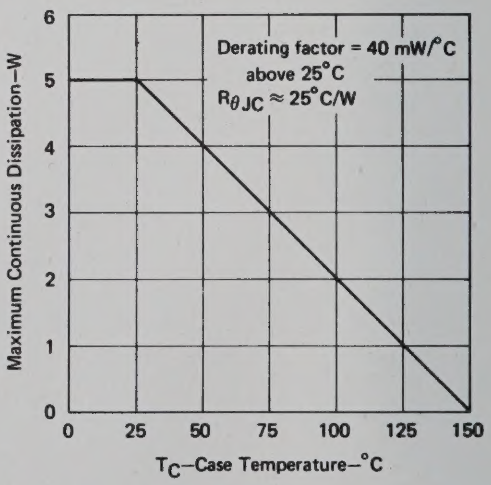

LA PACKAGE CASE TEMPERATURE
DISSIPATION DERATING CURVE

FIGURE 4

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

Special Functions

SPECIAL FUNCTIONS SELECTION GUIDE

Device	Description	Page
SE555	Precision Timer	295
TL182	Twin SPST BI-MOS Analog Switches	305
TL185	Twin DPST BI-MOS Analog Switch	308
TL188	Dual Complementary SPST BI-MOS Analog Switch	311
TL191	Twin Dual Complementary SPST BI-MOS Analog Switch	314
TL440	Zero Voltage Switch	317
TL441	Logarithmic Amplifier	323
TL500	Analog Processor	330
TL502	Digital Panel Meter Logic Device	331
TL560	Precision Level Detector	333
TL601	SPDT BI-MOS Analog Switch with Dual AND Inputs	339
TL604	Dual Complementary SPST BI-MOS Analog Switch	339
TL607	SPDT BI-MOS Analog Switch with Enable	339
TL610	SPDT BI-MOS Analog Switch with Triple AND Inputs	339
uA733	Differential Video Amplifier	345

7

TYPES SE555, NE555
PRECISION TIMERS

BULLETIN NO. DL-S 7612053, SEPTEMBER 1973—REVISED JUNE 1976

FORMERLY SN52555, SN72555

- Timing from Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL Compatible Output Can Sink or Source up to 200 mA
- Designed to be Interchangeable with Signetics SE555/NE555

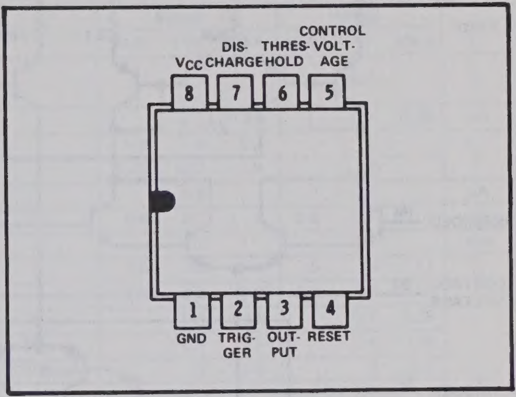
description

The SE555 and NE555 are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. When the threshold input rises above the threshold level, the flip-flop is reset and the output goes low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between the discharge terminal and ground.

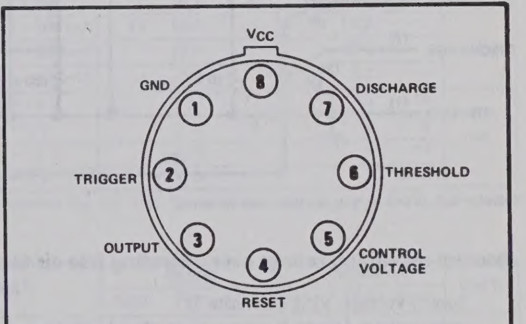
The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5-volt supply, output levels are compatible with TTL inputs.

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



CONTROL VOLTAGE
DISCHARGE
THRESHOLD
VCC
8
7
6
5
1
2
3
4
GND
TRIGGER
OUTPUT
RESET

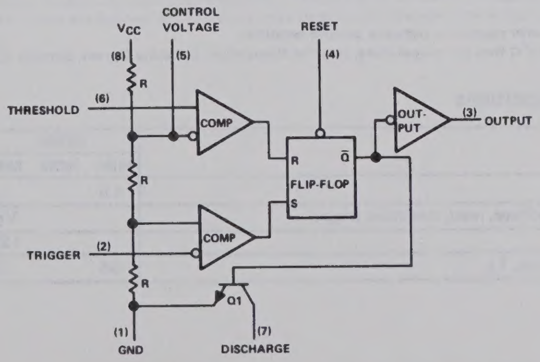
L PLUG-IN PACKAGE
(TOP VIEW)



VCC
8
GND
1
DISCHARGE
7
TRIGGER
2
THRESHOLD
6
OUTPUT
3
5
CONTROL VOLTAGE
4
RESET

PIN 1 IS IN ELECTRICAL CONTACT WITH THE CASE

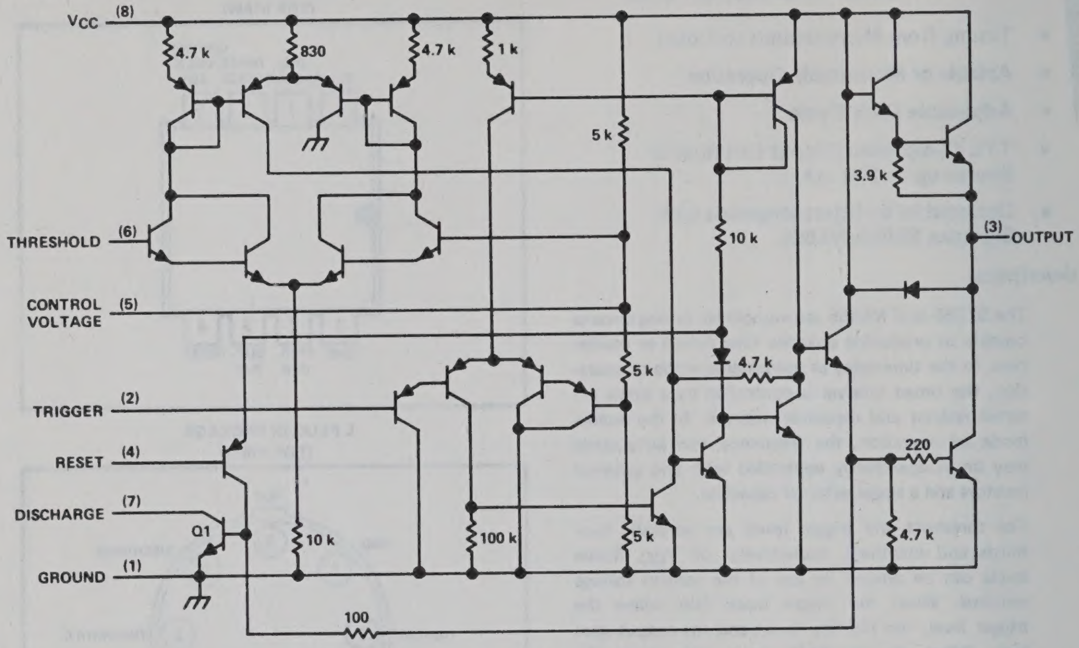
functional block diagram



VCC
(8)
CONTROL VOLTAGE
(5)
RESET
(4)
THRESHOLD
(6)
R
COMP
R
Q̄
FLIP-FLOP
S
OUTPUT
(3)
OUTPUT
R
COMP
TRIGGER
(2)
R
Q1
(1)
GND
(7)
DISCHARGE

TYPES SE555, NE555
PRECISION TIMERS

schematic


VCC (8)
4.7 k
830
4.7 k
1 k
5 k
3.9 k
THRESHOLD (6)
(3) OUTPUT
10 k
CONTROL VOLTAGE (5)
4.7 k
5 k
TRIGGER (2)
220
RESET (4)
DISCHARGE (7)
Q1
10 k
100 k
5 k
4.7 k
GROUND (1)
100

Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		18 V
Input voltage (control voltage, reset, threshold, trigger)		V_{CC}
Output current		±225 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)		600 mW
Operating free-air temperature range:	SE555	−55°C to 125°C
	NE555	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG or L package		300°C
Lead temperature 1/16 inch from case for 10 seconds: P package		260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

	SE555			NE555			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5		18	4.5		16	V
Input voltage, V_I (control voltage, reset, threshold, trigger)			V_{CC}			V_{CC}	V
Output Current, I_O			±200			±200	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555 MIN	SE555 TYP	SE555 MAX	NE555 MIN	NE555 TYP	NE555 MAX	UNIT
Threshold voltage level as a percentage of supply voltage				66.7			66.7		%
Threshold current (see Note 3)				0.1	0.25		0.1	0.25	µA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2		5		V
	V_{CC} = 5 V		1.45	1.67	1.9		1.67		
Trigger current				0.5			0.5		µA
Reset voltage level			0.4	0.7	1	0.4	0.7	1	V
Reset current				0.1			0.1		mA
Control voltage (open-circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA					0.25	0.35	
		I_{OL} = 8 mA		0.1	0.25				
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	11		9	14	
		V_{CC} = 5 V		2	4		2	5	

NOTE 3: This parameter influences the maximum value of the timing resistors R_A and R_B. For example when V_{CC} = 5 V the maximum value is $R = R_A + R_B \approx 20\ M\Omega$.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER	TEST CONDITIONS†		SE555 MIN	SE555 TYP	SE555 MAX	NE555 MIN	NE555 TYP	NE555 MAX	UNIT
Initial accuracy of timing interval	R_A = 1 kΩ to 100 kΩ, R_B = 0 to 100 kΩ, C = 0.1 µF	T_A = 25°C		0.5	2		1		%
Temperature coefficient of timing interval		T_A = MIN to MAX		30	100		50		ppm/°C
Supply voltage sensitivity of timing interval		T_A = 25°C		0.05	0.2		0.1		%/V
Output pulse rise time	C_L = 15 pF,	T_A = 25°C		100			100		ns
Output pulse fall time				100			100		ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

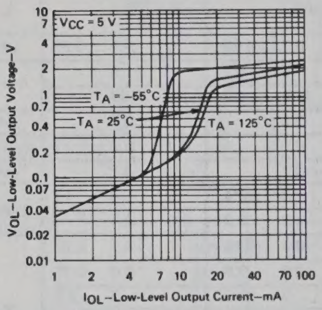


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

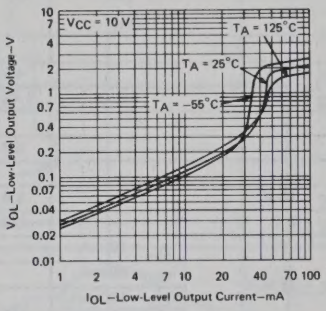


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

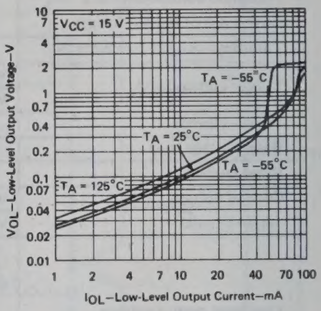


FIGURE 4

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

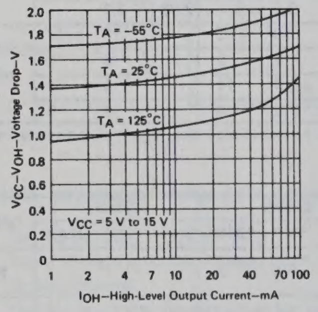


FIGURE 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

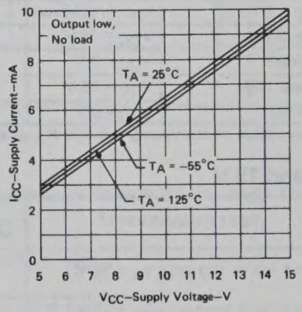


FIGURE 6

MINIMUM PULSE WIDTH REQUIRED
FOR TRIGGERING
vs
LOWEST VOLTAGE LEVEL OF
TRIGGER PULSE

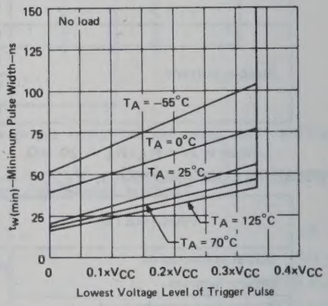


FIGURE 7

NORMALIZED OUTPUT PULSE WIDTH
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

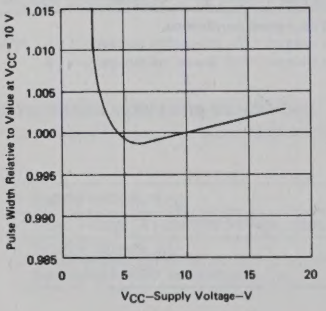


FIGURE 8

NORMALIZED OUTPUT PULSE WIDTH
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

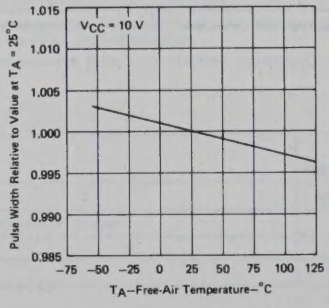


FIGURE 9

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

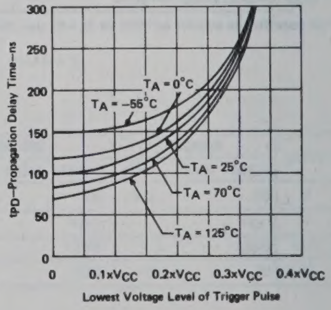


FIGURE 10

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†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL APPLICATION DATA

monostable operation

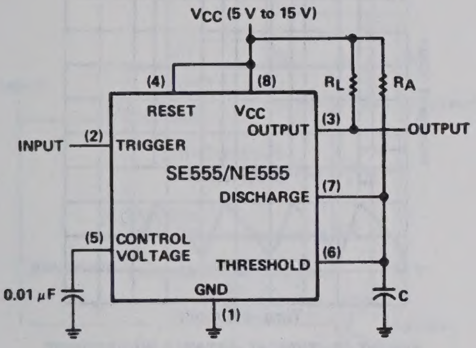


FIGURE 11—CIRCUIT FOR MONOSTABLE OPERATION

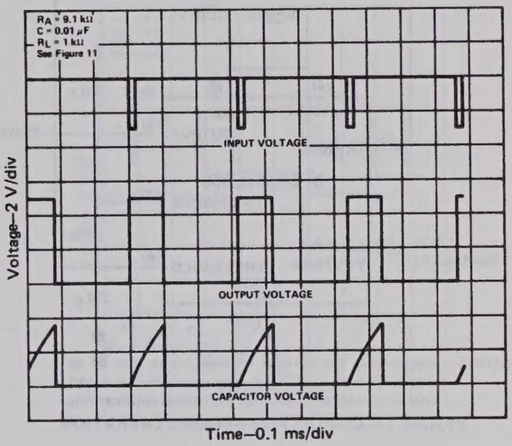


FIGURE 12—TYPICAL MONOSTABLE WAVEFORMS

The SE555 and NE555 may be connected as shown in Figure 11 for monostable operation producing an output pulse width independent of the input waveform and controlled by the $R_A \cdot C$ time constant. Prior to the negative-going input pulse, capacitor C is held discharged by transistor Q1 (see schematic). Application of a negative-going input-trigger-pulse sets the flip-flop, turns off Q1, and drives the output high. Capacitor C is now charged through R_A with a time constant $\tau = R_AC$. When the voltage across capacitor C reaches the threshold voltage of the comparator, the flip-flop is reset, energizing Q1 and discharging C; therefore driving the output back to the low level. Figure 12 shows the actual resultant waveforms.

Monostable operation is initiated when the negative-going input pulse reaches the trigger level. Once initiated, the timing interval will complete even if retriggering occurs during the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse width is approximately $t_w = 1.1\ R_AC$. Figure 13 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to the reset and trigger terminals during the timing interval will discharge C and re-initiate the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. When the reset input is not used, it should be connected to V_{CC} to prevent false triggering.

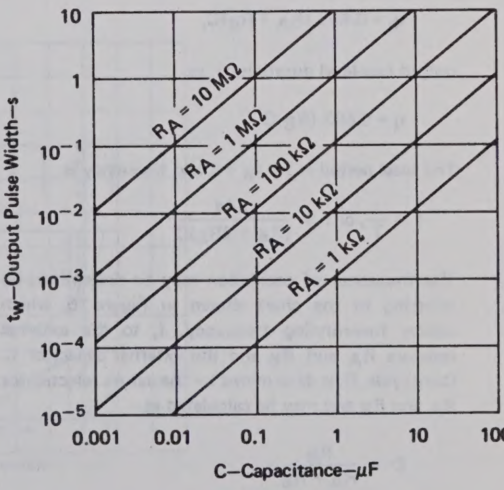
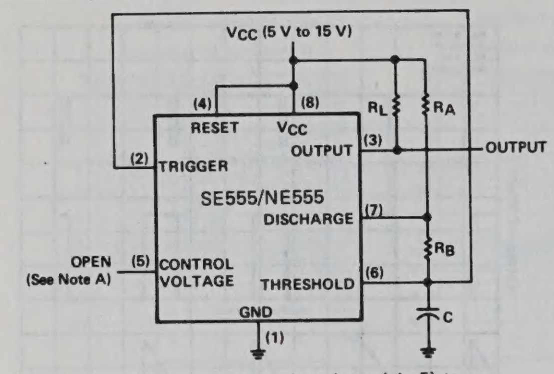


FIGURE 13—OUTPUT PULSE WIDTH vs CAPACITANCE

TYPICAL APPLICATION DATA

astable operation



NOTE A: Decoupling the control voltage input (pin 5) to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 14–CIRCUIT FOR ASTABLE OPERATION

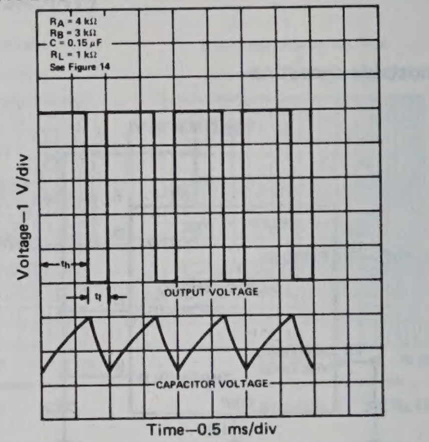


FIGURE 15–TYPICAL ASTABLE WAVEFORMS

Addition of a second resistor, R_B, to the circuit of Figure 11; as shown in Figure 14, and connection of the trigger input to the threshold input will cause the SE555/NE555 to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 15 shows typical waveforms generated during astable operation. The output high-level duration, t_h, is calculated as:

$$t_h = 0.693\,(R_A + R_B)C,$$

output low-level duration, t_l, as:

$$t_l = 0.693\,(R_B)C.$$

The total period is $T = t_h + t_l$ and frequency is

$$f = \frac{1}{T}, \text{ or } f = \frac{1.44}{(R_A + 2R_B)C}.$$

The frequency of oscillation may be determined by referring to the chart shown in Figure 16, which relates free-running frequency, f, to the external resistors R_A and R_B and the external capacitor C. Duty cycle, D, is determined by the values selected for R_A and R_B and may be calculated as:

$$D = \frac{R_B}{R_A + R_B}.$$

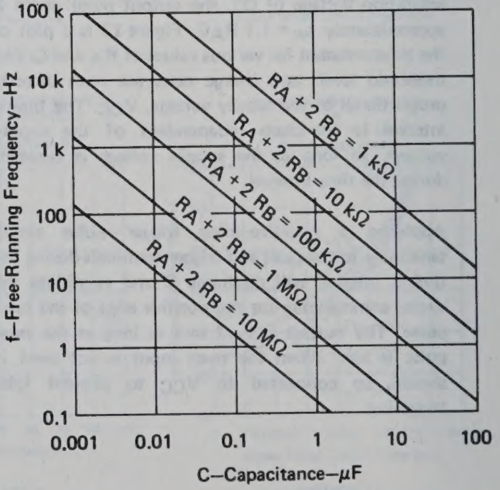


FIGURE 16–FREE-RUNNING FREQUENCY

TYPICAL APPLICATION DATA

missing-pulse detector

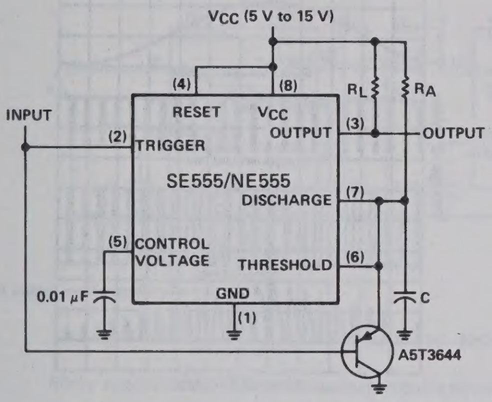

V_CC (5 V to 15 V)
(4)
(8)
RESET
V_CC
R_L
R_A
INPUT
(2)
TRIGGER
OUTPUT
(3)
OUTPUT
SE555/NE555
DISCHARGE
(7)
(5)
CONTROL
VOLTAGE
THRESHOLD
(6)
0.01 µF
GND
(1)
C
A5T3644

FIGURE 17—CIRCUIT FOR MISSING-PULSE DETECTOR

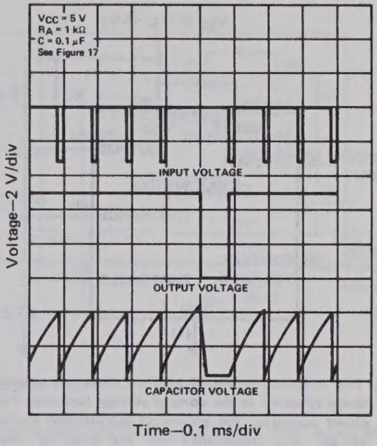


FIGURE 18—MISSING-PULSE-DETECTOR WAVEFORMS

The circuit shown in Figure 17 may be utilized to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train will permit the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 18.

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 11 can be made to operate as a frequency divider. Figure 19 illustrates a divide-by-3 circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

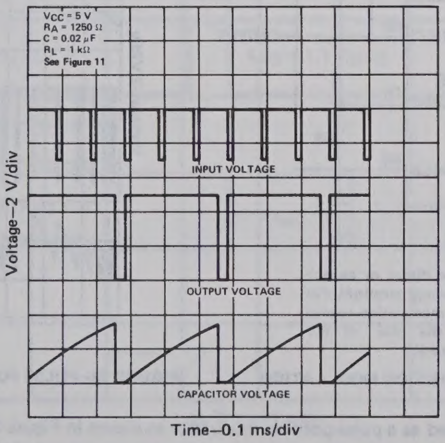
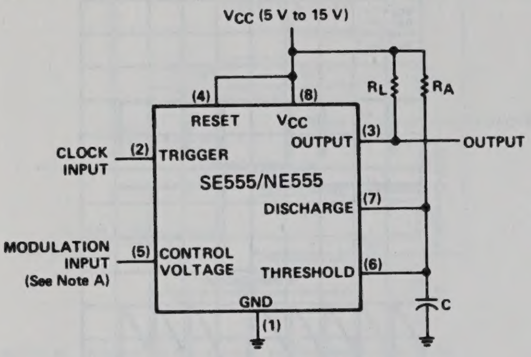


FIGURE 19—DIVIDE-BY-THREE CIRCUIT WAVEFORMS

7

TYPICAL APPLICATION DATA

pulse-width modulation


VCC (5 V to 15 V)
(4)
(8)
RL
RA
RESET
VCC
OUTPUT
(3)
OUTPUT
CLOCK INPUT
(2)
TRIGGER
SE555/NE555
DISCHARGE
(7)
MODULATION INPUT (See Note A)
(5)
CONTROL VOLTAGE
THRESHOLD
(6)
GND
(1)
C

NOTE A: The modulating signal may be direct or capacitively coupled to the control voltage terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the SE555/NE555 should be considered.

FIGURE 20–CIRCUIT FOR PULSE-WIDTH MODULATION

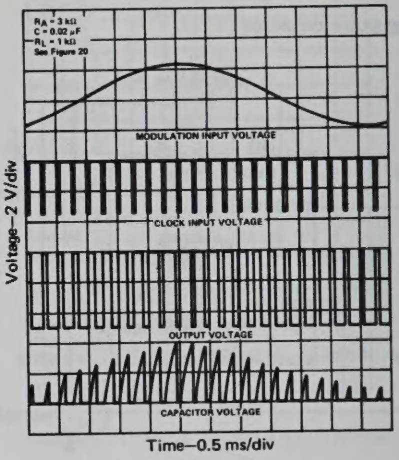
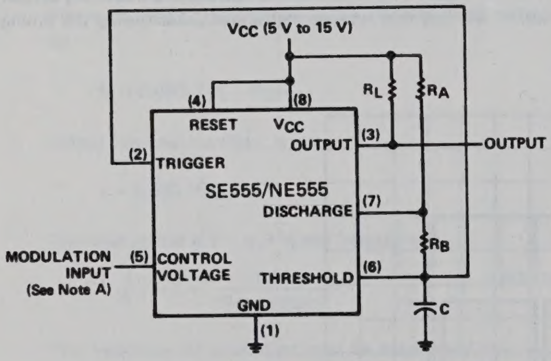


FIGURE 21–PULSE-WIDTH-MODULATION WAVEFORMS

The operation of the timer may be modified by modulating the internal threshold and trigger voltages. This is accomplished by applying an external voltage (or current) to the control voltage pin. Figure 20 is a circuit for pulse-width modulation. The monostable circuit is triggered by a continuous input pulse train and the threshold voltage is modulated by a control signal. The resultant effect is a modulation of the output pulse width, as shown in Figure 21. A sine-wave modulation signal is illustrated, but any wave-shape could be used.

pulse-position modulation


VCC (5 V to 15 V)
(4)
(8)
RL
RA
RESET
VCC
OUTPUT
(3)
OUTPUT
(2)
TRIGGER
SE555/NE555
DISCHARGE
(7)
RB
MODULATION INPUT (See Note A)
(5)
CONTROL VOLTAGE
THRESHOLD
(6)
GND
(1)
C

NOTE A: The modulating signal may be direct or capacitively coupled to the control voltage terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the SE555/NE555 should be considered.

FIGURE 22–CIRCUIT FOR PULSE-POSITION MODULATION

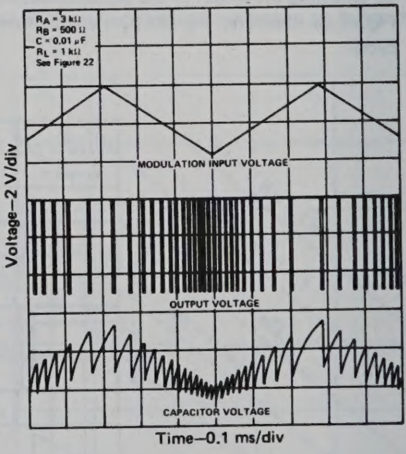
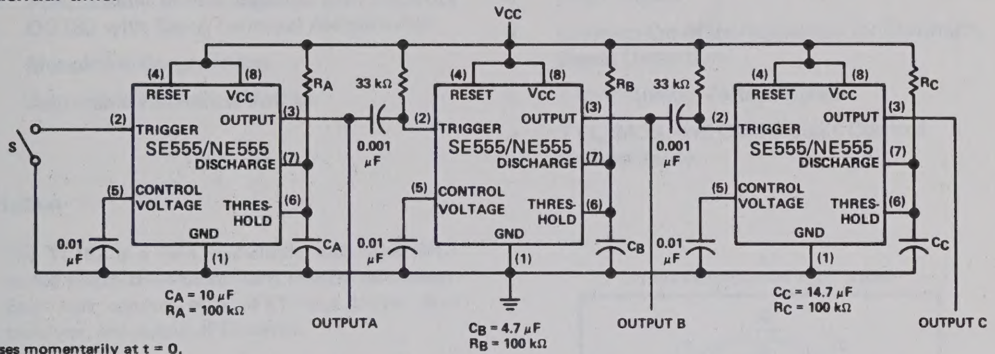


FIGURE 23–PULSE POSITION-MODULATION WAVEFORMS

The SE555/NE555 may be used as a pulse-position modulator as shown in Figure 22. In this application, the threshold voltage, and thereby the time delay, of a free-running oscillator is modulated. Figure 23 shows such a circuit, with a triangular-wave modulation signal, however, any modulating wave-shape could be used.

TYPICAL APPLICATION DATA

sequential timer


VCC
(4)
(8)
RESET
VCC
OUTPUT
(3)
(2)
TRIGGER
SE555/NE555
DISCHARGE
(7)
(5)
CONTROL
VOLTAGE
THRES-HOLD
(6)
GND
(1)
S
RA
33 kΩ
0.001 μF
0.01 μF
CA
CA = 10 μF
RA = 100 kΩ
OUTPUTA
RB
CB
CB = 4.7 μF
RB = 100 kΩ
OUTPUT B
RC
CC
CC = 14.7 μF
RC = 100 kΩ
OUTPUT C

S closes momentarily at t = 0.

FIGURE 24–SEQUENTIAL TIMER CIRCUIT

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications such as test equipment require activation of test signals in sequence. SE555/NE555 circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 24 illustrates a sequencer circuit with possible applications in many systems and Figure 25 shows the output waveforms.

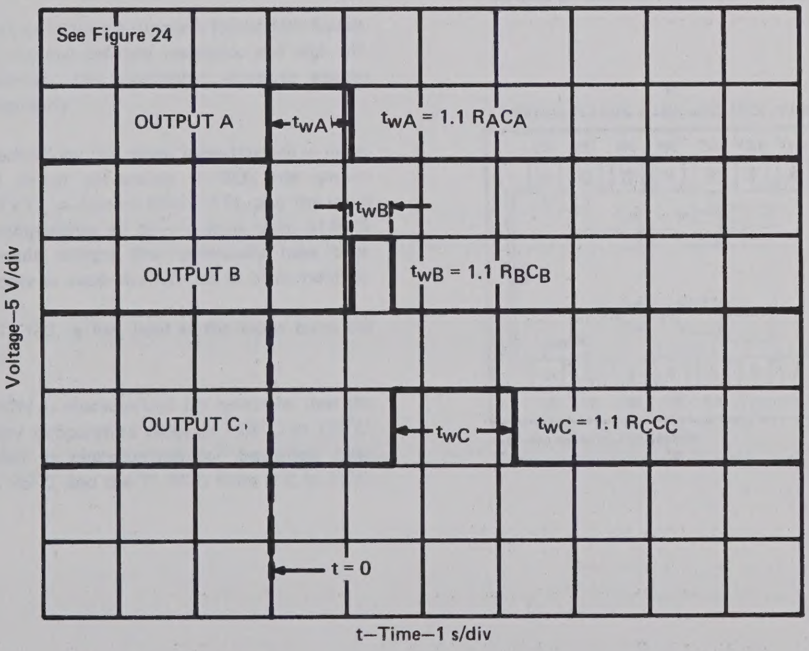


FIGURE 25–SEQUENTIAL TIMER WAVEFORMS

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TYPES TL182M, TL182I, TL182C
TWIN SPST BI-MOS ANALOG SWITCHES

BULLETIN NO. DL-S 7612416, JUNE 1976

- **Functionally Interchangeable with Signetics DG182 with Same Terminal Assignments**
- **Monolithic Construction**
- **Adjustable Reference Voltage**
- **JFET Inputs**
- **Uniform On-State Resistance for Minimum Signal Distortion**
- **±10-V Analog Voltage Range**
- **TTL, MOS, and CMOS Logic Control Compatibility**

description

The TL182 is a twin, monolithic, high-speed SPST analog switch constructed using BI-MOS technology. Each half consists of a JFET-input buffer, level translator, and output JFET switch.

The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOS, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

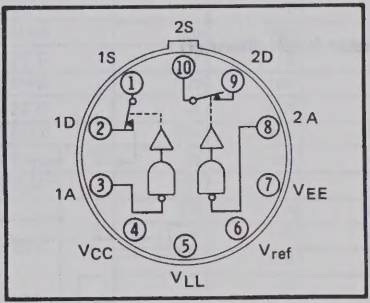
The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS has ion implanted JFETs, p-channel MOS-FETs, plus the usual bi-polar components all on the same chip. BI-MOS allows circuit designs that previously have been available only as expensive hybrids to be monolithic.

For the TL182, a low level at the input turns the switch on.

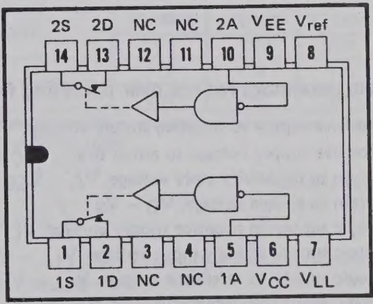
The TL182M is characterized for operation over the full military temperature range of −55°C to 125°C, the TL182I is characterized for operation from −25°C to 85°C, and the TL182C from 0°C to 70°C.

L
PLUG-IN PACKAGE (TOP VIEW)



All leads are electrically insulated from case.

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



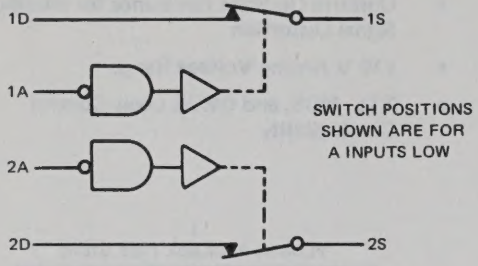
NC—No internal connection
Switch positions shown are A inputs low.

7

TENTATIVE DATA SHEET
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES TL182M, TL182I, TL182C
TWIN SPST BI-MOS ANALOG SWITCHES

functional diagram

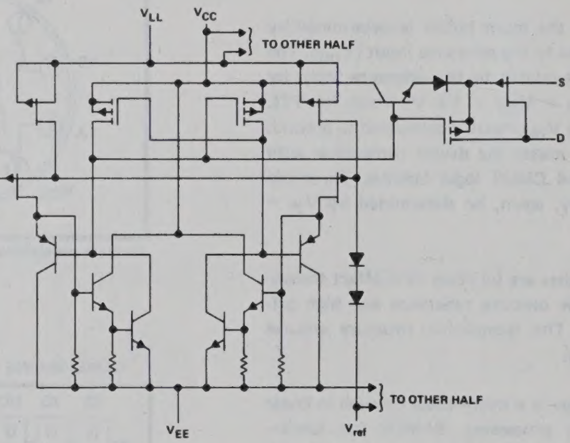


SWITCH POSITIONS SHOWN ARE FOR A INPUTS LOW

FUNCTION TABLE
(EACH HALF)

INPUT A	SWITCH S
L	ON (CLOSED)
H	OFF (OPEN)

schematic (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$	36 V
Positive supply voltage to either drain, $V_{CC} - V_D$	33 V
Drain to negative supply voltage, $V_D - V_{EE}$	33 V
Drain to source voltage, $V_D - V_S$	±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$	36 V
Logic supply to logic input voltage, $V_{LL} - V_I$	33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$	33 V
Logic input to reference voltage, $V_I - V_{ref}$	33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$	27 V
Reference to logic input voltage, $V_{ref} - V_I$	2 V
Current (any terminal)	30 mA
Continuous dissipation at (or below) 25°C free-air temperature: N package	1150 mW
L package (see Note 1)	625 mW
Operating free-air temperature range: TL182M	−55°C to 125°C
TL182I	−25°C to 85°C
TL182C	0°C to 70°C
Lead temperature 1/16 inch from case for 60 seconds: L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTE 1: For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2.

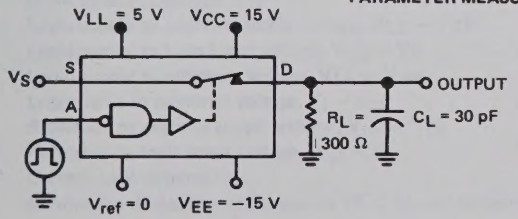
electrical characteristics, V_{CC} = 15 V, V_{EE} = –15 V, V_{LL} = 5 V, V_{ref} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TL182M		TL182I		TL182C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage			T_A = MIN to MAX	$V_{ref}+2$		$V_{ref}+2$		$V_{ref}+2$		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		$V_{ref}+0.8$		$V_{ref}+0.8$		$V_{ref}+0.8$	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		20	µA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0 V		T_A = MIN to MAX		–250		–250		–250	µA
$I_{D(off)}$	Off-state drain current	V_D = 10 V, V_S = –10 V, V_I = 2 V	V_{CC} = 15 V, V_{EE} = –15 V	T_A = 25°C		1		5		5	nA
				T_A = MAX		100		100		100	
			V_{CC} = 10 V, V_{EE} = –20 V	T_A = 25°C		1		5		5	
				T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = –10 V, V_S = 10 V, V_I = 2 V	V_{CC} = 15 V, V_{EE} = –15 V	T_A = 25°C		1		5		5	nA
				T_A = MAX		100		100		100	
			V_{CC} = 10 V, V_{EE} = –20 V	T_A = 25°C		1		5		5	
				T_A = MAX		100		100		100	
$I_{D(on)}+I_{S(on)}$	On-state channel leakage current	V_D = –10 V, V_S = –10 V, V_I = 0.8 V		T_A = 25°C		–2		–10		–10	nA
				T_A = MAX		–200		–200		–200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = –10 V, I_S = 1 mA, V_I = 0.8 V		T_A = MIN to 25°C		75		100		100	Ω
				T_A = MAX		100		150		150	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					–5		–5		–5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					–2		–2		–2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					–5		–5		–5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					–2		–2		–2	

switching characteristics, V_{CC} = 10 V, V_{EE} = –20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL182M	TL182I	TL182C	UNIT
			TYP	TYP	TYP	
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF, See Figure 1	175	175	175	ns
t_{off}	Turn-off time		350	350	350	

PARAMETER MEASUREMENT INFORMATION

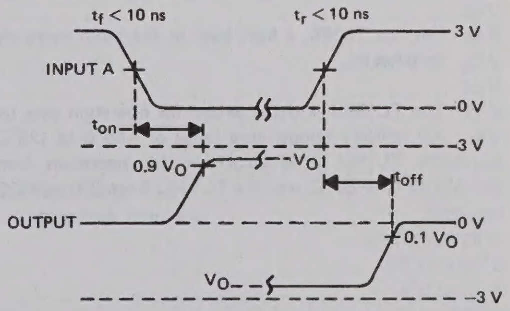


C_L includes probe and jig capacitance.

TEST CIRCUIT

V_S = 3 V for t_{on} and –3 V for t_{off}.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



VOLTAGE WAVEFORMS

V_o is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1

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TYPES TL185M, TL185I, TL185C
TWIN DPST BI-MOS ANALOG SWITCHES

BULLETIN NO. DL-S7612417, JUNE 1976

- **Functionally Interchangeable with Signetics DG185 with Same Terminal Assignments**
- **Monolithic Construction**
- **Adjustable Reference Voltage**
- **JFET Inputs**
- **Uniform On-State Resistance for Minimum Signal Distortion**
- **±10-V Analog Voltage Range**
- **TTL, MOS, and CMOS Logic Control Compatibility**

description

The TL185 is a twin, monolithic, high-speed DPST analog switch constructed using BI-MOS technology. Each half consists of a JFET-input buffer, level translator, and two output JFET switches.

The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOS, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

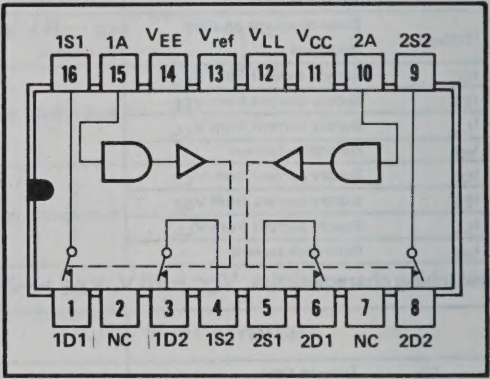
The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS has ion implanted JFETs, p-channel MOS-FETs, plus the usual bi-polar components all on the same chip. BI-MOS allows circuit designs that previously have been available only as expensive hybrids to be monolithic.

For the TL185, a high level at the input turns the switches on.

The TL185M is characterized for operation over the full military temperature range of −55°C to 125°C, the TL185I is characterized for operation from −25°C to 85°C, and the TL185C from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection
Switch positions shown are for A inputs high.

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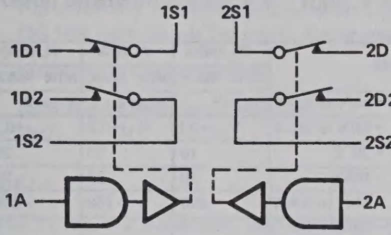
functional diagram

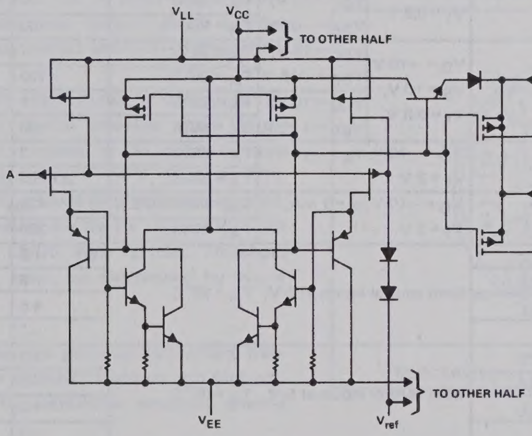


SWITCH POSITIONS SHOWN ARE FOR A INPUTS HIGH

FUNCTION TABLE (EACH HALF)

INPUT A	SWITCHES S1 AND S2
L	OFF (OPEN)
H	ON (CLOSED)

schematic (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$	36 V
Positive supply voltage to either drain, $V_{CC} - V_D$	33 V
Drain to negative supply voltage, $V_D - V_{EE}$	33 V
Drain to source voltage, $V_D - V_S$	±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$	36 V
Logic supply to logic input voltage, $V_{LL} - V_I$	33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$	33 V
Logic input to reference voltage, $V_I - V_{ref}$	33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$	27 V
Reference to logic input voltage, $V_{ref} - V_I$	2 V
Current (any terminal)	30 mA
Continuous dissipation at (or below) 25°C free-air temperature: N package	1150 mW
J package (see Note 1)	1025 mW
Operating free-air temperature range: TL185M	−55°C to 125°C
TL185I	−25°C to 85°C
TL185C	0°C to 70°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTE 1: For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2.

TYPES TL185M, TL185I, TL185C
TWIN DPST BI-MOS ANALOG SWITCHES

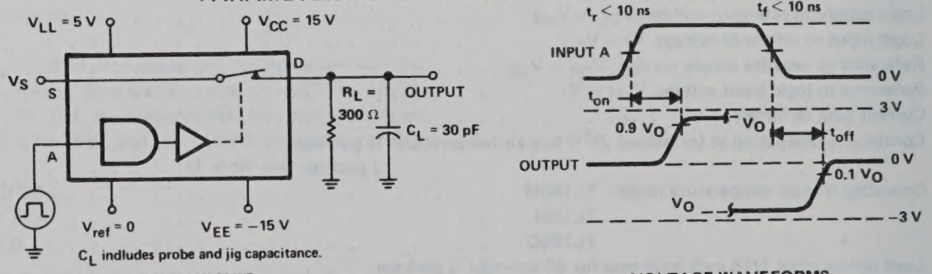
electrical characteristics, V_{CC} = 15 V, V_{EE} = −15 V, V_{LL} = 5 V, V_{ref} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TL185M		TL185I		TL185C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage			T_A = MIN to MAX	V_{ref}+2		V_{ref}+2		V_{ref}+2		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		V_{ref}+0.8		V_{ref}+0.8		V_{ref}+0.8	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		20	μA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0 V		T_A = MIN to MAX		−250		−250		−250	μA
$I_{D(off)}$	Off-state drain current	V_D = 10 V, V_S = −10 V, V_I = 0.8 V	V_{CC} = 15 V, V_{EE} = −15 V	T_A = 25°C		1		5		5	nA
				T_A = MAX		100		100		100	
			V_{CC} = 10 V, V_{EE} = −20 V	T_A = 25°C		1		5		5	
				T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = −10 V, V_S = 10 V, V_I = 0.8 V	V_{CC} = 15 V, V_{EE} = −15 V	T_A = 25°C		1		5		5	nA
				T_A = MAX		100		100		100	
			V_{CC} = 10 V, V_{EE} = −20 V	T_A = 25°C		1		5		5	
				T_A = MAX		100		100		100	
$I_{D(on)}+I_{S(on)}$	On-state channel leakage current	V_D = −10 V, V_S = −10 V, V_I = 2 V		T_A = 25°C		−2		−10		−10	nA
				T_A = MAX		−200		−200		−200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = −10 V, I_S = 1 mA, V_I = 2 V		T_A = MIN to 25°C		125		150		150	Ω
				T_A = MAX		250		300		300	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					−5		−5		−5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					−2		−2		−2	

switching characteristics, V_{CC} = 10 V, V_{EE} = −20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL185M	TL185I	TL185C	UNIT
				TYP	TYP	TYP	
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF,	See Figure 1	175	175	175	ns
t_{off}	Turn-off time			350	350	350	

PARAMETER MEASUREMENT INFORMATION



C_L indludes probe and jig capacitance.

TEST CIRCUIT

VOLTAGE WAVEFORMS

V_S = 3 V for t_{on} and −3 V for t_{off}. $V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$

V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1

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TYPES TL188M, TL188I, TL188C DUAL COMPLEMENTARY SPST BI-MOS ANALOG SWITCHES

BULLETIN NO. DL-S 7612418, JUNE 1976

- Functionally Interchangeable with Signetics DG188 with Same Terminal Assignments
- Monolithic Construction
- Adjustable Reference Voltage
- JFET Inputs
- Uniform On-State Resistance for Minimum Signal Distortion
- ±10-V Analog Voltage Range
- TTL, MOS, and CMOS Logic Control Compatibility

description

The TL188 is a monolithic, high-speed dual complimentary SPST switch constructed using BI-MOS technology. It consists of a JFET-input buffer, level translator, and two output JFET switches that can easily be connected in SPDT configuration.

The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with biploar, MOS, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

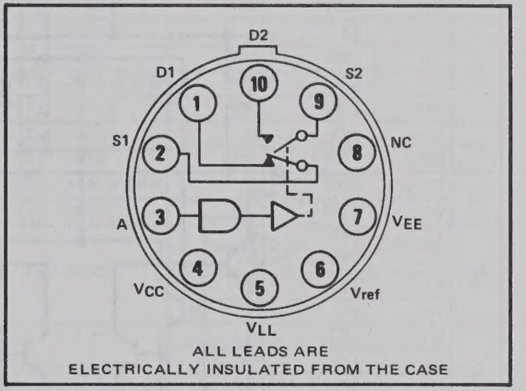
The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS has ion-implanted JFETs, p-channel MOS-FETs, plus the usual bi-polar components all on the same chip. BI-MOS allows circuit designs that have previously been available only as expensive hybrids to be monolithic.

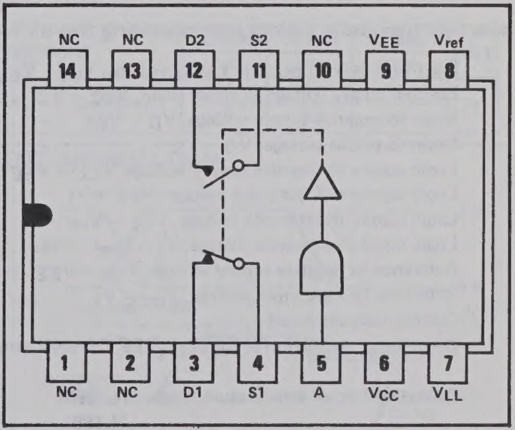
For the TL188, a high level at the input turns switch S1 on and S2 off.

The TL188M is characterized for operation over the full military temperature range of −55°C to 125°C, the TL188I is characterized for operation from −25°C to 85°C, and the TL188C from 0°C to 70°C.

L
PLUG-IN PACKAGE (TOP VIEW)



N
DUAL-IN-LINE PACKAGE (TOP VIEW)



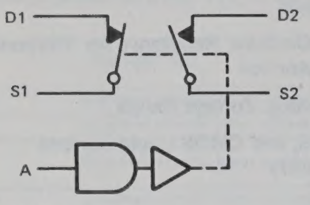
NC—No internal connection
Switch positions shown are for input A high.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TYPES TL188M, TL188I, TL188C
DUAL COMPLEMENTARY SPST BI-MOS ANALOG SWITCHES

functional diagram

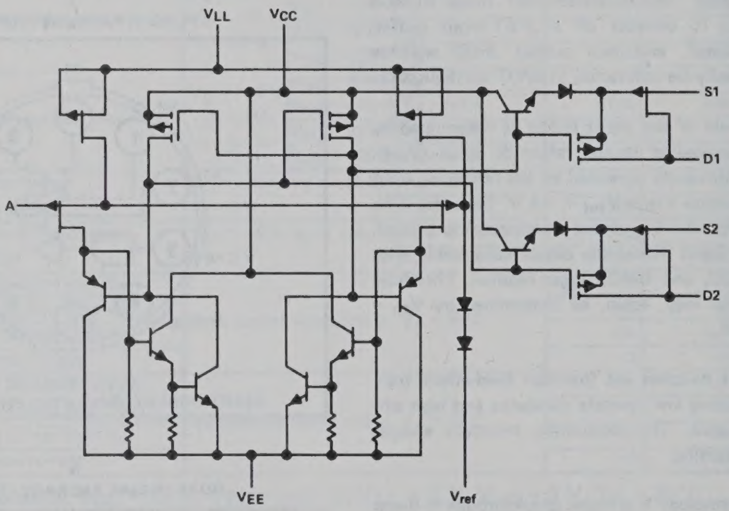


SWITCH POSITIONS
SHOWN ARE FOR
INPUT A HIGH

FUNCTION TABLE

INPUT	SWITCHES	
A	S1	S2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$	36 V
Positive supply voltage to either drain, $V_{CC} - V_D$	33 V
Drain to negative supply voltage, $V_D - V_{EE}$	33 V
Drain to source voltage, $V_D - V_S$	±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$	36 V
Logic supply to logic input voltage, $V_{LL} - V_I$	33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$	33 V
Logic input to reference voltage, $V_I - V_{ref}$	33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$	27 V
Reference to logic input voltage, $V_{ref} - V_I$	2 V
Current (any terminal)	30 mA
Continuous dissipation at (or below) 25°C free-air temperature: N package	1150 mW
L package (see Note 1)	625 mW
Operating free-air temperature range: TL188M	−55°C to 125°C
TL188I	−25°C to 85°C
TL188C	0°C to 70°C
Lead temperature 1/16 inch from case for 60 seconds: L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTE 1: For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2.

TYPES TL188M, TL188I, TL188C
DUAL COMPLEMENTARY SPST BI-MOS ANALOG SWITCHES

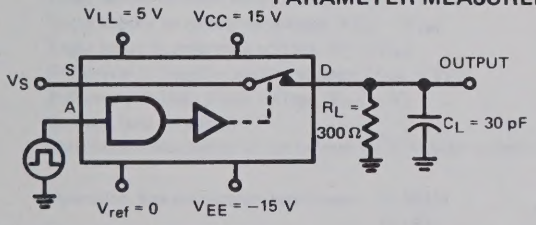
electrical characteristics, V_{CC} = 15 V, V_{EE} = –15 V, V_{LL} = 5 V, V_{ref} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TL188M		TL188I		TL188C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage			T_A = MIN to MAX	V_{ref}+2		V_{ref}+2		V_{ref}+2		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		V_{ref}–0.8		V_{ref}–0.8		V_{ref}–0.8	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		10	μA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0 V		T_A = MIN to MAX		–250		–250		–250	μA
$I_{D(off)}$	Off-state drain current	V_D = 10 V,	V_{CC} = 15 V,	T_A = 25°C		1		5		5	nA
		V_S = –10 V,	V_{EE} = –15 V	T_A = MAX		100		100		100	
		V_{IH} = 2 V,	V_{CC} = 10 V,	T_A = 25°C		1		5		5	
		V_{IL} = 0.8 V	V_{EE} = –20 V	T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = –10 V,	V_{CC} = 15 V,	T_A = 25°C		1		5		5	nA
		V_S = 10 V,	V_{EE} = –15 V	T_A = MAX		100		100		100	
		V_{IH} = 2 V,	V_{CC} = 10 V,	T_A = 25°C		1		5		5	
		V_{IL} = 0.8 V	V_{EE} = –20 V	T_A = MAX		100		100		100	
$I_{D(on)}+I_{S(on)}$	On-state channel leakage current	V_D = –10 V, V_S = –10 V,		T_A = 25°C		–2		–10		–10	nA
		V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = MAX		–200		–200		–200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = –10 V, I_S = 1 mA,		T_A = MIN to 25°C		75		100		100	Ω
		V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = MAX		150		150		150	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					–5		–5		–5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					–2		–2		–2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					–5		–5		–5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					–2		–2		–2	

switching characteristics, V_{CC} = 10 V, V_{EE} = –20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL188M	TL188I	TL188C	UNIT
			TYP	TYP	TYP	
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF, See Figure 1	175	175	175	ns
t_{off}	Turn-off time		350	350	350	

PARAMETER MEASUREMENT INFORMATION

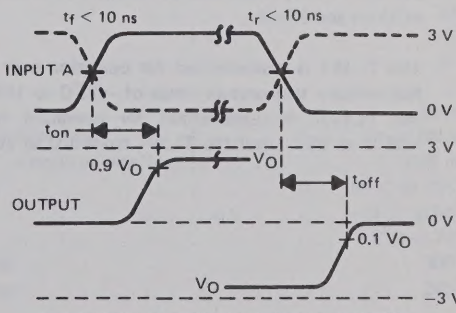


C_L includes probe and jig capacitance.

TEST CIRCUIT

V_S = 3 V for t_{on} and –3 V for t_{off}.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Input A: Solid for testing S1, dashed for testing S2.

VOLTAGE WAVEFORMS

V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1

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TYPES TL191M, TL191I, TL191C
TWIN DUAL COMPLEMENTARY SPST BI-MOS ANALOG SWITCHES

BULLETIN NO. DL-S 7612412, JUNE 1976

- **Functionally Interchangeable with Signetics DG191 with Same Terminal Assignments**
- **Monolithic Construction**
- **Adjustable Reference Voltage**
- **JFET Inputs**
- **Uniform On-State Resistance for Minimum Signal Distortion**
- **±10-V Analog Voltage Range**
- **TTL, MOS, and CMOS Logic Control Compatibility**

description

Each TL191 consists of two monolithic, high-speed dual complimentary SPST analog switches constructed using BI-MOS technology. Each half consists of a JFET-input buffer, level translator, and two output JFET switches that can easily be connected in SPDT configuration.

The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4$ V. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOS, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4$ V.

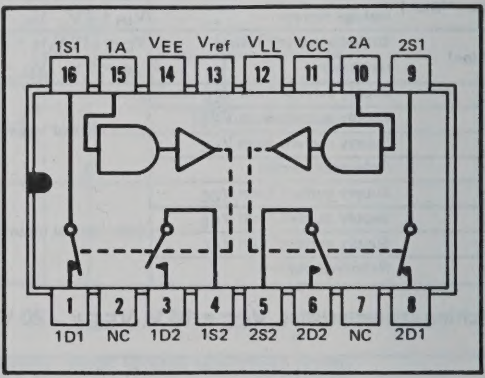
The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS has ion implanted JFETs, p-channel MOS-FETs, plus the usual bi-polar components all on the same chip. BI-MOS allows circuit designs that previously have been available only as expensive hybrids to be monolithic.

For the TL191, a high level at the input turns switches S1 on and S2 off.

The TL191 is characterized for operation over the full military temperature range of −55°C to 125°C, the TL191I is characterized for operation from −25°C to 85°C, and the TL191 from 0°C to 70°C.

J or N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection
Switch positions shown are for A inputs high.

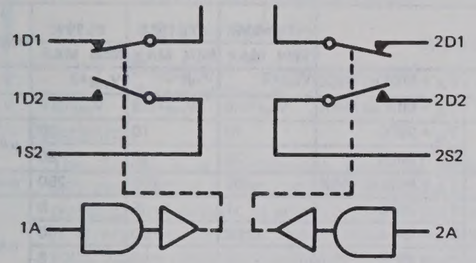
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TYPES TL191M, TL191I, TL191C
TWIN DUAL COMPLEMENTARY SPST BI-MOS ANALOG SWITCHES

functional diagram

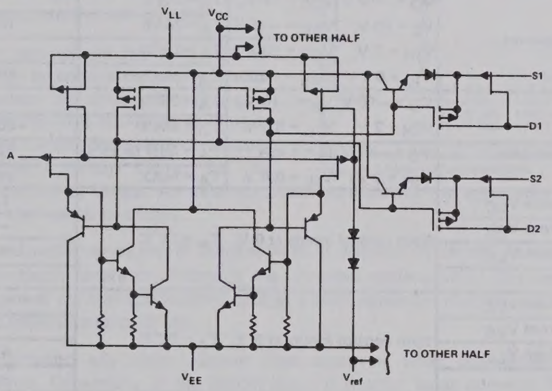


SWITCH POSITIONS
SHOWN ARE FOR
A INPUTS HIGH

FUNCTION TABLE
(EACH HALF)

INPUT A	SWITCHES S1	SWITCHES S2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$	36 V
Positive supply voltage to either drain, $V_{CC} - V_D$	33 V
Drain to negative supply voltage, $V_D - V_{EE}$	33 V
Drain to source voltage, $V_D - V_S$	±22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$	36 V
Logic supply to logic input voltage, $V_{LL} - V_I$	33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$	33 V
Logic input to reference voltage, $V_I - V_{ref}$	33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$	27 V
Reference to logic input voltage, $V_{ref} - V_I$	2 V
Current (any terminal)	30 mA
Continuous dissipation at (or below) 25°C free-air temperature: N package	1150 mW
J package (see Note 1)	1025 mW
Operating free-air temperature range: TL191M	−55°C to 125°C
TL191I	−25°C to 85°C
TL191C	0°C to 70°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTE 1: For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2.

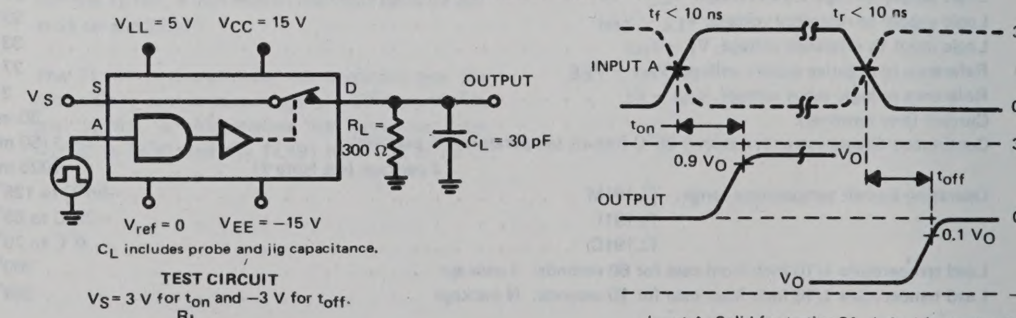
electrical characteristics, V_{CC} = 15 V, V_{EE} = –15 V, V_{LL} = 5 V, V_{ref} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TL191M		TL191I		TL191C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage			T_A = MIN to MAX	$V_{ref}+2$		$V_{ref}+2$		$V_{ref}+2$		V
V_{IL}	Low-level control input voltage			T_A = MIN to MAX		$V_{ref}+0.8$		$V_{ref}+0.8$		$V_{ref}+0.8$	V
I_{IH}	High-level control input current	V_I = 5 V		T_A = 25°C		10		10		20	µA
				T_A = MAX		20		20		20	
I_{IL}	Low-level control input current	V_I = 0 V		T_A = MIN to MAX		–250		–250		–250	µA
$I_{D(off)}$	Off-state drain current	V_D = 10 V, V_S = –10 V, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = 15 V, V_{EE} = –15 V	T_A = 25°C		1		5		5	nA
				T_A = MAX		100		100		100	
			V_{CC} = 10 V, V_{EE} = –20 V	T_A = 25°C		1		5		5	
				T_A = MAX		100		100		100	
$I_{S(off)}$	Off-state source current	V_D = –10 V, V_S = 10 V, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = 15 V, V_{EE} = –15 V	T_A = 25°C		1		5		5	nA
				T_A = MAX		100		100		100	
			V_{CC} = 10 V, V_{EE} = –20 V	T_A = 25°C		1		5		5	
				T_A = MAX		100		100		100	
$I_{D(on)}+I_{S(on)}$	On-state channel leakage current	V_D = –10 V, V_S = –10 V, V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = 25°C		–2		–10		–10	nA
				T_A = MAX		–200		–200		–200	
$r_{DS(on)}$	Drain-to-source on-state resistance	V_D = –10 V, I_S = 1 mA V_{IH} = 2 V, V_{IL} = 0.8 V		T_A = MIN to 25°C		125		150		150	Ω
				T_A = MAX		250		300		300	
I_{CC}	Supply current from V_{CC}	Both control inputs at 0 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					–5		–5		–5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					–2		–2		–2	
I_{CC}	Supply current from V_{CC}	Both control inputs at 5 V, T_A = 25°C				1.5		1.5		1.5	mA
I_{EE}	Supply current from V_{EE}					–5		–5		–5	
I_{LL}	Supply current from V_{LL}					4.5		4.5		4.5	
I_{ref}	Reference current					–2		–2		–2	

switching characteristics, V_{CC} = 10 V, V_{EE} = –20 V, V_{LL} = 5 V, V_{ref} = 0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL191M	TL191I	TL191C	UNIT
			TYP	TYP	TYP	
t_{on}	Turn-on time	R_L = 300 Ω, C_L = 30 pF, See Figure 1	175	175	175	ns
t_{off}	Turn-off time		350	350	350	

PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance.

TEST CIRCUIT

V_S = 3 V for t_{on} and –3 V for t_{off}.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Input A: Solid for testing S1, dashed for testing S2.

VOLTAGE WAVEFORMS

V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1

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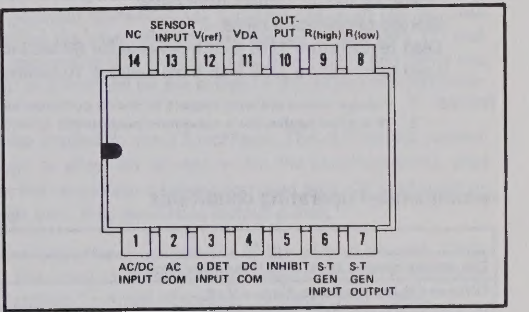
TYPE TL440C
ZERO-VOLTAGE SWITCH

BULLETIN NO. DL-S 7611595, MAY 1972—REVISED JUNE 1976

FORMERLY SN72440

- Differential Amplifier Inputs
- A-C Line Operation
- Capable of Triggering Several Types of Triacs
- Internal Active Elements of Saw-Tooth Generator for Proportional Control
- Wide Variety of Possible Connections of Input Section and of Output Section

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)


NC
SENSOR INPUT
V(ref)
VDA
OUT-PUT
R(high)
R(low)
14
13
12
11
10
9
8
1
2
3
4
5
6
7
AC/DC INPUT
AC COM
0 DET INPUT
DC COM
INHIBIT
S-T GEN INPUT
S-T GEN OUTPUT

NC—No internal connection.

description

The TL440 is a combination threshold detector and zero-crossing trigger, intended primarily for a-c power-control circuits. It allows a triac or SCR to be fired when the a-c input signal crosses through zero volts, thereby minimizing undesirable electromagnetic interference. In this manner, the load utilizes full cycles of line voltage as opposed to partial cycles typical with SCR phase-control power circuits.

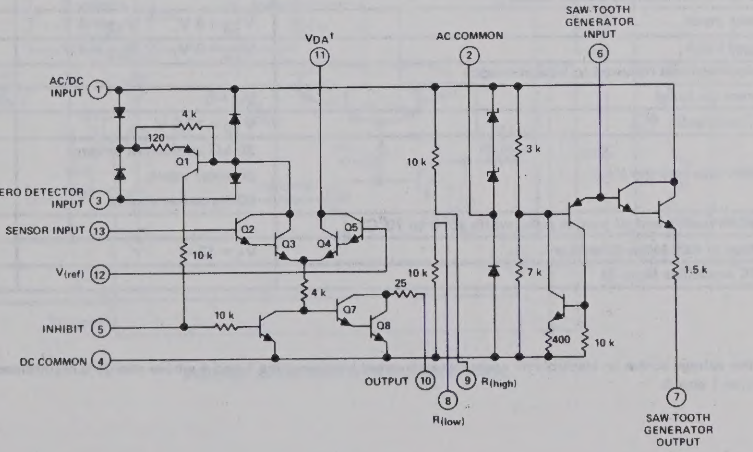
The circuit includes a zero-voltage detector, a differential amplifier that may be used in conjuction with a resistance bridge to sense the parameter being controlled, the active elements of a saw-tooth generator, and an output section. Also included are resistors which may be used as a voltage divider for the reference side of the resistance bridge. An external sensor suitable for the application and an external potentiometer form the input side of the resistance bridge.

The TL440 can be used either as an on-off control with or without hysteresis, or as a proportional control with the use of the internal saw-tooth generator. Although the principal application of this device is in temperature control, it can be used for many power control applications such as a photosensistive control, voltage level sensor, a-c lamp flasher, small relay driver, or a miniature lamp driver.

The inhibit function prevents any output pulses from occurring when the applied voltage at the inhibit input is typically 1 volt or greater. Conversely, if the inhibit input is shorted to dc common, an output pulse will be obtained for each zero-crossing of the a-c power input waveform regardless of the sensor input conditions.

The TL440C is characterized for operation from 0°C to 70°C.

schematic


AC/DC INPUT 1
ZERO DETECTOR INPUT 3
SENSOR INPUT 13
V(ref) 12
INHIBIT 5
DC COMMON 4
VDA† 11
AC COMMON 2
SAW TOOTH GENERATOR INPUT 6
OUTPUT 10
R(low) 8
R(high) 9
SAW TOOTH GENERATOR OUTPUT 7
4 k
120
Q1
Q2
Q3
Q4
Q5
Q7
Q8
10 k
4 k
10 k
10 k
25
10 k
3 k
7 k
400
10 k
1.5 k

Resistor values shown are nominal and in ohms.

†Pin 11 is usually connected to the AC/DC input, pin 1, unless a control circuit requiring hysteresis is desired. See Figure 4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage applied to AC/DC input (See Note 1)	15 V
Peak current into AC/DC input	40 mA
Peak current into zero-detector input	30 mA
Peak output sink current (See Note 2)	250 mA
Continuous total power dissipation at (or below) 70°C free-air temperature range	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the dc common terminal unless otherwise specified.
2. This value applies for a maximum pulse width of 400 μs and for a maximum duty cycle of 2%.

recommended operating conditions

	MIN	NOM	MAX	UNIT
D-c voltage applied to AC/DC input (See Note 3)		12		V
Differential input voltage, $V_{13} - V_{12}$			±2	V
Voltage at sensor or $V_{(ref)}$ input, V_{13} or V_{12}		6		V
Peak output current (See Note 4)			200	mA
Output pulse width	100		400	μs
Operating free-air temperature, T_A	0		70	°C

NOTES: 3. This is the recommended d-c supply voltage when the voltage across pins 1 and 4 is not being maintained by charging an electrolytic capacitor from the line voltage. See typical application data.
4. This value applies for $t_w \leq 400$ μs, duty cycle ≤ 2%.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sensor input voltage hysterysis	Pin 11 connected to Pin 1		30		mV
Voltage required at inhibit input to inhibit output			1	3	V
Current into sensor input	$V_{13} = 6$ V, $V_{12} = 4$ V			5	μA
Current into $V_{(ref)}$ input	$V_{12} = 6$ V, $V_{13} = 4$ V			5	μA
Current into inhibit terminal required to inhibit output			20		μA
Peak output current (pulsing)	$V_5 = 0$	75	100		mA
Output current (inhibited)	$V_{10} = 13.5$ V			1	μA
Output pulse width into resistive load	25 kΩ connected to zero-detector input, 60-Hz power source		150		μs
Average temperature coefficient of output pulse width (0°C to 70°C)			0.7		μs/°C
Peak output voltage of saw-tooth generator	$V_1 = 12$ V		9		V
Voltage at AC/DC input(See Note 5)		9	11.5		V

NOTE 5: This is the voltage across an electrolytic capacitor connected between pins 1 and 4 whose charge is maintained by the a-c line voltage. See Figures 1 and 3.

TYPICAL APPLICATION DATA

The circuit shown in Figure 1 provides on-off temperature control. Electrolytic capacitor C1 maintains the d-c operating voltage. Since the series combination of D5 and D6 is in parallel with the series combination of C1 and D7, the voltage developed across C1 is limited to approximately 12 V. Because the energy to fire the triac comes from C1, the voltage across pins 1 and 4 will fluctuate as the triac fires. If a more stable operation of the circuit is desired, a 12-volt d-c supply should be connected between pins 1 and 4 in lieu of C1. The temperature sensor must have a negative coefficient in this circuit.

During most of the a-c cycle, Q1 is turned on by the current flow through either D1, Q1, D4 or D2, Q1, D3, depending on the polarity of the a-c voltage between pins 1 and 3. The collector current of Q1 turns on Q6. With Q6 on, base drive to Q7 and Q8 is inhibited, resulting in no output pulse to fire the triac. When the a-c voltage crosses zero, Q1 and Q6 are turned off. This enables Q7 and Q8 to turn on, thereby connecting d-c common to the triac trigger and firing the triac. This one output pulse per zero crossing is either inhibited or permitted by the action of the differential amplifier and resistance bridge circuit.

As the controlled temperature begins to rise, the positive voltage applied to pin 13 increases. The differential control amplifier acts to lower the potential of the base of Q1 enough to allow Q1 to stay on for the complete cycle, thus inhibiting the output pulses as explained above. Similarly when the temperature being controlled falls, Q1 is allowed to turn off during the intervals where the line voltage passes through zero, thus generating output pulses.

The width of the output pulse at pin 10 can be varied to suit the triggering characteristics of the triac to be used. Table I shows the output pulse lengths obtained as R20 is changed. For small load currents (less than 4-5 amps) a triac with high gate sensitivity may be required due to the high value of "latch-up" current of medium to high power triacs.

TABLE I

R20	OUTPUT PULSE WIDTH
15 kΩ	100 μs
22 kΩ	150 μs
42 kΩ	300 μs

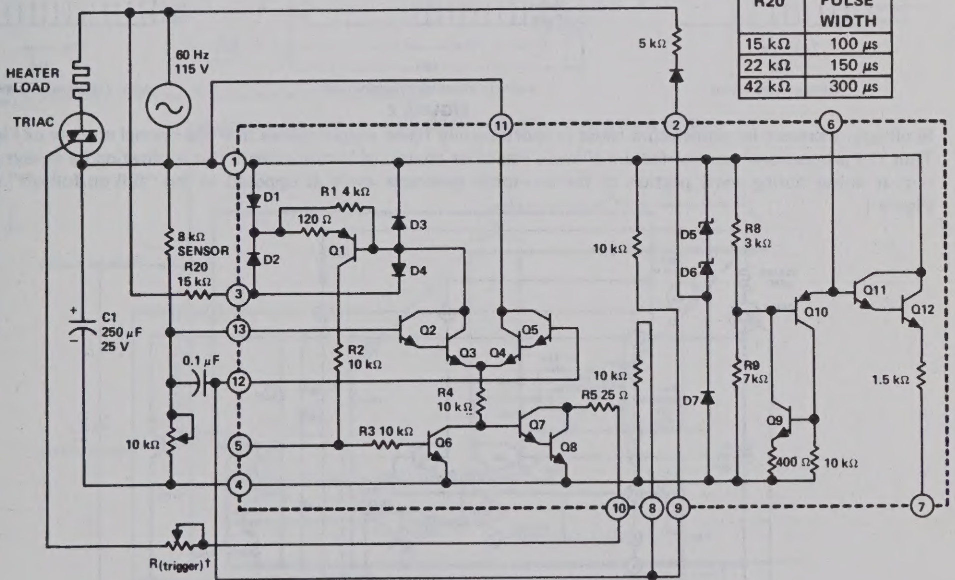


FIGURE 1—ON-OFF HEATER CONTROL

---

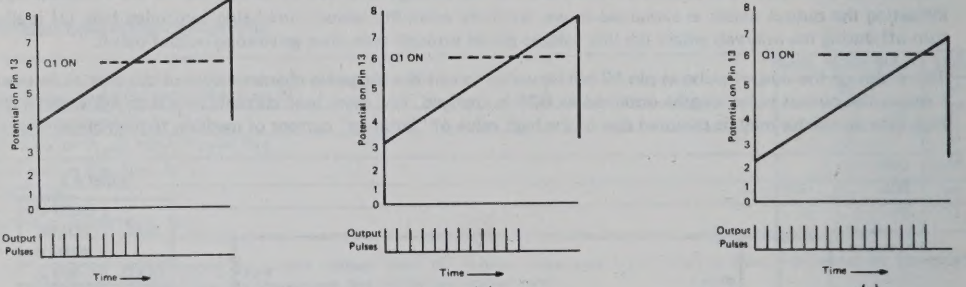
† R(trigger) is adjusted so that the peak output is less than 200 mA.

TYPICAL APPLICATION DATA

The circuit shown in Figure 3 provides proportional control of a heating system. With the exception of the saw-tooth generator, the circuit of Figure 3 functions the same as that of Figure 1. The sensor of Figure 3 has a negative temperature coefficient.

Transistors Q9 and Q10 are connected to function as an SCR in order to discharge external capacitor C2 very quickly. The time constant of the saw-tooth generator can be varied by changing either the external capacitor or the external resistor. However it is suggested that the capacitor be varied and not the resistor since too low a value of resistance would allow Q9 and Q10 to stay on continuously. The period of the saw-tooth generator is usually 10 to 100 times the period of the line voltage.

At the start of the saw-tooth waveform the base of Q1 is high and output pulses occur at pin 10. At the desired temperature a certain number of output pulses occur during each saw-tooth cycle as shown in Figure 2(a). At a slightly decreased temperature the resistance of the sensor increases, lowering the d-c potential of pin 13. This lowers the potential of the entire saw-tooth waveform as shown in Figure 2(b) which causes a few more output pulses to occur. At greatly decreased temperatures many more pulses occur each saw-tooth cycle as shown in Figure 2(c).



(a)
DESIRED TEMPERATURE

(b)
SLIGHTLY DECREASED TEMPERATURE

(c)
GREATLY DECREASED TEMPERATURE

FIGURE 2

Similiarly, increases in temperature cause proportionately fewer output pulses than the normal number of Figure 2(a). Thus the proportional control feature allows a smoother control of temperature in this application by always providing output pulses during some portion of the saw-tooth generator cycle as opposed to the "full on/full off" circuit of Figure 1.

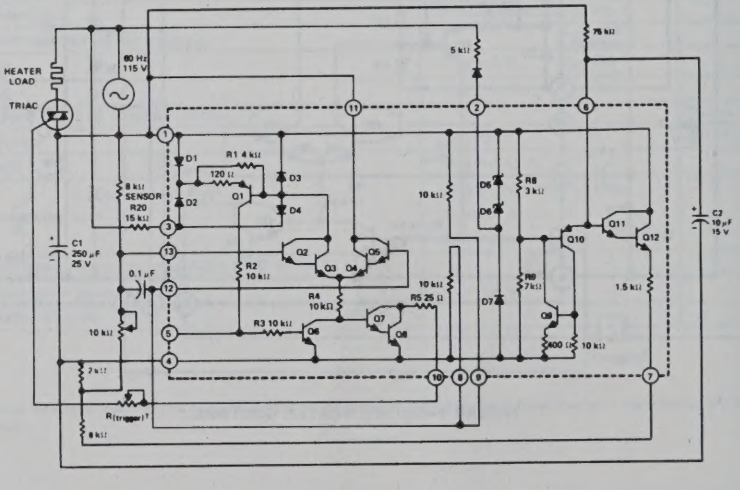

75 kΩ
5 kΩ
60 Hz
115 V
HEATER LOAD
TRIAC
11
2
6
1
D1
R1 4 kΩ
120 Ω
D3
8 kΩ
SENSOR
R20
15 kΩ
Q1
D2
D4
3
13
C1
250 µF
25 V
Q2
Q3
Q4
Q5
R2
10 kΩ
0.1 µF
12
10 kΩ
R4
10 kΩ
R3 10 kΩ
Q6
Q7
Q8
5
4
10 kΩ
R5 25 Ω
10 kΩ
D5
D6
R8
3 kΩ
R9
7 kΩ
D7
Q9
400 Ω
10 kΩ
Q10
Q11
Q12
1.5 kΩ
C2
10 µF
15 V
2 kΩ
R(trigger)†
8 kΩ
10
8
9
7

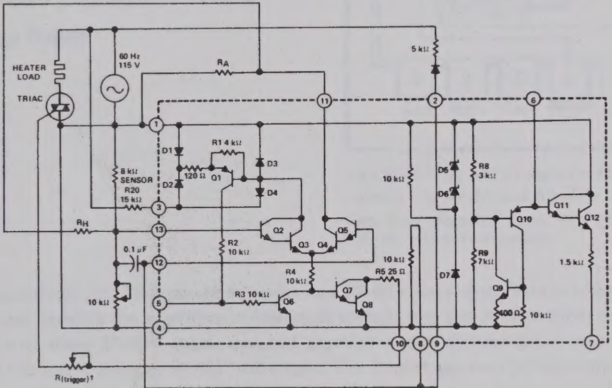
FIGURE 3—PROPORTIONAL HEATER CONTROL

†$R_{(trigger)}$ is adjusted so that the peak output is less than 200 mA.

TYPE TL440C
ZERO-VOLTAGE SWITCH

TYPICAL APPLICATION DATA

Hysteresis may be added to the TL440 by externally making the differential amplifier appear in Schmitt-trigger configuration. This is done by applying positive feedback from pin 11 to pin 13 through hysteresis resistors R_A and R_H. When the output is enabled, the voltage drop developed across resistor R_A is fed through R_H to the sensor input of the differential amplifier. This lowers the voltage at this point from the voltage level present when the output is inhibited. The resistance of the sensor must now decrease enough to overcome this additional ("hysteresis") voltage in order to inhibit the output. R_H should have a typical value close to the value of the sensor used. The value of R_A, which determines the amount of hysteresis, should be approximately one tenth the value of R_H. In Figure 4 the 10 kΩ potentiometer is adjusted to set the voltage at pin 13 to the level at which the output is enabled. When precise control is not needed, such a circuit eliminates the small "uncertainity range" observed in time-proportioning systems.


HEATER LOAD
TRIAC
60 Hz 115 V
RA
5 kΩ
8 kΩ SENSOR
R20 15 kΩ
RH
0.1 μF
10 kΩ
R(trigger)†
D1
D2
D3
D4
R1 4 kΩ
120 Ω
Q1
Q2
Q3
Q4
Q5
R2 10 kΩ
R4 10 kΩ
R3 10 kΩ
Q6
Q7
Q8
R5 25 Ω
10 kΩ
10 kΩ
D6
D6
D7
R8 3 kΩ
R9 7 kΩ
Q9
400 Ω
10 kΩ
Q10
Q11
Q12
1.5 kΩ
1
2
3
4
5
6
7
8
9
10
11
12
13

† $R_{(trigger)}$ is adjusted so that the peak output is less than 200 mA.

FIGURE 4—ON-OFF HEATER CONTROL WITH HYSTERSIS ADDED

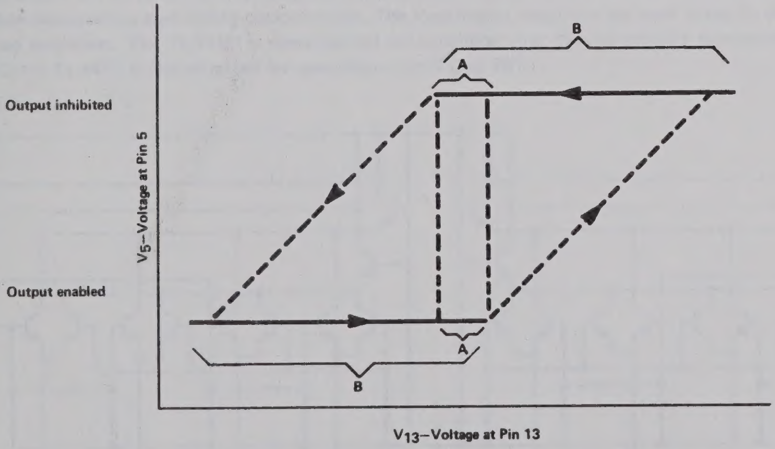


FIGURE 5—HYSTERESIS CURVE FOR FIGURE 4

A—Circuit without added hysteresis ($\Delta V_{13} \approx$ 15 to 20 mV residual hysteresis)
B—Circuit with added hysteresis ($\Delta V_{13} \approx$ 200 to 300 mV added hysteresis)
NOTE 1: Dotted lines represent discontinuous changes where the differential amplifier changes from inhibit to enable or vice-versa. Solid lines represent stable states (inhibit or enable) of the differential amplifier.

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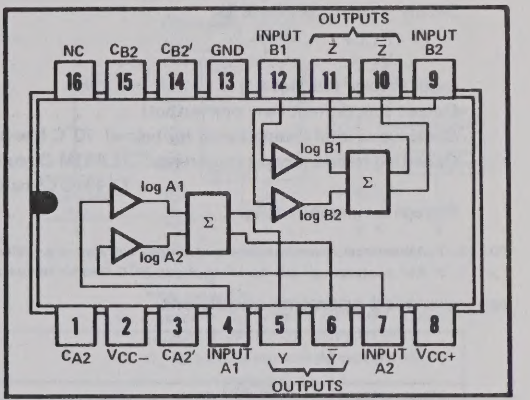
TYPES TL441M, TL441C
LOGARITHMIC AMPLIFIERS

BULLETIN NO. DL-S 7611427, JANUARY 1971–REVISED JUNE 1976

FORMERLY SN56502, SN76502

- Excellent Dynamic Range
- Wide Bandwidth
- Built-In Temperature Compensation
- Log Linearity (30 dBV Sections) . . . 1 dBV
- Wide Input Voltage Range

J OR N
DUAL-IN-LINE PACKAGES (TOP VIEW)


OUTPUTS
NC
CB2
CB2'
GND
INPUT B1
Z
Z̄
INPUT B2
16
15
14
13
12
11
10
9
log B1
Σ
log A1
log B2
Σ
log A2
1
2
3
4
5
6
7
8
CA2
VCC–
CA2'
INPUT A1
Y
Ȳ
INPUT A2
VCC+
OUTPUTS

$Y \propto \log A1 + \log A2$; $Z \propto \log B1 + B2$

where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.

C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$, are detector compensation inputs.

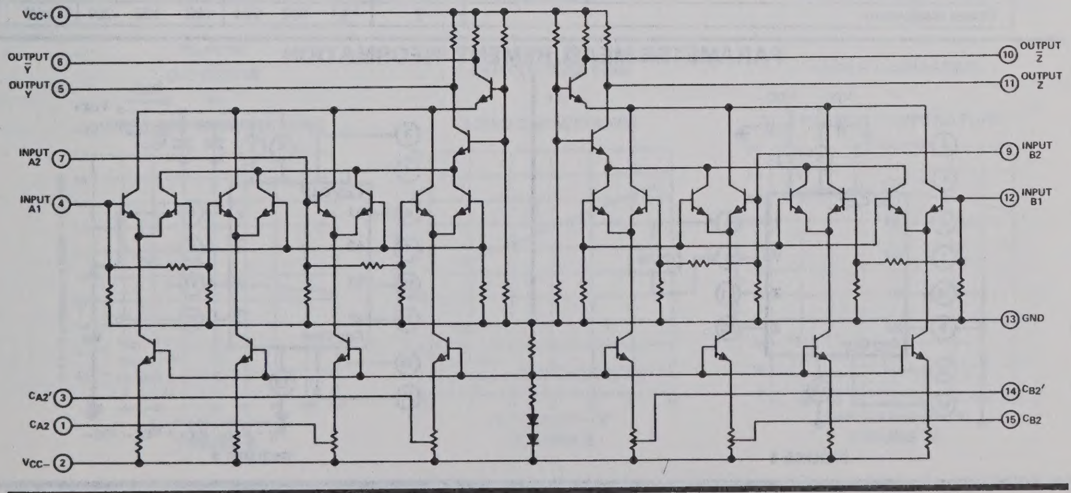
NC–No internal connection

description

This monolithic logarithmic amplifier circuit contains four 30-dBV log stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dBV input voltage range. Each half of the circuit contains two of these 30-dBV stages summed together in one differential output which is proportional to the sum of the logs of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dBV. In practice, this permits the input voltage range to be typically greater than 80 dBV with log linearity of ±0.5 dBV (see application data). Bandwidth is from dc to 40 megahertz.

These circuits are useful in military weapons systems, broadband radar, and infrared reconnaissance systems. They serve for data compression and analog compensation. The logarithmic amplifiers are used in log IF circuitry as well as video and log amplifiers. The TL441M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL441C is characterized for operation from 0°C to 70°C.

schematic


VCC+ 8
OUTPUT Ȳ 6
OUTPUT Y 5
INPUT A2 7
INPUT A1 4
CA2' 3
CA2 1
VCC– 2
10 OUTPUT Z̄
11 OUTPUT Z
9 INPUT B2
12 INPUT B1
13 GND
14 CB2'
15 CB2

TYPES TL441M, TL441C
LOGARITHMIC AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1):
V_{CC+} 8V
V_{CC-} . . . . −8V
Input voltage (see Note 1) 6V
Output sink current (any one output) . . . . 30 mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 2) . . . . 500 mW
Operating free-air temperature range: TL441M Circuits . . . . −55°C to 125°C
TL441C Circuits . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTES: 1. All voltages, except differential output voltages, are with respect to network ground terminal.
2. For operation of the TL441M above 70°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

	TL441M			TL441C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Input voltage for each 30-dBV stage	0.01		1	0.01		1	V_{p-p}
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics, $V_{CC+} = 6\text{ V}$, $V_{CC-} = -6\text{ V}$, $T_A = 25°C$

PARAMETER	TEST FIGURE	TL441M			TL441C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential output offset voltage	1		±25	±60		±40		mV
Quiescent output voltage	2	5.45	5.6	5.85	5.45	5.6	5.85	V
D-c scale factor (differential output), each 30-dBV stage, −35 dBV to −5 dBV	3	7	8	10	6	8	12	mV/dBV
A-c scale factor (differential output)			8			8		mV/dBV
D-c error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2		1		dBV
Input impedance			500			500		Ω
Output impedance			200			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	30		20	30	ns
Supply current from V_{CC+}	2	14.5	18.5	23	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−10.5	−6	−8.5	−10.5	mA
Power dissipation	2	123	162	201	123	162	201	mW

PARAMETER MEASUREMENT INFORMATION

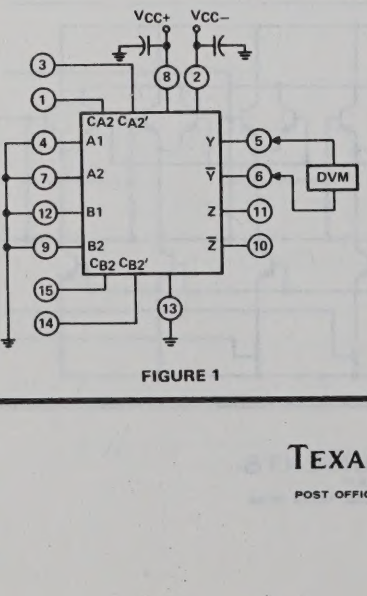
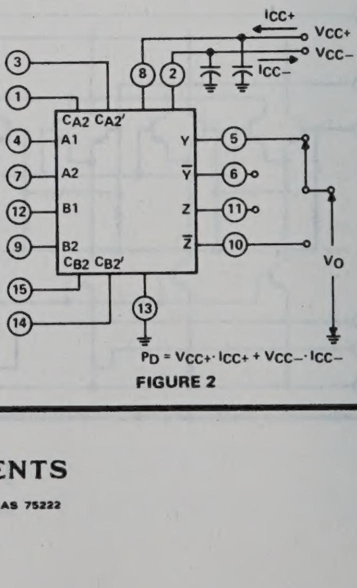


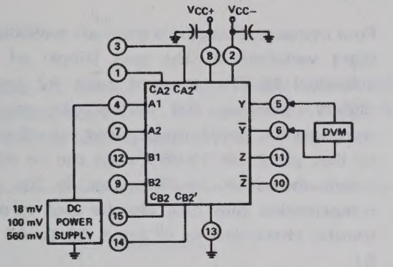
FIGURE 1



$P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$

FIGURE 2

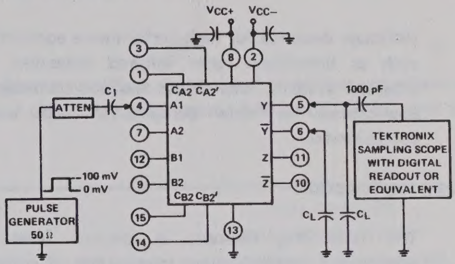
PARAMETER MEASUREMENT INFORMATION


VCC+
VCC−
3
1
8
2
CA2 CA2'
4
A1
7
A2
12
B1
9
B2
CB2 CB2'
Y
5
Ȳ
6
Z
11
Z̄
10
DVM
18 mV
100 mV
560 mV
DC
POWER
SUPPLY
15
14
13

$$\text{Scale Factor} = \frac{[V_{out(560\ mV)} - V_{out(18\ mV)}]\ mV}{30\ dBV}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\ V_{out(560\ mV)} - 0.5\ V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3


VCC+
VCC−
3
1
8
2
CI
ATTEN
4
CA2 CA2'
A1
7
A2
12
B1
9
B2
CB2 CB2'
100 mV
0 mV
PULSE
GENERATOR
50 Ω
15
14
13
Y
5
Ȳ
6
Z
11
Z̄
10
1000 pF
TEKTRONIX
SAMPLING SCOPE
WITH DIGITAL
READOUT OR
EQUIVALENT
CL
CL

NOTES: A. The input pulse has the following characteristics: $t_w = 50$ ns, $t_r \leqslant 2$ ns, $t_f \leqslant 2$ ns, PRR = 10 MHz.

B. Capacitor C_I consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.

C. C_L includes probe and jig capacitance.

FIGURE 4

TYPICAL CHARACTERISTICS

TL441M
DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

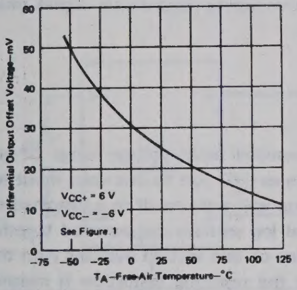


FIGURE 5

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

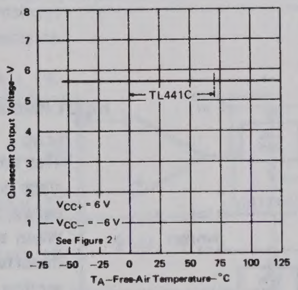


FIGURE 6

TL441M
D-C SCALE FACTOR
vs
FREE-AIR TEMPERATURE

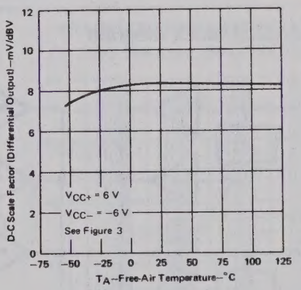


FIGURE 7

TL441M
D-C ERROR
vs
FREE-AIR TEMPERATURE

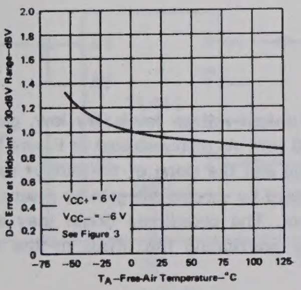


FIGURE 8

OUTPUT RISE TIME
vs
LOAD CAPACITANCE

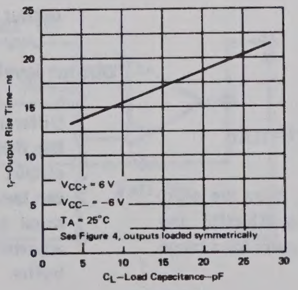


FIGURE 9

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

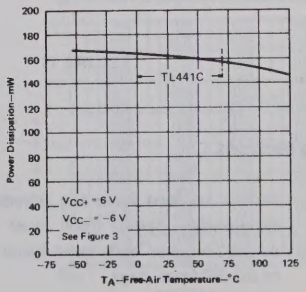


FIGURE 10

TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection, and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic log function

The basic log response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln\left[(I_C + I_{CES})/I_{CES}\right]$$

where: I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to noise.

functional block diagram

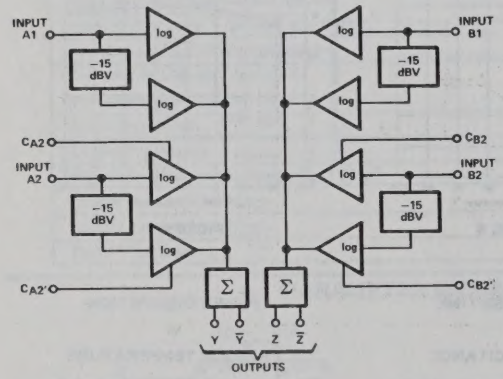


FIGURE 11

log sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dBV log subsection, and each input feeds two pairs for a range of 30 dBV per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dBV stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dBV stage can be adjusted to match the other 15-dBV stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 volt to one volt. Input levels in excess of one volt may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 volts, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 volts to ensure a clean output.

output levels

Differential-output-voltage levels are low, generally less than 0.6 volt. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using these logarithmic amplifiers. Operational amplifiers not otherwise designated are uA741. For operation at higher frequency, use of uA733 is recommended instead of uA741, with the differential outputs connected as in Figure 14.

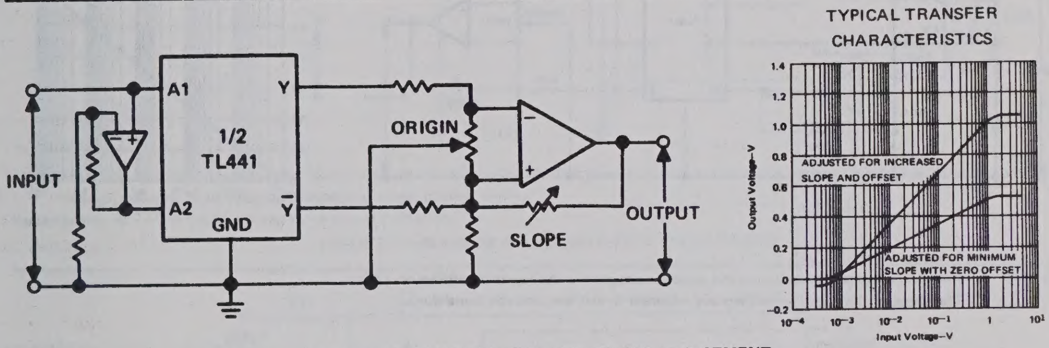

TYPICAL TRANSFER CHARACTERISTICS
INPUT
A1
Y
1/2
TL441
A2
$\overline{Y}$
GND
ORIGIN
SLOPE
OUTPUT
ADJUSTED FOR INCREASED SLOPE AND OFFSET
ADJUSTED FOR MINIMUM SLOPE WITH ZERO OFFSET
Output Voltage—V
Input Voltage—V
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0
−0.2
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10^1

FIGURE 12—OUTPUT SLOPE AND ORIGIN ADJUSTMENT

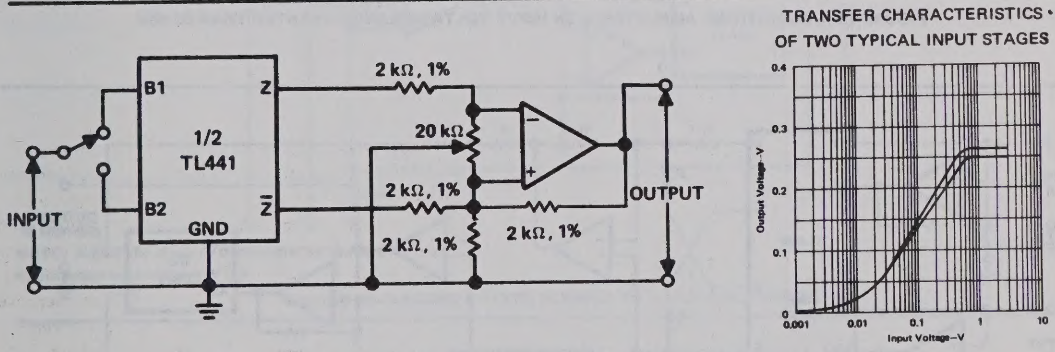

TRANSFER CHARACTERISTICS OF TWO TYPICAL INPUT STAGES
INPUT
B1
B2
Z
$\overline{Z}$
1/2
TL441
GND
2 kΩ, 1%
20 kΩ
2 kΩ, 1%
2 kΩ, 1%
2 kΩ, 1%
OUTPUT
Output Voltage—V
Input Voltage—V
0.4
0.3
0.2
0.1
0
0.001
0.01
0.1
1
10

FIGURE 13—UTILIZATION OF SEPARATE STAGES

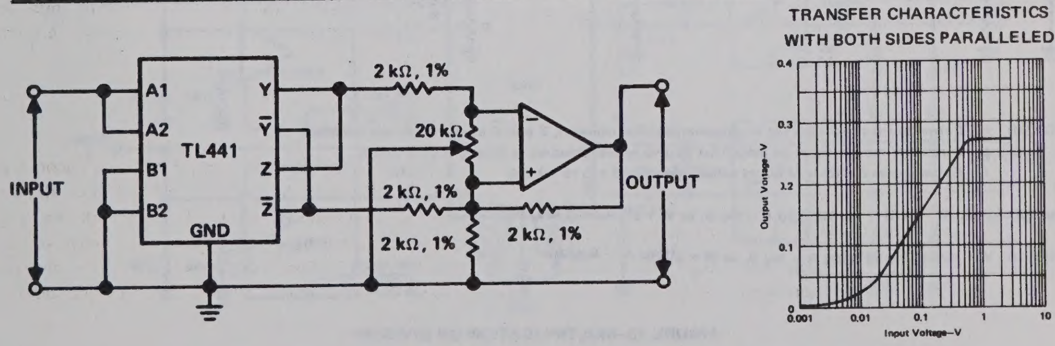
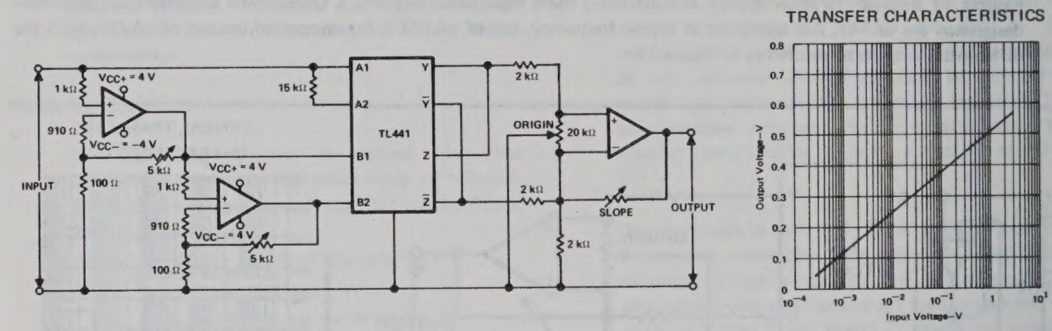

TRANSFER CHARACTERISTICS WITH BOTH SIDES PARALLELED
INPUT
A1
A2
B1
B2
Y
$\overline{Y}$
Z
$\overline{Z}$
TL441
GND
2 kΩ, 1%
20 kΩ
2 kΩ, 1%
2 kΩ, 1%
2 kΩ, 1%
OUTPUT
Output Voltage—V
Input Voltage—V
0.4
0.3
0.2
0.1
0
0.001
0.01
0.1
1
10

FIGURE 14—UTILIZATION OF PARALLELED INPUTS

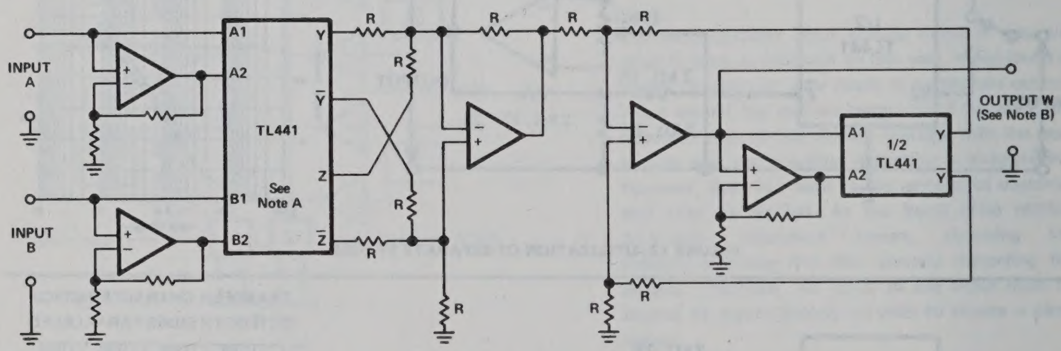
TYPICAL APPLICATION DATA


TRANSFER CHARACTERISTICS
Output Voltage—V
Input Voltage—V
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10^{1}
INPUT
1 kΩ
910 Ω
100 Ω
VCC+ = 4 V
VCC− = −4 V
5 kΩ
1 kΩ
910 Ω
100 Ω
VCC+ = 4 V
VCC− = −4 V
5 kΩ
15 kΩ
A1
A2
B1
B2
Y
$\overline{Y}$
Z
$\overline{Z}$
TL441
2 kΩ
ORIGIN
20 kΩ
2 kΩ
2 kΩ
SLOPE
OUTPUT

NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.

B. The gains of the input amplifiers are adjusted to achieve smooth transitions.

FIGURE 15—LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dBV


INPUT A
INPUT B
A1
A2
B1
B2
Y
$\overline{Y}$
Z
$\overline{Z}$
TL441
See Note A
R
R
R
R
R
R
R
R
R
R
OUTPUT W (See Note B)
A1
A2
Y
$\overline{Y}$
1/2 TL441

NOTES: A. Connections shown are for multiplication. For division, Z and $\overline{Z}$ connections are reversed.

B. Output W may need to be amplified to give actual product or quotient of A and B.

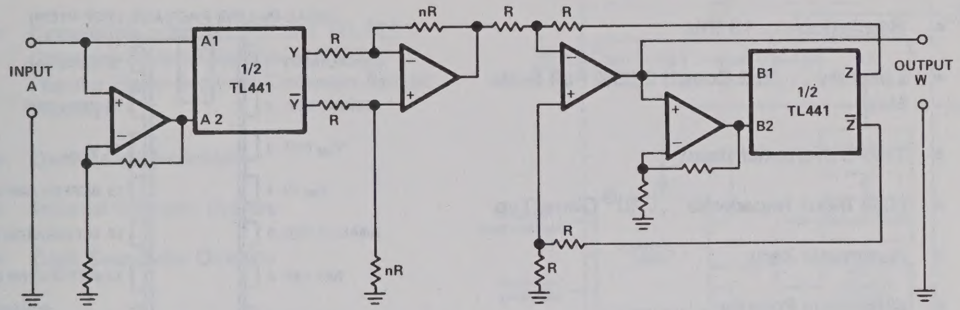
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A - \log_a B)}$

FIGURE 16—MULTIPLICATION OR DIVISION

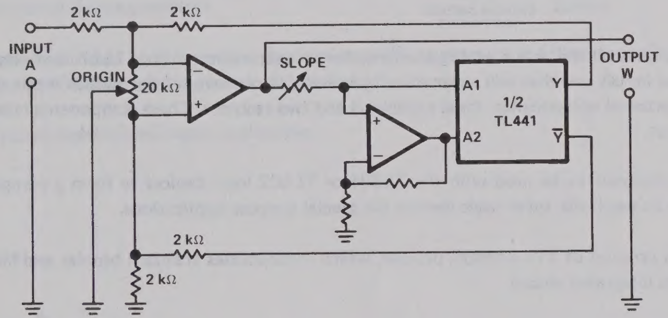
TYPICAL APPLICATION DATA


INPUT
A
A1
A 2
1/2
TL441
Y
Y̅
R
R
nR
nR
R
R
R
R
B1
B2
1/2
TL441
Z
Z̅
OUTPUT
W

NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17–RAISING A VARIABLE TO A FIXED POWER


2 kΩ
2 kΩ
INPUT
A
ORIGIN
20 kΩ
SLOPE
OUTPUT
W
A1
A2
1/2
TL441
Y
Y̅
2 kΩ
2 kΩ

NOTE: Adjust the slope to correspond to the base "a".

Exponential to any base: W = a

FIGURE 18–RAISING A FIXED NUMBER TO A VARIABLE POWER

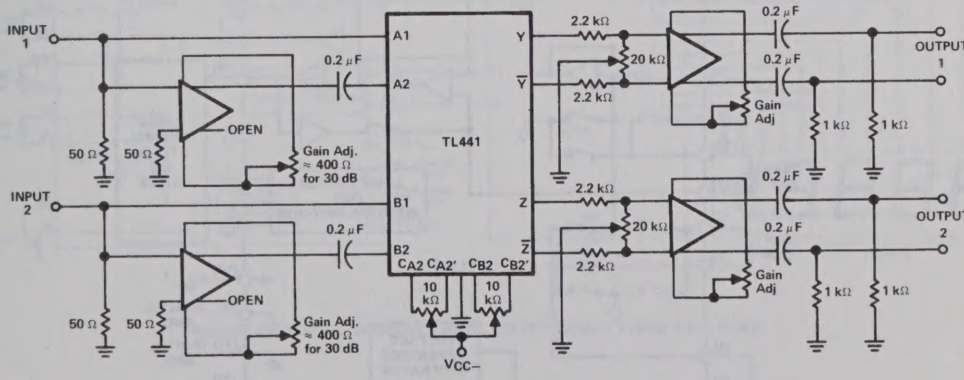

INPUT
1
A1
A2
0.2 μF
OPEN
50 Ω
50 Ω
Gain Adj.
≈ 400 Ω
for 30 dB
TL441
Y
Y̅
2.2 kΩ
2.2 kΩ
20 kΩ
0.2 μF
0.2 μF
Gain
Adj
1 kΩ
1 kΩ
OUTPUT
1
INPUT
2
B1
B2
0.2 μF
OPEN
50 Ω
50 Ω
Gain Adj.
≈ 400 Ω
for 30 dB
Z
Z̅
CA2 CA2′ CB2 CB2′
10
kΩ
10
kΩ
VCC–
2.2 kΩ
2.2 kΩ
20 kΩ
0.2 μF
0.2 μF
Gain
Adj
1 kΩ
1 kΩ
OUTPUT
2

FIGURE 19–DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

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TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

FUTURE PRODUCT
TO BE ANNOUNCED

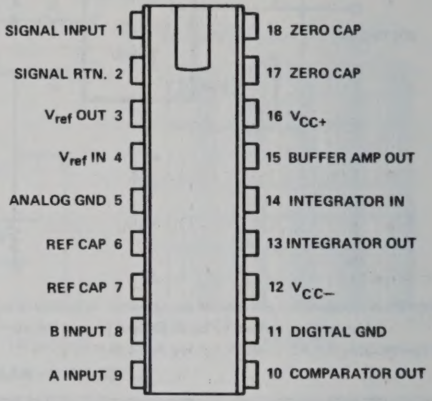
TYPE TL500
ANALOG PROCESSOR

JUNE 1976

features

- Resolution . . . 13 Bits
- Linearity . . . (±1 Count) 0.05% Full Scale Max
- True Differential Input
- High Input Impedance . . . 10^8 Ohms Typ
- Automatic Zero
- Automatic Polarity
- Internal Precision Voltage Reference
- 200 Conversions/Second Typ

N
DUAL-IN-LINE PACKAGE (TOP VIEW)


SIGNAL INPUT 1
SIGNAL RTN. 2
V_{ref} OUT 3
V_{ref} IN 4
ANALOG GND 5
REF CAP 6
REF CAP 7
B INPUT 8
A INPUT 9
18 ZERO CAP
17 ZERO CAP
16 V_{CC+}
15 BUFFER AMP OUT
14 INTEGRATOR IN
13 INTEGRATOR OUT
12 V_{CC-}
11 DIGITAL GND
10 COMPARATOR OUT

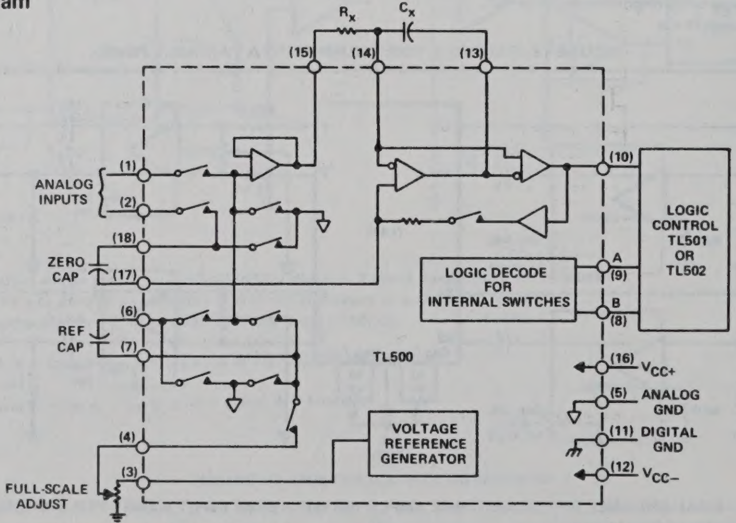
description

The TL500 contains all the active analog elements for an automatic zeroing, 13-bit dual-slope A/D converter that has true differential inputs and that will automatically indicate the polarity of the applied input signal. The TL500 requires a total of five external components: three capacitors and two resistors. These components need no special matching nor special tolerances.

The TL500 is designed to be used with the TL501 or TL502 logic devices to form a complete A/D converter; however, it can also be used with other logic devices for special purpose applications.

The TL500 is a product of TI's BI-MOS process, which incorporates standard bipolar and MOSFET transistors on the same monolithic integrated circuit.

functional diagram


R_x
C_x
(15)
(14)
(13)
(10)
ANALOG INPUTS
(1)
(2)
(18)
ZERO CAP
(17)
(6)
REF CAP
(7)
(4)
(3)
FULL-SCALE ADJUST
LOGIC DECODE FOR INTERNAL SWITCHES
A
(9)
B
(8)
LOGIC CONTROL TL501 OR TL502
TL500
VOLTAGE REFERENCE GENERATOR
(16) V_{CC+}
(5) ANALOG GND
(11) DIGITAL GND
(12) V_{CC-}

TENTATIVE DATA SHEET
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

**FUTURE PRODUCT
TO BE ANNOUNCED**

TYPE TL502
DIGITAL PANEL METER
LOGIC CONTROL DEVICE

JUNE 1976

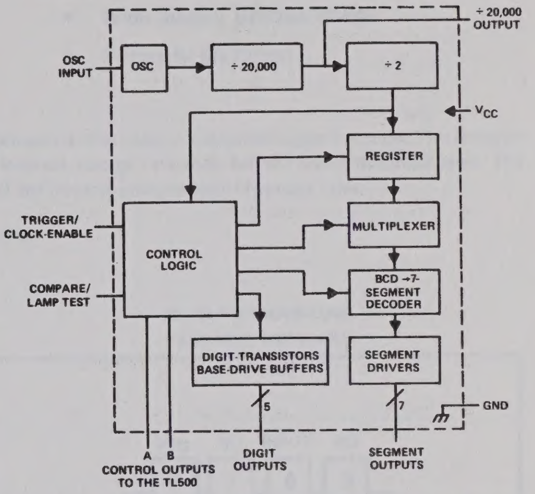
features

- **Compatible with TIL330 and TIL321 Common-Anode Displays, and Other Popular Seven-Segment Common-Anode Displays**
- **Over-Range Indicator**
- **Internal Segment Drivers**
- **Digit Base-Drive Outputs**

description

The TL502 is a 4½-digit Digital Panel Meter Logic Device. It is designed to interface with the TL500 analog processor, to provide base drive for the external p-n-p digit drivers, and to drive LED segments through external limiting resistors.

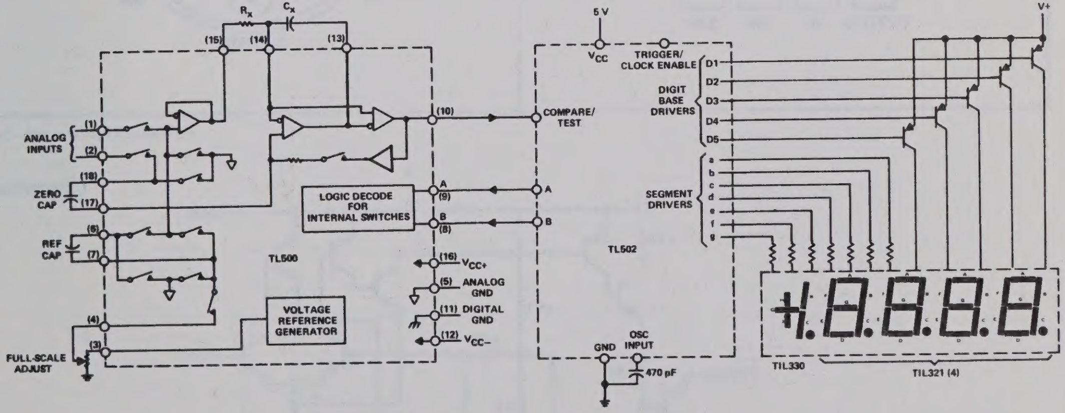
functional block diagram



÷ 20,000 OUTPUT
OSC INPUT
OSC
÷ 20,000
÷ 2
V_{CC}
REGISTER
TRIGGER/ CLOCK-ENABLE
MULTIPLEXER
CONTROL LOGIC
COMPARE/ LAMP TEST
BCD →7- SEGMENT DECODER
DIGIT-TRANSISTORS BASE-DRIVE BUFFERS
SEGMENT DRIVERS
5
7
GND
A B
CONTROL OUTPUTS TO THE TL500
DIGIT OUTPUTS
SEGMENT OUTPUTS

The TL502 oscillator input can be driven directly from any TTL output, or a 470-pF capacitor connected between that input and ground will develop an internal clock frequency.

Figure 1 shows a typical digital panel meter application.



R_x
C_x
(15)
(14)
(13)
ANALOG INPUTS
(1)
(2)
(18)
ZERO CAP
(17)
(6)
REF CAP
(7)
TL500
(4)
(3)
FULL-SCALE ADJUST
LOGIC DECODE FOR INTERNAL SWITCHES
VOLTAGE REFERENCE GENERATOR
(10)
A
(9)
B
(8)
(16) V_{CC+}
(5) ANALOG GND
(11) DIGITAL GND
(12) V_{CC-}
5 V
V_{CC}
TRIGGER/ CLOCK ENABLE
COMPARE/ TEST
A
B
DIGIT BASE DRIVERS
D1
D2
D3
D4
D5
SEGMENT DRIVERS
a
b
c
d
e
f
g
TL502
GND
OSC INPUT
470 pF
V+
TIL330
TIL321 (4)

FIGURE 1- TYPICAL DIGITAL PANEL METER USING TL500 AND TL502

TENTATIVE DATA SHEET

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE TL560C
PRECISION LEVEL DETECTOR

BULLETIN NO. DL-S 7612400, MAY 1976

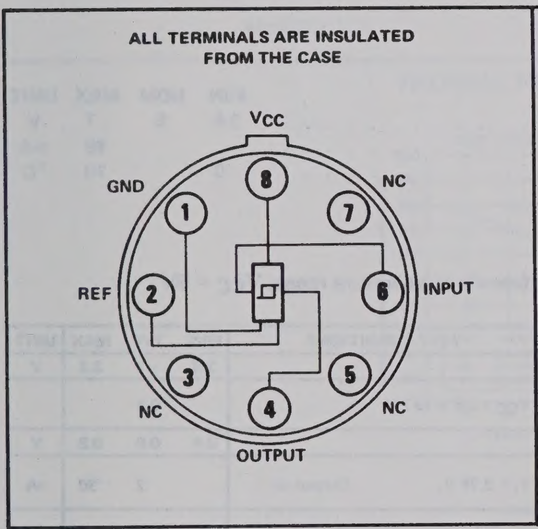
- Stable Threshold Level
- Low Input Current
- High Output Sink Current Capability
- Threshold Hysteresis
- Wide Supply Voltage Range
- Formerly SN72560

description

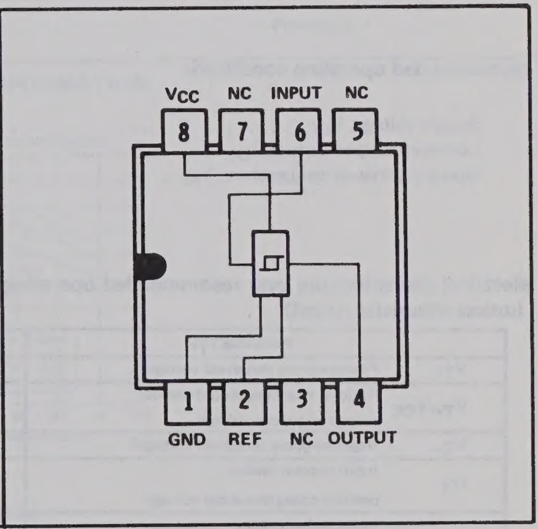
The TL560 is a precision level detector intended for applications that require a Schmitt-trigger function. The detector has excellent voltage and temperature stability and an internal voltage reference for the input threshold level. The reference-voltage pin is available for external adjustment of the positive-going threshold voltage level.

The TL560C is characterized for operation from 0°C to 70°C.

L PLUG-IN PACKAGE
(TOP VIEW)

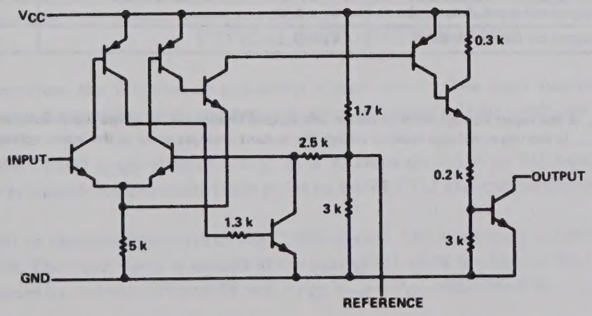

ALL TERMINALS ARE INSULATED
FROM THE CASE
VCC
GND
NC
8
1
7
REF
2
6
INPUT
3
5
4
NC
NC
OUTPUT

JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)


VCC
NC
INPUT
NC
8
7
6
5
1
2
3
4
GND
REF
NC
OUTPUT

NC—No internal connection

schematic


VCC
0.3 k
1.7 k
2.5 k
INPUT
0.2 k
OUTPUT
3 k
1.3 k
5 k
3 k
GND
REFERENCE

Resistor values shown are nominal and in ohms.

TYPE TL560C
PRECISION LEVEL DETECTOR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	V_{CC}
Output voltage (see Note 1)	25 V
Output sink current	160 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. For operation above 25°C free-air temperature refer to Dissipation Derating Curve, Figure 3. This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.5	5	7	V
Low-level output current, I_{OL}			48	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{T+}	Positive-going threshold voltage[†]			2.8	3	3.2	V
V_{T+}/V_{CC}	Ratio of positive-going threshold voltage to supply voltage	V_{CC} = 2.5 V to 7 V			0.6		
V_{T-}	Negative-going threshold voltage[‡]			0.4	0.6	0.8	V
I_{T+}	Input current below positive-going threshold voltage	V_I = 2.75 V,	Output on		2	30	nA
I_{T-}	Input current above negative-going threshold voltage	V_I = 1 V,	Output off		1.2		µA
$I_{O(off)}$	Off-state output current	V_I = 4 V,	V_O = 25 V			10	µA
$V_{O(on)}$	On-state output voltage	V_I = 0,	I_O = 48 mA		0.2	0.4	V
$I_{CC(off)}$	Supply current, output off (each detector)	V_I = 4 V			4.8	6.5	mA
$I_{CC(on)}$	Supply current, output on (each detector)	V_I = 0			10	15	mA

[†] Positive-going threshold voltage, V_{T+}, is the input voltage level at which the output changes state as the input voltage is increased.

[‡] Negative-going threshold voltage, V_{T-}, is the input voltage level at which the output changes state as the input voltage is decreased.

See data sheet DL-S 7412126, *Linear and Interface Circuits Ordering Instructions and Mechanical Data*, dated April 1974 and its Supplement, dated February 1976.

TYPICAL CHARACTERISTICS

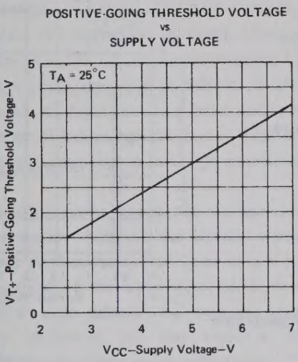


FIGURE 1

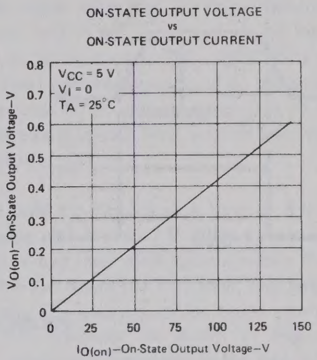
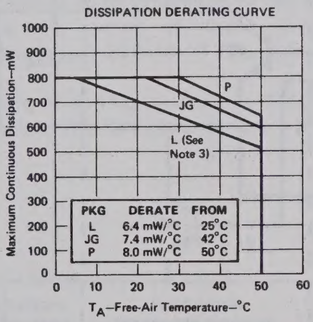


FIGURE 2

THERMAL INFORMATION



PKG	DERATE	FROM
L	6.4 mW/°C	25°C
JG	7.4 mW/°C	42°C
P	8.0 mW/°C	50°C

FIGURE 3

NOTE 3: This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

TYPICAL APPLICATION DATA

The TL560 performs the function of a Schmitt trigger circuit. The logic function is noninverting and has a wide hysteresis between the positive-going and negative-going threshold voltage levels (see Figure 4).

Operation of the TL560 is specified at a V_{CC} of 5 V, although 2.5-V to 7-V supply operation is possible. The device can be used with popular logic systems (such as Series 54/74 TTL) and standard battery voltages.

Figure 5 is used to illustrate operation of the TL560 circuit. The input stage is a differential amplifier composed of Q1, Q2, Q3, and Q4. The input signal is applied at the base of Q1 while the base of Q2 is connected to an internal reference voltage determined by resistors R4 and R5 and V_{CC}; $V_{ref} = V_{CC} \cdot R5/(R4+R5)$.

TYPICAL APPLICATION DATA

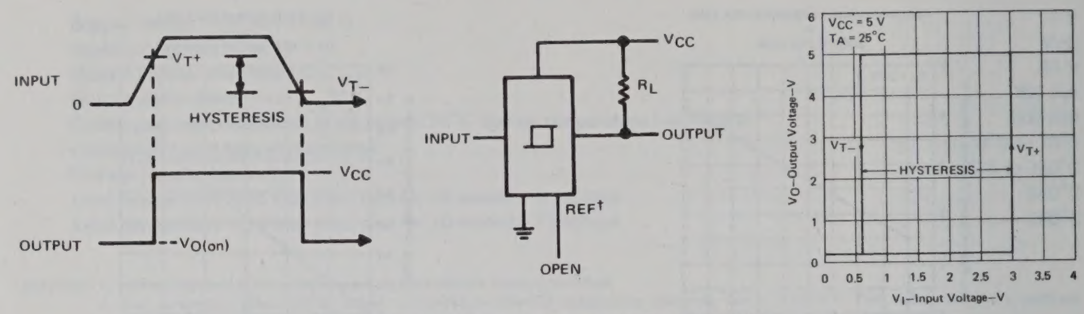


FIGURE 4—INPUT-OUTPUT TRANSFER FUNCTION

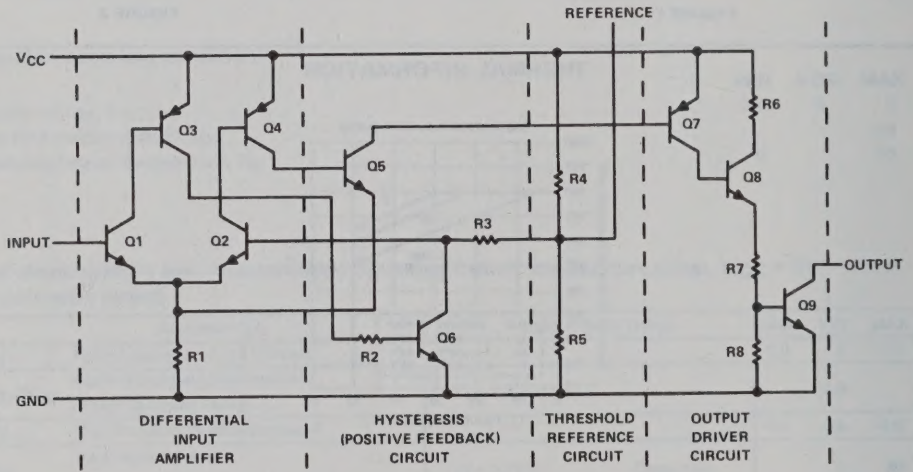

REFERENCE
V_{CC}
Q3
Q4
Q5
Q7
R6
Q8
R4
INPUT
Q1
Q2
R3
R7
OUTPUT
Q9
R1
R2
Q6
R5
R8
GND
DIFFERENTIAL INPUT AMPLIFIER
HYSTERESIS (POSITIVE FEEDBACK) CIRCUIT
THRESHOLD REFERENCE CIRCUIT
OUTPUT DRIVER CIRCUIT

FIGURE 5—FUNCTIONAL CIRCUIT DIAGRAM

If the base of Q1 is less positive than the base of Q2, Q2 conducts and causes Q4, Q5, Q7, Q8, and the output transistor, Q9, to conduct. Transistors Q2 and Q5 share the current in emitter resistor R1. Since Q1 does not conduct, Q3 and Q6 do not conduct. There is no base current in Q1, and therefore no current required from the input source. A very high input impedance therefore exists. Since Q2 is conducting, a small voltage drop exists across R3 due to Q2 base current.

If the input voltage is increased, Q1 does not conduct until the input voltage (base voltage of Q1) approaches the base voltage of Q2. Current is then switched from the emitters of Q2 and Q5 to the emitter of Q1. Conduction in Q1 causes current to flow in Q3 and Q6 which results in additional voltage drop in R3 and therefore a reduction in the base voltage of Q2. This positive feedback accelerates switching action and causes conduction to rapidly cease in Q2, Q4, Q5, Q7, Q8, and the output transistor, Q9. Conduction in Q6 causes the base of Q2 to assume a voltage (approximately 0.6 V) much lower than the original reference voltage (approximately 3 V). This results in hysteresis between the positive-going and negative-going threshold levels.

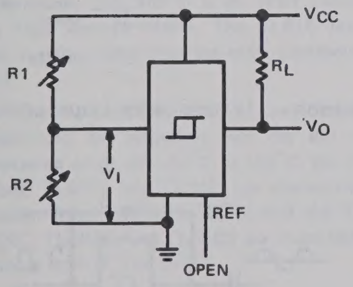
TYPICAL APPLICATION DATA

After switching occurs, the base current of Q1 increases to a somewhat higher value than just below threshold because of higher Q1 operating currents. Once the positive-going threshold level (≈3 V) has been reached, the input voltage must be reduced to the negative-going threshold level (≈0.6 V) before switching back to the original state will occur. Figure 4 illustrates the threshold levels of the TL560. Because the input current increases after the positive-going threshold voltage level has been exceeded, the input voltage will be reduced by an amount dependent on the source resistance. If the reduced input voltage is not below the negative-going threshold voltage level, a stable state will exist. If the source resistance is too high, oscillation or periodic switching may occur.

The positive-going threshold voltage level (V_{T+}) is guaranteed to be 3.00 ± 0.20 volts at a V_{CC} of 5 V. It is also approximately 60% of the supply voltage over the supply voltage range of 2.5 V to 7 V. With a resistor-capacitor network as illustrated in Figure 7, a V_{T+}/V_{CC} ratio of 60% results in a timed interval of approximately RC seconds, independent of the V_{CC} level. Since the input current is nominally 2 nA just below the V_{T+} level, very large values of R and/or large values of C may be used to achieve long-timed intervals. The duration of the timed interval may be greatly increased (at the expense of accuracy) by using a P-N-P transistor as shown in Figure 11 in a capacitance-multiplication technique. The timed interval is, however, sensitive to variations in the h_{FE} of the P-N-P transistor. Also for any of the timing applications, very-low-leakage capacitors are necessary for accurate operation.

The low input current (30 nA maximum for I_{T+}) and high output sink current (160 mA maximum) make the TL560 excellent in applications of interfacing between low-level systems and TTL systems where precision level detection is required. The output is capable of sinking up to a maximum of 160 mA with a TTL-compatible on-state voltage of 0.4 V maximum guaranteed at a sink current of 48 mA. With an appropriate output pull-up resistor (R_L ≈ 2 kΩ to 5 V), a fan-out of approximately 30 Series 74 TTL loads can be accommodated.

In addition to applications interfacing with TTL systems, the TL560 finds application in driving relays, lamps, solenoids, thyristors (SCRs and triacs), and other peripheral devices.



Output turns off when $V_I \geq V_{T+}$
Output turns on when $V_I \leq V_{T-}$

where $V_I = V_{CC}\frac{R2}{R1+R2}$

FIGURE 6–BASIC SENSOR CIRCUIT

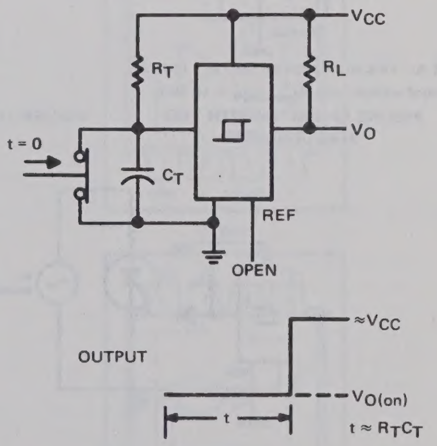


FIGURE 7–BASIC TIMED-INTERVAL CIRCUIT

TYPICAL APPLICATION DATA

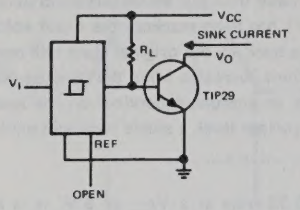

VCC
SINK CURRENT
RL
VO
VI
TIP29
REF
OPEN

FIGURE 8—EXTERNAL N-P-N TRANSISTOR FOR INCREASING SINK CURRENT

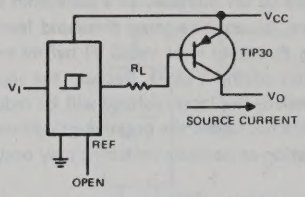

VCC
TIP30
RL
VI
VO
SOURCE CURRENT
REF
OPEN

FIGURE 9—EXTERNAL P-N-P TRANSISTOR FOR INCREASING SOURCE CURRENT

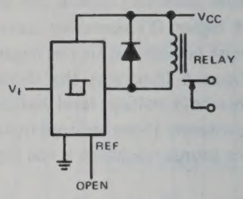

VCC
RELAY
VI
REF
OPEN

FIGURE 10—RELAY DRIVER

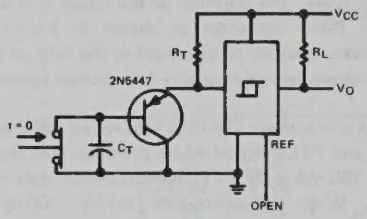

VCC
RT
RL
2N5447
VO
t = 0
CT
REF
OPEN

FIGURE 11—LONG-TIMED-INTERVAL CIRCUIT

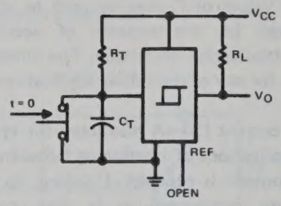
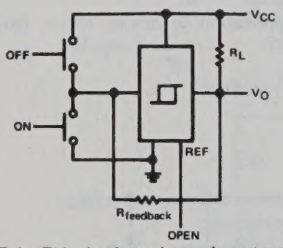

VCC
RT
RL
VO
t = 0
CT
REF
OPEN

FIGURE 12—BOUNCELESS SWITCH


VCC
OFF
RL
VO
ON
REF
Rfeedback
OPEN

NOTE A: This circuit can be used as a touch-control switch with $R_{feedback} \approx 10\ M\Omega$.

FIGURE 13—SWITCH WITH TWO STABLE STATES

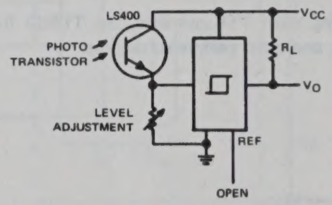

LS400
VCC
PHOTO TRANSISTOR
RL
VO
LEVEL ADJUSTMENT
REF
OPEN

FIGURE 14—LIGHT-LEVEL SENSOR

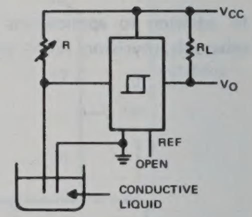

VCC
R
RL
VO
REF
OPEN
CONDUCTIVE LIQUID

FIGURE 15—LIQUID-LEVEL SENSOR

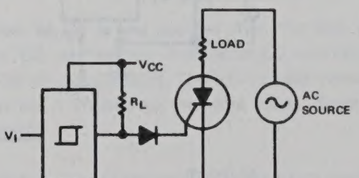

LOAD
VCC
RL
AC SOURCE
VI
REF
OPEN

FIGURE 16—THYRISTOR DRIVER CIRCUIT

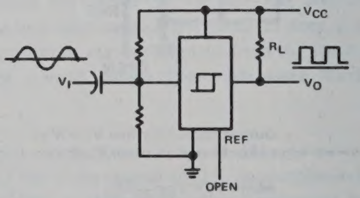

VCC
RL
VI
VO
REF
OPEN

FIGURE 17—SINE-WAVE-TO-SQUARE-WAVE CONVERTER

PRINTED IN U.S.A.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.

LINEAR INTEGRATED CIRCUITS

TYPES TL601, TL604, TL607, TL610
P-MOS ANALOG SWITCHES

BULLETIN NO. DL-S 7612401, JUNE 1976

- **Switches ±10-V Analog Signals**
- **TTL/DTL Logic Capability**
- **5- to 30-V Supply Ranges**
- **Low (100 Ω) On-State Resistance**
- **High (10^{11} Ω) Off-State Resistance**
- **8-Pin Functions**

description

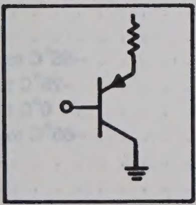
The TL601, TL604, TL607, and TL610 are a family of monolithic P-MOS analog switches that provide fast switching speeds with high r_{off}/r_{on} ratio and no offset voltage. The p-channel enhancement-type MOS switches will accept analog signals up to ±10 volts and are controlled by TTL-compatible logic inputs. The monolithic structure is made possible by BI-MOS technology, which combines p-channel MOS with standard bipolar transistors.

These switches are particularly suited for use in military, industrial, and commercial applications such as data acquisition, multiplexers, A/D and D/A converters, MODEMS, sample-and-hold systems, signal multiplexing, integrators, programmable operational amplifiers, programmable voltage regulators, crosspoint switching networks, logic interface, and many other analog systems.

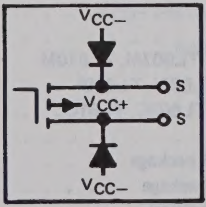
The TL601 is an SPDT switch with two logic control inputs. The TL604 is a dual complementary SPST switch with a single control input. The TL607 is an SPDT switch with one logic control input and one enable input. The TL610 is an SPST switch with three logic control inputs. The TL610 features a higher r_{off}/r_{on} ratio than the other members of the family.

The TL601M, TL604M, TL607M, and TL610M are characterized for operation over the full military temperature range of −55°C to 125°C, the TL601I, TL604I, TL607I, and TL610I are characterized for operation from −25°C to 85°C, and the TL601C, TL604C, TL607C, and TL610C are characterized for operation from 0°C to 70°C.

TYPICAL OF ALL INPUTS

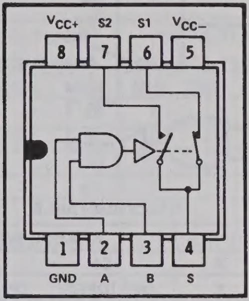


TYPICAL OF ALL SWITCHES

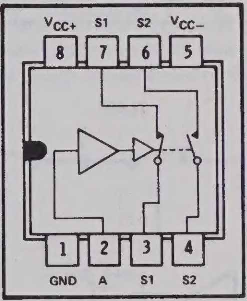


JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

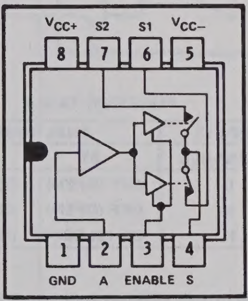
TL601



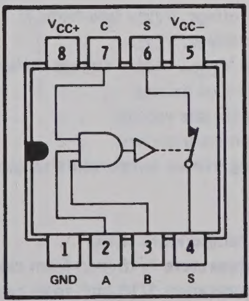
TL604



TL607



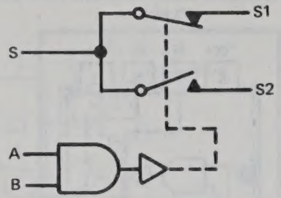
TL610



Switch positions shown are for all inputs high.

TYPES TL601, TL604, TL607, TL610
P-MOS ANALOG SWITCHES

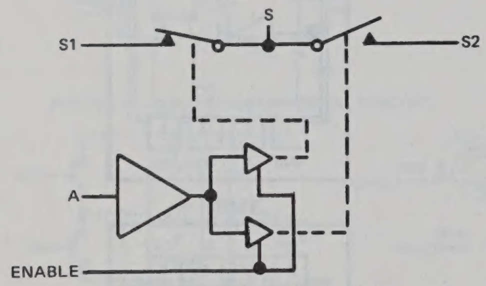
TL601



FUNCTION TABLE

LOGIC INPUTS		ANALOG SWITCH	
A	B	S1	S2
L	X	OFF (OPEN)	ON (CLOSED)
X	L	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)

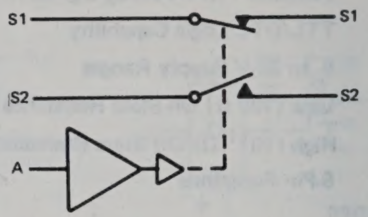
TL607



FUNCTION TABLE

INPUTS		ANALOG SWITCH	
A	ENABLE	S1	S2
X	L	OFF (OPEN)	OFF (OPEN)
L	H	OFF (OPEN)	ON (CLOSED)
H	H	ON (CLOSED)	OFF (OPEN)

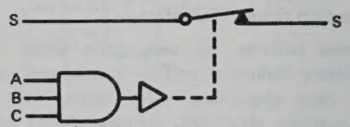
TL604



FUNCTION TABLE

LOGIC INPUT	ANALOG SWITCH	
A	S1	S2
H	ON (CLOSED)	OFF (OPEN)
L	OFF (OPEN)	ON (CLOSED)

TL610



FUNCTION TABLE

INPUTS			ANALOG SWITCH
A	B	C	S
L	X	X	OFF (OPEN)
X	L	X	OFF (OPEN)
X	X	L	OFF (OPEN)
H	H	H	ON (CLOSED)

H = high logic level
L = low logic level
X = irrelevant

Switch positions shown are for all inputs high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	30 V
Supply voltage, V_{CC-}	−30 V
V_{CC+} to V_{CC-} supply voltage differential	35 V
Control input voltage	V_{CC+}
Switch off-state voltage	30 V
Switch on-state current	10 mA
Operating free-air temperature range: TL601M, TL604M, TL607M, TL610M	−55°C to 125°C
TL601I, TL604I, TL607I, TL610I	−25°C to 85°C
TL601C, TL604C, TL607C, TL610C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	TL601M, TL604M TL607M, TL610M			TL601I, TL604I TL607I, TL610I			TL601C, TL604C TL607C, TL610C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+} (see Figure 1)	5	10	25	5	10	25	5	10	25	V
Supply voltage, V_{CC-} (see Figure 1)	–5	–20	–25	–5	–20	–25	–5	–20	–25	V
V_{CC+} to V_{CC-} supply voltage differential (see Figure 1)	15		30	15		30	15		30	V
Control input voltage	0		5.5	0		5.5	0		5.5	V
Switch on-state current			10			10			10	mA
Operating free-air temperature, T_A	–55		125	–25		85	0		70	°C

Figure 1 shows power supply boundry conditions for proper operation of the TL601 Series. The range of operation for supply V_{CC+} from +5 V to +25 V is shown on the vertical axis. The range of supply V_{CC-} from –5 V to –25 V is shown on the horizontal axis. A recommended 30-volt maximum voltage differential from V_{CC+} to V_{CC-} governs the maximum V_{CC+} for a chosen V_{CC-} (or vice versa). A minimum recommended difference of 15 volts from V_{CC+} to V_{CC-} and the boundaries shown in Figure 1 allow the designer to select the proper combinations of the two supplies.

RECOMMENDED COMBINATIONS
OF SUPPLY VOLTAGES

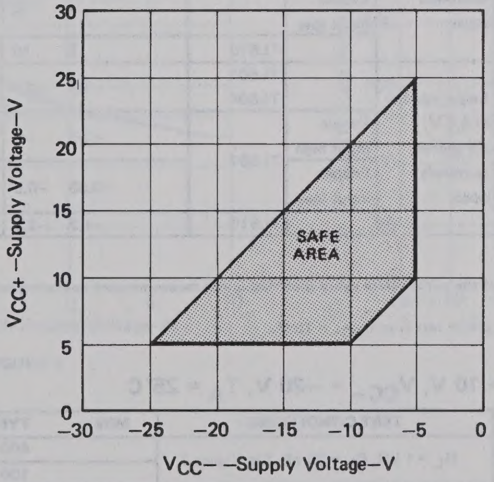


FIGURE 1

electrical characteristics over recommended operating free-air temperature range, $V_{CC+} = 10$ V, $V_{CC-} = -20$ V, analog switch test current = 1 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TL6--M TL6--I			TL6--C			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level control input voltage				2			2			V
V_{IL}	Low-level control input voltage						0.8			0.8	V
I_{IH}	High-level control input current	$V_I = 5.5$ V				0.5	10		0.5	10	μA
I_{IL}	Low-level control input current	$V_I = 0.4$ V				−50	−250		−50	−250	μA
I_{off}	Switch off-state current	$V_{I(sw)} = -10$ V, See Note 2		$T_A = 25°C$		−400	−800		−500	−1000	pA
				T_A = MAX		−50	−100		−10	−20	nA
r_{on}	Switch on-state resistance	$V_{I(sw)} = 10$ V, $I_{O(sw)} = -1$ mA		TL601 TL604 TL607		55	100		75	200	Ω
				TL610		40	80		40	100	
		$V_{I(sw)} = -10$ V, $I_{O(sw)} = -1$ mA		TL601 TL604 TL607		220	400		220	600	
				TL610		120	300		120	400	
r_{off}	Switch off-state resistance					1×10^{11}			5×10^{10}		Ω
C_{on}	Switch on-state input capacitance	$V_{I(sw)} = 0$ V, f = 1 MHz				16			16		pF
C_{off}	Switch off-state input capacitance	$V_{I(sw)} = 0$ V, f = 1 MHz				8			8		pF
I_{CC+}	Supply current from V_{CC+}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		5	10		5	10	mA
			Enable input high	TL607		5	10		5	10	
			Enable input low			3	5		3	5	
				TL610		5	10		5	10	
I_{CC-}	Supply current from V_{CC-}	Logic input(s) at 5.5 V, All switch terminals open		TL601 TL604		−1.2	−2.5		−1.2	−2.5	mA
			Enable input high	TL607		−2.5	−5		−2.5	−5	
			Enable input low			−0.05	−0.5		−0.05	−0.5	
				TL610		−1.2	−2.5		−1.2	−2.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

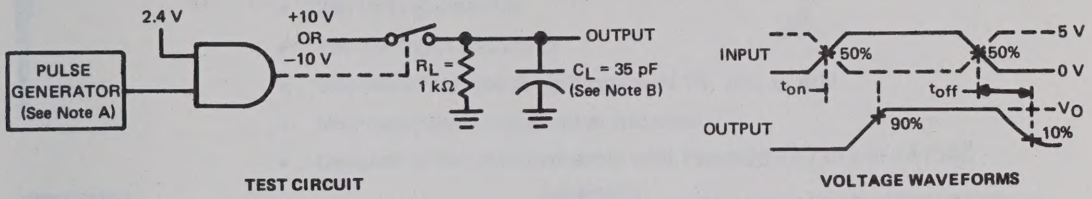
‡All typical values are at $T_A = 25°C$.

NOTE 2: The other terminal of the switch under test is at $V_{CC+} = 10$ V.

switching characteristics, $V_{CC} = 10$ V, $V_{CC-} = -20$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Switch turn-off time	$R_L = 1$ kΩ, $C_L = 35$ pF, See Figure 2		400	500	ns
t_{on}	Switch turn-on time			100	150	

PARAMETER MEASUREMENT INFORMATION


2.4 V
+10 V
OR
−10 V
PULSE
GENERATOR
(See Note A)
R_L =
1 kΩ
OUTPUT
C_L = 35 pF
(See Note B)
INPUT
50%
50%
5 V
0 V
t_{on}
t_{off}
V_O
OUTPUT
90%
10%

TEST CIRCUIT

VOLTAGE WAVEFORMS

$$V_O = (10\text{ V})\,\frac{1\text{ k}\Omega}{1\text{ k}\Omega + r_{on}}$$

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ns, t_f = 15 ns, t_w = 500 ns.

B. C_L includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTCS

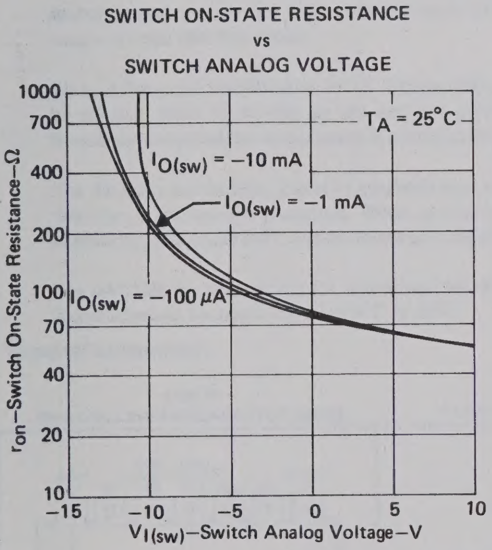

SWITCH ON-STATE RESISTANCE
vs
SWITCH ANALOG VOLTAGE

FIGURE 3

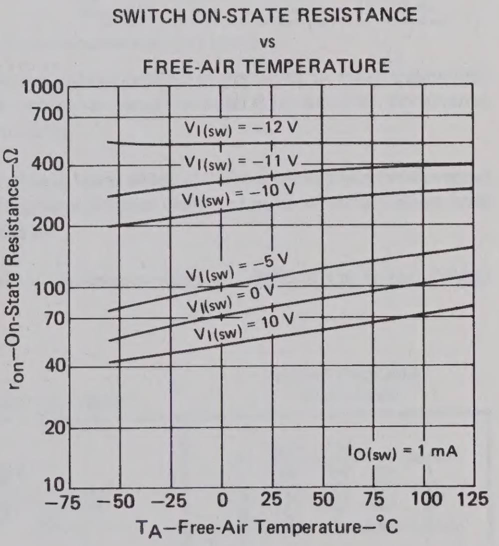

SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

FIGURE 4

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TYPES uA733M, uA733C
DIFFERENTIAL VIDEO AMPLIFIERS

BULLETIN NO. DL-S 7611415, NOVEMBER 1970—REVISED JUNE 1976

FORMERLY SN52733, SN72733

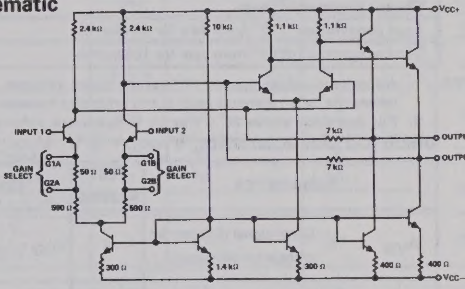
- **200 MHz Bandwidth**
- **250 kΩ Input Resistance**
- **Selectable Nominal Amplification of 10, 100, or 400**
- **No Frequency Compensation Required**
- **Designed to be Interchangeable with Fairchild μA733 and μA733C**

description

The uA733 is a monolithic two-stage video amplifier with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

schematic


VCC+
2.4 kΩ
2.4 kΩ
10 kΩ
1.1 kΩ
1.1 kΩ
INPUT 1
INPUT 2
7 kΩ
OUTPUT 1
OUTPUT 2
7 kΩ
GAIN SELECT
G1A
G2A
50 Ω
50 Ω
G1B
G2B
GAIN SELECT
500 Ω
500 Ω
300 Ω
1.4 kΩ
300 Ω
400 Ω
400 Ω
VCC−

Component values shown are nominal

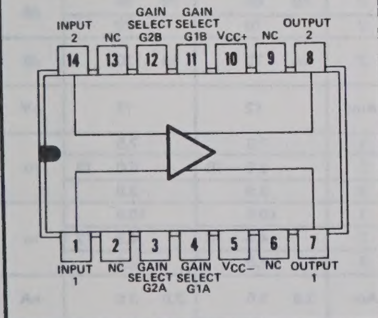
Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between G1A and G1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

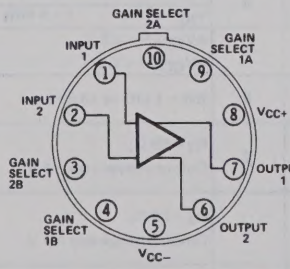
The uA733M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA733C is characterized for operation from 0°C to 70°C.

terminal assignments

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

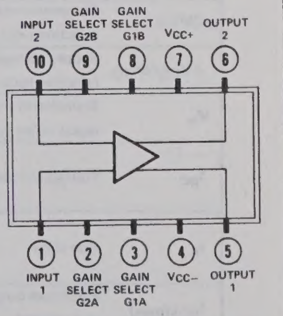

INPUT 2
NC
GAIN SELECT G2B
GAIN SELECT G1B
VCC+
NC
OUTPUT 2
14
13
12
11
10
9
8
1
2
3
4
5
6
7
INPUT 1
NC
GAIN SELECT G2A
GAIN SELECT G1A
VCC−
NC
OUTPUT 1

L
PLUG-IN PACKAGE (TOP VIEW)


GAIN SELECT 2A
INPUT 1
GAIN SELECT 1A
INPUT 2
VCC+
GAIN SELECT 2B
OUTPUT 1
GAIN SELECT 1B
OUTPUT 2
VCC−
1
2
3
4
5
6
7
8
9
10

PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE

U FLAT PACKAGE
(TOP VIEW)


INPUT 2
GAIN SELECT G2B
GAIN SELECT G1B
VCC+
OUTPUT 2
10
9
8
7
6
1
2
3
4
5
INPUT 1
GAIN SELECT G2A
GAIN SELECT G1A
VCC−
OUTPUT 1

NC—No internal connection

TYPES uA733M, uA733C
DIFFERENTIAL VIDEO AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA733M	uA733C	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)		500	500	mW
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16" from case for 60 seconds	J, L, or U package	300	300	°C
Lead temperature 1/16" from case for 10 seconds	N package	260	260	°C

NOTES: 1. All voltage values, except differential input voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

electrical characteristics, $V_{CC+} = 6$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN† SELECT	uA733M			uA733C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	$V_{OD} = 1$ V	1	300	400	500	250	400	600	
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	$R_S = 50\ \Omega$	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	µA
I_{IB}	Input bias current			Any		9	20		9	30	µA
V_I	Input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \leq 1$ V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \leq 1$ V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	$V_{IC} = \pm 1$ V, $f \leq 100$ kHz	2	60	86		60	86		dB
			$V_{IC} = \pm 1$ V, $f = 5$ MHz	2		70			70		
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	$\Delta V_{CC+} = \pm 0.5$ V, $\Delta V_{CC-} = \pm 0.5$ V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		µV
t_{pd}	Propagation delay time	2	$R_S = 50\ \Omega$, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	$R_S = 50\ \Omega$, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, No signal	Any		16	24		16	24	mA

† The gain selection is made as follows:

Gain 1 . . . Gain Select pin G1A is connected to pin G1B, and pins G2A and G2B are open.
Gain 2 . . . Gain Select pin G1A and pin G1B are open, pin G2A is connected to pin G2B.
Gain 3 . . . All four gain-select pins are open.

electrical characteristics (continued), $V_{CC+} = 6$ V, $V_{CC-} = -6$ V
$T_A = -55°C$ to 125°C for uA733M, 0°C to 70°C for uA733C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN† SELECT	uA733M		uA733C		UNIT
					MIN	MAX	MIN	MAX	
A_{VD}	Large-signal differential voltage amplification	1	$V_{OD} = 1$ V	1	200	600	250	600	
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		5		6	μA
I_{IB}	Input bias current			Any		40		40	μA
V_I	Input voltage range	1		Any	±1		±1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.2		1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.5		2.8		V
r_i	Input resistance	3	$V_{OD} \leq 1$ V	2	8		8		kΩ
CMRR	Common-mode rejection ratio	4	$V_{IC} = \pm1$ V, $f \leq 100$ kHz	2	50		50		dB
			$V_{IC} = \pm1$ V, $f = 5$ MHz	2					
$\Delta V_{CC}/\Delta V_{IO}$	Supply voltage rejection ratio	1	$\Delta V_{CC+} = \pm0.5$ V, $\Delta V_{CC-} = \pm0.5$ V	2	50		50		dB
$I_{sink(max)}$	Maximum output sink current			Any	2.2		2.5		mA
I_{CC}	Supply current		No load, no signal	Any		27		27	mA

†The gain selection is made as follows:
Gain 1 . . . Gain Select pin G1A is connected to pin G1B, and pins G2A and G2B are open.
Gain 2 . . . Gain Select pin G1A and pin G1B are open, pin G2A is connected to pin G2B.
Gain 3 . . . All four gain-select pins are open.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage that if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$) The absolute value of the ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

Equivalent Input Noise Voltage (V_n) The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents I_{CC1} and I_{CC2}.

PARAMETER MEASUREMENT INFORMATION

test circuits

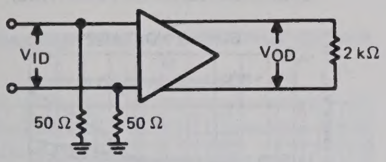

V_{ID}
V_{OD}
2 kΩ
50 Ω
50 Ω

FIGURE 1

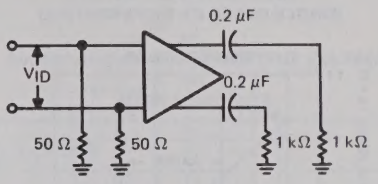

0.2 μF
V_{ID}
0.2 μF
50 Ω
50 Ω
1 kΩ
1 kΩ

FIGURE 2

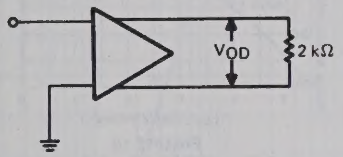


FIGURE 3

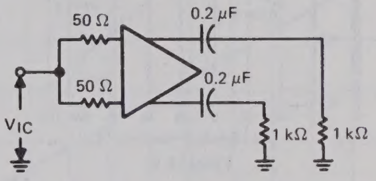

50 Ω
0.2 μF
50 Ω
0.2 μF
V_{IC}
1 kΩ
1 kΩ

FIGURE 4

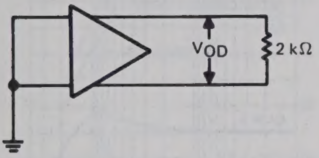
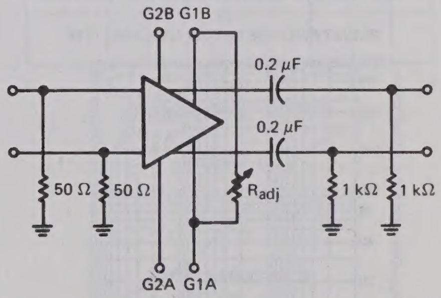


FIGURE 5


G2B G1B
0.2 μF
0.2 μF
50 Ω
50 Ω
R_{adj}
1 kΩ
1 kΩ
G2A G1A

VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

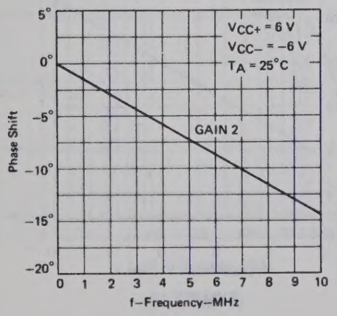


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

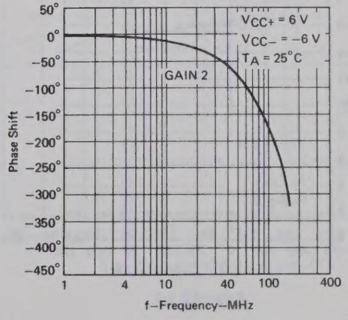


FIGURE 8

TYPICAL CHARACTERISTICS

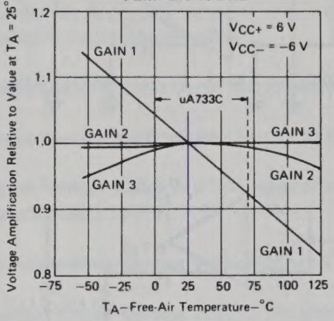

VOLTAGE AMPLIFICATION (SINGLE-ENDED OR DIFFERENTIAL) vs TEMPERATURE

FIGURE 9

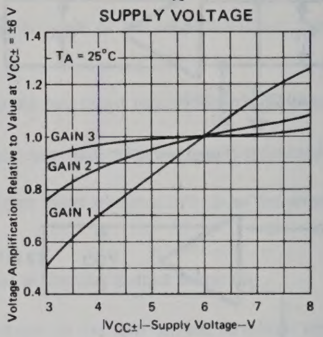

VOLTAGE AMPLIFICATION (SINGLE-ENDED OR DIFFERENTIAL) vs SUPPLY VOLTAGE

FIGURE 10

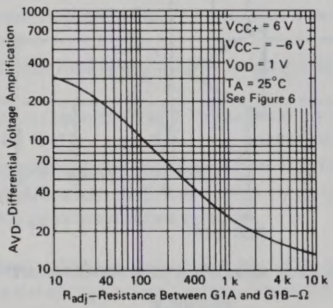

DIFFERENTIAL VOLTAGE AMPLIFICATION vs RESISTANCE BETWEEN G1A AND G1B

FIGURE 11

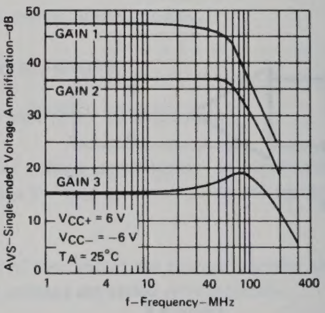

SINGLE-ENDED VOLTAGE AMPLIFICATION vs FREQUENCY

FIGURE 12

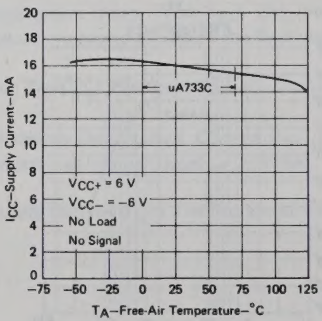

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

FIGURE 13

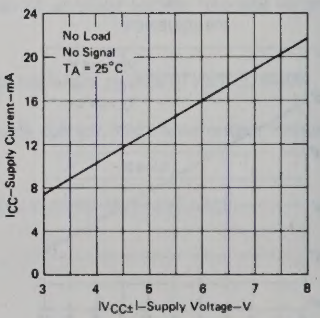

SUPPLY CURRENT vs SUPPLY VOLTAGE

FIGURE 14

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

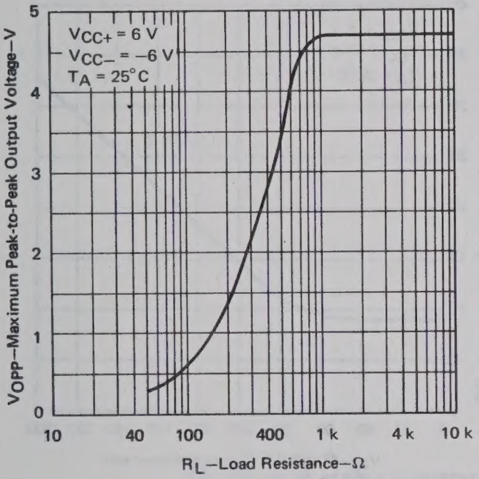


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

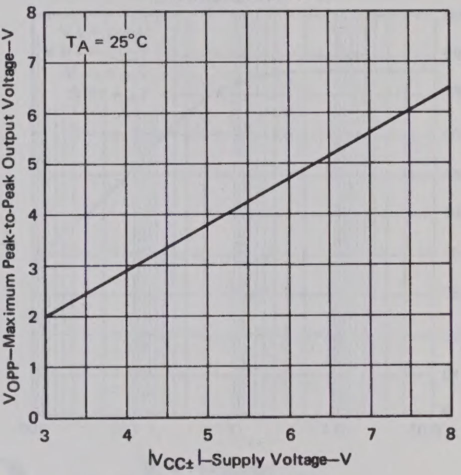


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

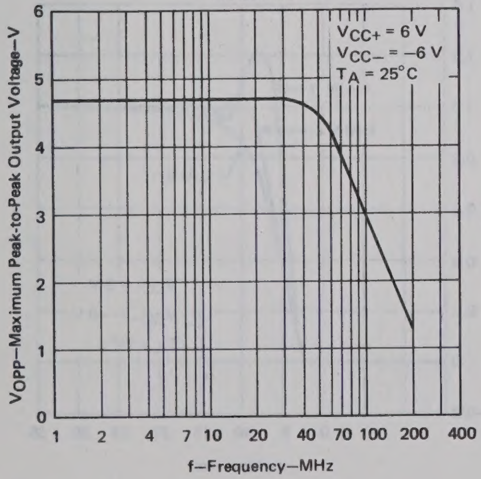


FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

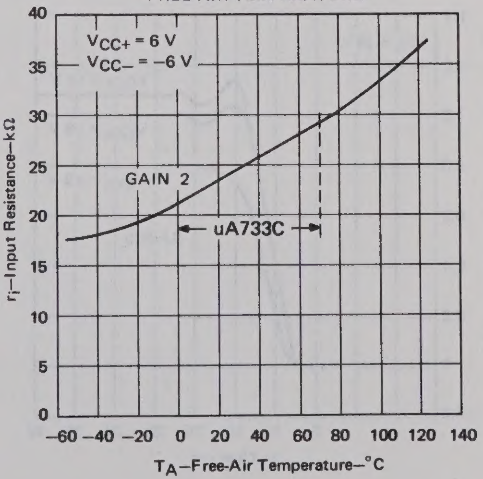
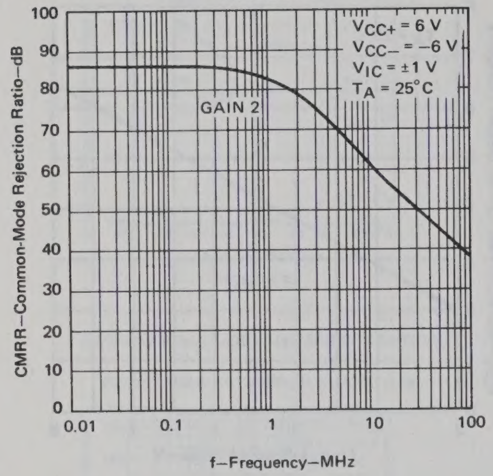


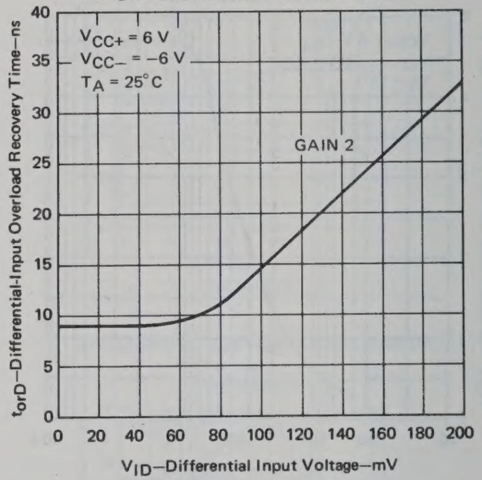
FIGURE 18

TYPICAL CHARACTERISTICS



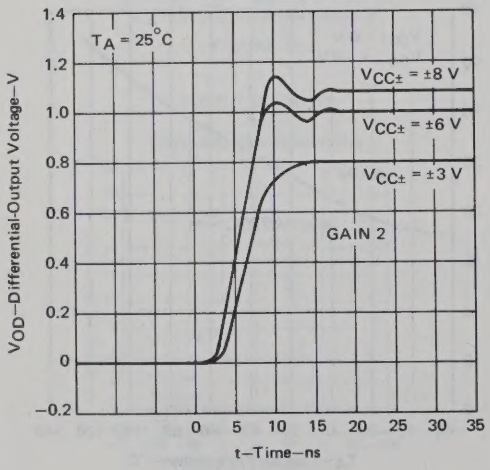
COMMON-MODE REJECTION RATIO
vs
FREQUENCY

FIGURE 19



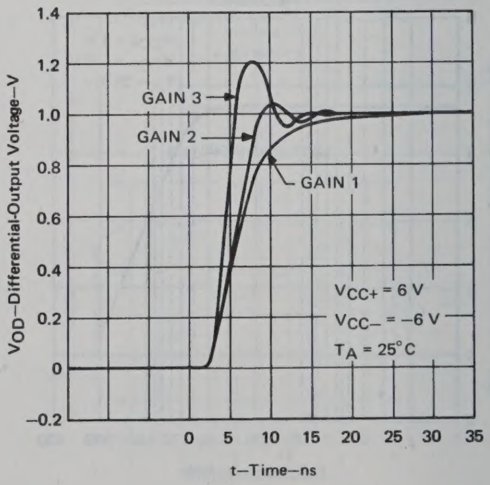
DIFFERENTIAL INPUT OVERLOAD RECOVERY TIME
vs
DIFFERENTIAL INPUT VOLTAGE

FIGURE 20



PULSE RESPONSE
AS A FUNCTION OF
SUPPLY VOLTAGE

FIGURE 21



PULSE RESPONSE
AS A FUNCTION OF GAIN

FIGURE 22

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Military Products

MIL-M-38510 AND MIL-STD-883 MILITARY HIGH REL INTEGRATED CIRCUITS

The Texas Instruments MIL-M-38510 and MIL-STD-883 programs offer a variety of options designed to meet contractual, reliability, and cost goals. MIL-M-38510 and MIL-STD-883 have been fully implemented to provide a broad product line of control circuits for both military original equipment and logistic requirements. Included in this section is a complete cross reference from the JAN part number to the corresponding standard catalog part number for ease in locating the commerical equivalent. The cross-reference from the catalog number to the JAN slash sheet number is also included.

When system designs utilize control circuits not listed on the current QPL or where no slash sheet specification exists, the TI /883 or MIL-M-38510 JAN-processed program is recommended as a cost-effective substitute for non-standard program drawings or specifications.

As an aid to predicting system reliability performance, the following is the estimated quality factor, Π_Q, for Texas Instruments Linear Control Circuits, when processed to the options outlined in Table A.

OPTION		Π_Q
JAN MIL-M-38510	CLASS B	2
JAN-PROCESSED	CLASS B	3
/883B		4
STANDARD HERMETIC		10

The following military documents (see Note 1) establish the processing, quality, and reliability assurance requirements for JAN integrated circuits. The detail requirements of each individual JAN device are specified in the slash sheets.

MIL-M-38510/XXX, Microcircuits, Digital, TTL, . . . , . . . ,
Monolithic Silicon (Slash Sheets)
MIL-M-38510, Microcircuits, General Specification for
MIL-STD-883, Test Methods and Procedures for Microelectronics
QPL-38510, Qualified Products List for MIL-M-38510

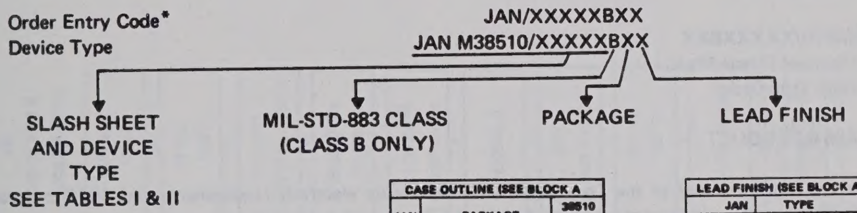
NOTE 1: Copies of these documents may be requested from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120.

MILITARY HIGH-REL PRODUCTS

I. JAN MIL-M-38510 CLASS B PRODUCT

These devices will be manufactured to the full requirements of the appropriate MIL-M-38510 slash sheet in DESC approved domestic production facilities. The TI Linear Department is supplying only Class B product (see Table A, Column I).

A. Ordering Instructions:



Order Entry Code* JAN/XXXXXBXX
Device Type JAN M38510/XXXXXBXX

SLASH SHEET AND DEVICE TYPE SEE TABLES I & II
MIL-STD-883 CLASS (CLASS B ONLY)
PACKAGE
LEAD FINISH

CASE OUTLINE (SEE BLOCK A		
JAN	PACKAGE	38510 (APP.C)
A	1/4" X 1/4" FLAT-14	F-1
B/T	1/4" X 1/8" FLAT-14	F-3
C	DIP-14	D-1
D	1/4" X 3/8" FLAT-14	F-2
E	DIP-16	D-2
F	1/4" X 3/8" FLAT-16	F-5
G	TO-99	A-1
H	1/4" X 1/4" FLAT-10	F-4
I	TO-100	A-2
J	DIP-24	D-3
K	3/8" X 5/8" FLAT-24	F-6
L	3/8" X 1/2" FLAT-24	F-7
‡	DIP-22	‡
‡	DIP-18	‡
X	TO-5	–
Y	TO-3	–
Z	1/4" X 3/8" FLAT-24	F-8

LEAD FINISH (SEE BLOCK A)	
JAN	TYPE
A	SOLDER DIP
B	TIN-PLATE
C	GOLD-PLATE
X	OPTIONAL‡

BLOCK A JAN CASE OUTLINE & FINISH FOR TI FAMILIES												
PRODUCT	A	B	C	D	E	F	G	I	J	L		
SERIES 54			X	X	X	X			X	X		
SERIES 54H			X	X	X	X						
SERIES 54L		X	X		X							
SERIES 54LS			X	X	X	X			X	X		
SERIES 54S			X	X	X	X			X	X		
LINEAR CONTROL			X				X	X				
SERIES 55			X		X							
MOS LSI											X	X
LEAD FINISH A												
LEAD FINISH B			X	X	X	X			X	X	X	X
LEAD FINISH C		X					X	X				

B. Symbolization:

JM38510/XXXXXBXX
TI Symbol (Trade Mark)
4-Digit Date Code

---

*Order entry code is used because the TI order entry system is limited to 14 digits.

‡"X" Denotes finish A, B, or C at option of manufacturer. Devices will be marked A, B, or C as applicable.

MILITARY PRODUCTS

II. MIL-M-38510 JAN-PROCESSED CLASS B PRODUCT[§]

These devices will be tested to the electrical requirements of the JAN slash sheet specification and 100% processed to the MIL-STD-883 Class B requirements of Method 5004 (see Table A, Column II).

A. Ordering Instructions: same numbering system as JAN with the omission of the JAN designation (see 1 above)

Order Entry Code[*]	TL/XXXXXBXX
Device Type	M38510/XXXXXBXX

B. Symbolization:

M38510/XXXXXBXX
TI Symbol (Trade Mark)
4-Digit Date Code

III. 883 CLASS B PRODUCT

These devices will be tested to the Data Book full-temperature electrical requirements and 100% processed to the MIL-STD-883 Class B requirements of Method 5004 (see Table A, Column III).

A. Ordering Instructions:

	Device Prefix	Designator[¶]	Package	/883B
Example:	TL	497M	J	/883B

B. Symbolization:

(Device prefix, designator and package)[¶] /883B
TI Symbol (Trade Mark)
4-Digit Date Code

IV. STANDARD HERMETIC PRODUCT

This material will be tested to the Data Book electrical requirements and processed per Table A, Column IV.

A. Ordering Instructions:

Device Prefix Designator[¶] Package

B. Symbolization

(Device prefix, designator and package)[¶]
TI Symbol (Trade Mark)
4-Digit Date Code

---

[*] Order entry code is used because the TI order entry system is limited to 14 digits.

[§] Similar to TI SNJ JAN-Processed program.

[¶] See ordering instructions on page 35.

TABLE A
MILITARY PRODUCTS PROCESS FLOW

	MIL-STD-883	I JAN JM38510/XXXXX	II JAN-PROCESSED M38510/XXXXX	III 833 CLASS B XXXXX/883B	IV STANDARD HERMETIC
Visual Pre-Cap Method 2010	Condition B	40X and 100X	40X and 100X	40X and 100X	40X
Stabilization Bake Method 1008	Condition C	24 hrs/ +150°C	24 hrs/ +150°C	24 hrs/ +150°C	24 hrs/ +150°C
Temp. Cycle Method 1010	Condition C	10 cycles −65°C to +150°C	10 cycles −65°C to +150°C	10 cycles −65°C to +150°C	
Centrifuge Method 2001	Condition E	30,000 G's Y_1 Plane	30,000 G's Y_1 Plane	30,000 G's Y_1 Plane	
Fine Leak Method 1014	Condition A or B	5 X 10^{-8} atm cc/sec	5 X 10^{-8} atm cc/sec	5 X 10^{-8} atm cc/sec	1 X 10^{-7} atm cc/sec
Gross Leak Method 1014	Condition C	COND C	COND C	COND C	COND C
Electrical Test		JAN SLASH SHEET	JAN SLASH SHEET 25°C	25°C JAN ELECT	
Burn-In (minimum) Method 1015	Condition B or D	160 hrs 125°C	160 hrs 125°C	160 hrs 125°C	
Final Electrical	Method 5004	JAN SLASH SHEET	JAN SLASH SHEET	DATA SHEET	DATA SHEET
Quality Conformance Sample Testing	Method 5005	GROUP A, B, C & D PER JAN SPEC	GROUP A PLUS GENERIC B, C & D	GROUP A PLUS GENERIC B, C & D	GROUP A
External Visual Method 2009		3X to 10X	3X to 10X	3X to 10X	3X to 10X

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
00101	5430	01401	54150	03303	15950	07102	54S112
00102	5420	01402	9312‡	03304	9094	07103	54S113
00103	5410	01403	54153	03501	MH0026	07104	54S114
00104	5400	01404	9309	04001	54H50	07105	54S174
00105	5404	01405	54157	04002	54H51	07106	54S175
00106	5412	01406	54151	04003	54H53	07201	54S40
00107	5401	01501	5475	04004	54H54	07301	54S02
00108	5405	01502	5477	04005	54H55	07401	54S51
00109	5403	01503	54116	04101	54L51	07402	54S64
00201	5472	01504	9314‡	04102	54L54	07403	54S65
00202	5473	01601	5408	04103	54L55	07501	54S86
00203	54107	01602	5409	04104◆	54L54	07502	54S135
00204	5476	01701	54174	04201	54L121	07601†	54S194
00205	5474	01702	54175	04202	54L122	07602†	54S195
00206	5470	01703†	54173	04301	93L18	07701†	54S138
00207	5479‡	01801	54170	04401	93L24	07702†	54S139
00301	5440	01901	54180	04501†	93L14	07703†	54S280
00302	5437	02001	54L30	04502+	93L08	07801†	54S181
00303	5438	02002	54L20	04601	93L09	07802†	54S182
00401	5402	02003	54L10	04602	93L12	07901	54S151
00402	5423	02004	54L00	04603	93L22	07902	54S153
00403	5425	02005	54L04	05001	4011A	07903	54S157
00404	5427	02006	54L01/54L03	05002	4012A	07904	54S158
00501	5450	02101	54L71	05003	4023A	07905	54S251
00502	5451	02102	54L72	05101	4013A	07906	54S257
00503	5453	02103	54L73	05102	4027A	07907	54S258
00504	5454	02104	54L78	05201	4000A	08001	54S11
00601	5482	02105	54L74	05202	4001A	08002	54S15
00602	5483	02201	54H72	05203	4002A	08101	54S140
00603	9304‡	02202	54H73	05204	4025A	08201†	54S85
00701	5486	02203	54H74	05301	4007A	10101	52741
00801	5406	02204	54H76	05302	4019A	10102	52747
00802	5416	02205	54H101	05303	4030A	10103	52101A
00803	5407	02206	54H103	05401	4008A	10104	52108A
00804	5417	02301	54H30	05501	4009A	10105	LH2101A
00805	5426	02302	54H20	05502	4010A	10106	LH2108A
00901	5495	02303	54H10	05503	4049A	10107	52118
00902	5496	02304	54H00	05504	4050A	10201	52723
00903	54164	02305	54H04	05505	4041A	10202†	52104
00904	54165	02306	54H01	05601	4017A	10203†	52105
00905	54194	02307	54H22	05602	4018A	10301	52710
00906	54195	02401	54H40	05603	4020A	10302	52711
00907†	9300‡	02501	54L90	05604	4022A	10303	52106
00908†	9328	02502	54L93	05605	4024A	10304	52111
00909†	54198	02503	54L193	05701	4006A	10401	55107
00910†	54166	02504	93L10	05702	4014A	10402	55108
01001	5442	02505	93L16	05703	4015A	10403	55114
01002	5443	02601	54L86	05704	4021A	10404	55115
01003	5444	02701	54L02	05705	4031A	10405	55113
01004	5445	02801	54L95	05706†	4035A	10406	7831
01005	54145	02802	54L164	05707†	4034A	10407	7832
01006	5446	02803	93L28‡	05801†	4016A	10501†	52733
01007	5447	02804	93L00	06001	10501‡	10601	LM102‡
01008	5448	02805	76L70	06002	10502‡	10602	52110
01009	5449	02806◆	54L91	06003	10505‡	10701	52109
01101	54181	02901	54L42	06004	10506‡	10702†	LM140-12
01102	54182	02902	54L43	06005	10507‡	10703†	LM140-15
01201	54121	02903	54L44	06006	10509‡	10704†	LM140-24
01202	54122	02904	54L46	06101	10531‡	10801	3018A
01203	54123	02905	54L47	06102	10631‡	10802	3045
01204	9601	02906	76L42A	06103	10576‡	10901†	52555
01205	9602	02907	93L01	06104	10535‡	10902†	52556
01301	5492	03001	15930	06201†	10504	15001	5485
01302	5493	03002	15935	07001	54S00	15101	5413
01303	54160	03003	15936	07002	54S03	15102	5414
01304	54163	03004	15946	07003	54S04	15103	54132
01305	54162	03005	15962	07004	54S05	15201	54154
01306	54161	03101	15932	07005	54S10	15202	54155
01307	5490	03102	15944	07006	54S20	15203	54156
01308	54192	03103	15957	07007	54S22	15204	8250
01309	54193	03104	15958	07008	54S30	15205	8251
01310†	54196	03105	15933	07009	54S133	15206	8252
01311†	54197	03301	15945	07010	54S134	15301	54125
01312†	54177	03302	15948	07101	54S74	15302	54126

NOTE: Only the basic JAN and commercial numbers are shown.

†Slash sheets not released as of date of this publication.

‡Not recommended for new designs.

◆Class S only.

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
54LS153	30902†	54L164	02802	5423	00402	54163	01304
54LS157	30903†	54L193	02503	5425	00403	54164	00903
54LS158	30904†	54S00	07001	5426	00805	54165	00904
54LS160	31503†	54S02	07301†	5427	00404	54166	00910†
54LS161	31504†	54S03	07002	5428	16201†	54173	01703†
54LS164	30605†	54S04	07003	5430	00101	54174	01701
54LS168	31505†	54S05	07004	5432	16101†	54175	01702
54LS169	31506†	54S10	07005	5437	00302	53177	01312†
54LS174	30106†	54S11	08001	5438	00303	54180	01901
54LS175	30107†	54S15	08002	5440	00301	54181	01101
54LS181	30801	54S20	07006	5442	01001	54182	01102
54LS192	31507†	54S22	07007	5443	01002	54186	20101
54LS193	31508†	54S30	07008	5444	01003	54192	01308
54LS194	30601†	54S40	07201	5445	01004	54193	01309
54LS195	30602†	54S51	07401	5446	01006	54194	00905
54LS196	32001	54S64	07402	5447	01007	54195	00906
54LS197	32002	54S65	07403	5448	01008	54196	01310
54LS221	31402†	54S74	07101	5449	01009	54197	01311†
54LS251	30905†	54S85	08201	5450	00501	54198	00909†
54LS253	30908†	54S86	07501	5451	00502	5531	23001† (256 RAM)
54LS257	30906†	54S112	07102	5453	00503	55107	10401
54LS258	30907†	54S113	07103	5454	00504	55108	10402
54LS261	31801†	54S114	07104	5470	00206	55113	10405
54LS266	30303	54S133	07009	5472	00201	55114	10403
54LS279	31602†	54S134	07010	5473	00202	55115	10404
54LS283	31202†	54S135	07502	5474	00205	76L42A	02906
54LS290	32003	54S138	07701†	5475	01501	76L70	02805
54LS293	32004	54S139	07702†	5476	00204	7831	10406
54LS295	30606	54S140	08101	5477	01502	8250	15204
54LS298	30909	54S151	07901	5479‡	00207	8251	15205
54LS324	31702†	54S153	07902	5482	00601	8252	15206
54LS395	30607†	54S157	07903	5483	00602	9093	03304
54LS670	31901	54S158	07904	5485	15001	93L00	02804
54L00	02004	54S174	07105	5486	00701	93L01	02907
54L01	02006	54S175	07106	5490	01307	93L08	04502†
54L02	02701	54S181	07801†	5492	01301	93L09	04601
54L03	02006	54S182	07802†	5493	01302	93L10	02504
54L04	02005	54S194	07601†	5495	00901	93L12	04602
54L10	02003	54S195	07602†	5496	00902	93L14	04501†
54L20	02002	54S251	07905	54107	00203	93L16	02505
54L30	02001	54S257	07906	54116	01503	93L18	04301
54L42	02901	54S258	07907	54120	15401†	93L22	04603
54L43	02902	54S280	07703†	54121	01201	93L24	04401
54L44	02903	54S387	20201†	54122	01202	93L28‡	02803
54L46	02904	5400	00104	54123	01203	9300‡	00907†
54L47	02905	5401	00107	54125	15301	9300	15901†
54L51	04101	5402	00401	54126	15302	9304‡	00603
54L54	04102, 04104♦	5403	00109	54132	15103	9308	01503
54L55	04103	5404	00105	54145	01005	9309	01404
54L71	02101	5405	00108	54147	15601	9312‡	01402
54L72	02102	5406	00801	54148	15602	9314‡	01504
54L73	02103	5407	00803	54150	01401	9317	15802
54L74	02105	5408	01601	54151	01406	9318‡	15603†
54L78	02104	5409	01602	54153	01403	9322	01405
54L86	02601	5410	00103	54154	15201	9328	00908
54L90	02501	5412	00106	54155	15202	9334	16001
54L91	02806♦	5413	15101	54156	15203	9338	15701
54L93	02502	5414	15102	54157	01405	93410	23002 (266 RAM)
54L95	02801	5416	00802	54160	01303	9601	01204
54L121	04201	5417	00804	54161	01306	9602	01205
54L122	04202	5420	00102	54162	01305		

NOTE: Only the basic JAN and commercial numbers are shown.
†Slash sheets not released as of date of this publication.
‡Not recommended for new designs.
♦Class S only.

MILITARY PRODUCTS

TABLE I. JAN INTEGRATED CIRCUITS AND CIRCUIT-TYPE CROSS-REFERENCE

JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE
15401	54120	30002	54LS03	30502	54LS86	31202†	54LS283
15501	54H08	30003	54LS04	30601†	54LS194	31301†	54LS13
15502	54H11	30004	54LS05	30602†	54LS195	31302†	54LS14
15503	54H21	30005	54LS10	30603†	54LS95	31303†	54LS132
15601†	54147	30006	54LS12	30604†	54LS96	31401†	54LS123
15602†	54148	30007	54LS20	30605†	54LS164	31402†	54LS221
15603†	9318‡	30008	54LS22	30606†	54LS295	31501†	54LS90
15701	9338	30009	54LS30	30607†	54LS395	31502†	54LS93
15801	9321	30101†	54LS73	30701†	54LS138	31503†	54LS160
15802	9317	30102†	54LS74	30702†	54LS139	31504†	54LS161
15901†	9300	30103†	54LS112	30703†	54LS42	31505†	54LS168
15902†	9328	30104†	54LS113	30704†	54LS47	31506†	54LS169
16001	9334	30105†	54LS114	30801	54LS181	31507†	54LS192
16101†	5432	30106†	54LS174	30901†	54LS151	31508†	54LS193
16201†	5428	30107†	54LS175	30902†	54LS153	31601†	54LS75
20101	54186 (PROM 512)	30108†	54LS107	30903†	54LS157	31602†	54LS279
20102	MCM5304‡	30109†	54LS109	30904†	54LS158	31701†	54LS124
20103†	IM5603A	30110	54LS76	30905†	54LS251	31702†	54LS324
20201†	54S387 (PROM 1024)	30201	54LS40	30906†	54LS257	31801†	54LS261
20202†	IM5623	30202	54LS37	30907†	54LS258	31901	54LS670
23001†	5531 (256 RAM)	30203	54LS38	30908†	54LS253	32001	54LS196
23002†	93410 (256 RAM)	30204	54LS28	30909	54LS298	32002	54LS197
23501†	TMS4060 (4K RAM)	30301	54LS02	31001	54LS11	32003	54LS290
23502†	TMS4050 (4K RAM)	30302	54LS27	31002	54LS15	32004	54LS293
23503	TMS4060 (4K RAM)	30303	54LS266	31003	54LS21	32101	54LS22
23504	TMS4050 (4K RAM)	30401	54LS51	31004	54LS08	32102	54LS26
30001	54LS00	30402	54LS54	31101	54LS85	40001	6800
		30501	54LS32	31201†	54LS83A	42001	8080A

TABLE II. CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.	CKT TYPE	JAN /NO.
LH2101A	10105	3018A	10801	52111	10304	54LS13	31301†
LH2108A	10106	3045	10802	52118	10107	54LS14	31302†
LM102	10601	4000A	05201	52555	10901†	54LS15	31002
LM140-12	10702†	4001A	05202	52556	10902†	54LS20	30007
LM140-15	10703†	4002A	05203	52710	10301	54LS21	31003
LM140-24	10704†	4006A	05701	52711	10302	54LS22	32101
MCM5304‡	20102	4007A	05301	52723	10201	54LS26	32102
MH0026	03501	4008A	05401	52733	10501†	54LS27	30302†
TMS4050	23502 (4K RAM)	4009A	05501	52741	10101	54LS28	30204
TMS4050	23504 (4K RAM)	4010A	05502	54H00	02304	54LS30	30009†
TMS4060	23501 (4K RAM)	4011A	05001	54H01	02306	54LS32	30501
TMS4060	23503 (4K RAM)	4012A	05002	54H04	02305	54LS37	30202
1M5600	20103	4013A	05101	54H08	15501	54LS38	30203
1M5603A	20103†	4014A	05702	54H10	02303	54LS40	30201
1M5623	20202†	4015A	05703	54H11	15502	54LS42	30703†
10501‡	06001	4016A	05801†	54H20	02302	54LS47	30704†
10502‡	06002	4017A	05601	54H21	15503	54LS51	30401
10504	06201†	4018A	05602	54H22	02307	54LS54	30402
10505‡	06003	4019A	05302	54H30	02301	54LS73	30101†
10506‡	06004	4020A	05603	54H40	02401	54LS74	30102†
10507‡	06005	4021A	05704	54H50	04001	54LS75	31601†
10509‡	06006	4022A	05604	54H51	04002	54LS76	30110
10531‡	06101	4023A	05003	54H53	04003	54LS83A	31201
10535‡	06104	4024A	05605	54H54	04004	54LS85	31101
10576‡	06103	4025A	05204	54H55	04005	54LS86	30502
10631‡	06102	4027A	05102	54H72	02201	54LS90	31501†
15930	03001	4030A	05303	54H73	02202	54LS93	31502†
15932	03101	4031A	05705	54H74	02203	54LS95	30603†
15933	03105	4034A	05706†	54H76	02204	54LS96	30604†
15935	03002	4035A	05707†	54H101	02205	54LS107	30108†
15936	03003	4041A	05505	54H103	02206	54LS109	30109†
15944	03102	4049A	05503	54LS00	30001	54LS112	30103†
15945	03301	4050A	05504	54LS02	30301	54LS113	30104†
15946	03004	52101A	10103	54LS03	30002	54LS114	30105†
15948	03302	52104	10202†	54LS04	30003	54LS123	31401†
15950	03303	52105	10203†	54LS05	30004	54LS124	31701†
15951	03201	52106	10303	54LS08	31004	54LS132	31303†
15957	03103	52108A	10104	54LS10	30005	54LS138	30701†
15958	03104	52109	10701	54LS11	31001	54LS139	30702†
15962	03005	52110	10602	54LS12	30006	54LS151	30901†

NOTE: Only the basic JAN and commercial numbers are shown.

†Slash sheets not released as of date of this publication.

‡Not recommended for new designs.

IC Sockets and Interconnection Panels

IC SOCKETS AND INTERCONNECTION PANELS

Texas Instruments lines of off-the-shelf interconnection products are designed specifically to meet the performance needs of volume commercial applications. They provide both the economy of a standard product line and performance features developed after many year's experience with custom designs. Foremost among these is our ability to selectively bond a wrought gold stripe at the contact point. No waste. Reduced cost. Reliable contacts.

Wrought Gold Contact

Plate a contact with gold and you get a better contact. More reliable, longer lasting. Increase the gold, you improve the contact. But gold is precious, so improved performance has to be costly – right? Wrong. Because now you can get the gold only where it is needed – at the point of contact.

How? With selective metallurgical bonding; a gold stripe inlay. Not porous plating, but durable wrought gold bonded to the contact by the same technology used to produce clad coins and thermostat metals.

Texas Instruments, Attleboro, Massachusetts, is the world's largest producer of these multimetal systems. We also know our way around electronics. The result? A full line of reliable, low cost, interconnection systems featuring an extra measure of gold where it's needed. Premium performance at no premium in price.

IC Sockets

Texas Instruments family of IC sockets includes every type and size in common use today, and as wide a choice of contact materials as you'll find anywhere. Choose from open or closed entry *wire-wrapped*[†] sockets, standard or low profile solder tail sockets, cable plugs, and component platforms. Sizes from 8 to 40 pins.

IC Panels

To match the industry's broadest line of IC sockets TI offers one of the industry's widest selections of off-the-shelf socket panel products. Logic panels. Logic cards. Accessories. Add TI's custom design capability and wire wrapping for full service.

Additional information including pricing and delivery quotations may be obtained from your nearest TI Distributor, TI Representative, or:

Texas Instruments Incorporated
Connector Systems Department
MS 2-16
Attleboro, Massachusetts 02703
Telephone: (617) 222-2800
TELEX: ABORA927708

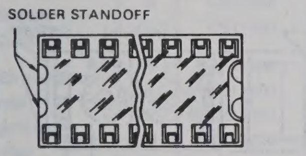
[†] Registered trademark of Gardner-Denver

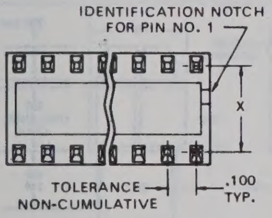
LOW PROFILE SOCKETS

SOLDER TAIL

C-93 SERIES GOLD-CLAD CONTACTS
C-83 SERIES TIN-PLATED CONTACTS

- **Universal mounting and packaging**
- **Anti-wicking wafer**
- **Stand-off tabs on base for solder flush**
- **Redundant contact points for low contact resistance, high reliability and repetitive insertion**
- **Closed entry construction**



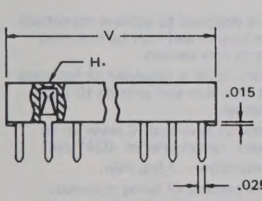


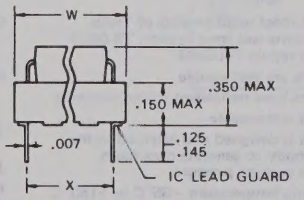
MATERIAL:

A. Body-glass filled nylon (GFN)
B. Contact-copper nickel alloy
C. Finish-see part number schedule

NOTES:

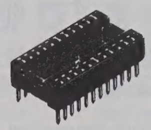
A. Sockets meet requirements of Texas Instruments test specification TS-0005 and test report TR-0003
B. Operating temperature −65° C to ±150° C
C. Contacts have redundant spring elements
D. Accommodates standard IC leads up to .024" square, rectangular, or .024" diameter
E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
F. Socket is designed to achieve maximum density on boards
G. Sockets may be mounted end to end on .100" centers continuous line or on .400" centers row to row
H. Socket is designed to prevent IC leads from contacting P.C. board
I. Closed entry feature provided to facilitate automatic IC insertion and protects the IC leads against damage





	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	40 Pin
Dimension X ±.005	.300	.300	.300	.300	.300	.400	.600	.600	.600
Dimension V ±.010	.400	.700	.800	.900	1.000	1.100	1.200	1.400	2.000
Dimension W (max)	.400	.400	.400	.400	.400	.500	.700	.700	.700

PART NO. SCHEDULE



BLACK BODY

NOMEX ANTI-WICKING WAFER

Pins	C-93 SERIES	C-83 SERIES
8	C930810	C830810
14	C931410	C831410
16	C931610	C831610
18	C931810	C831810
20	C932010	C832010
22	C932210	C832210
24	C932410	C832410
28	C932810	C832810
40	C934010	C934010

CONTACT FINISH
C-93 SERIES:
100 microinch minimum gold stripe inlay
C-83 SERIES:
200 microinch minimum bright tin plate

STANDARD PROFILE SOCKET

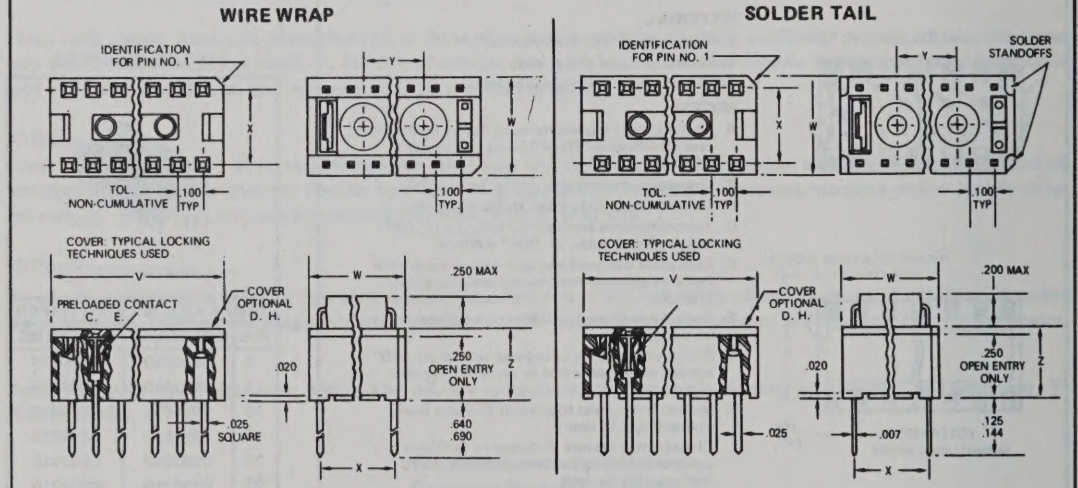
SOLDER TAIL

C-82 SERIES PLATED CONTACTS • C-92 SERIES GOLD CLAD CONTACTS

WIRE WRAP

C-81 SERIES PLATED CONTACTS • C-91 SERIES GOLD CLAD CONTACTS

- Designed for low cost, reliable, high density production packaging
- Universal mounting and packaging capabilities
- 8 to 40 pin lead configurations
- Contacts accommodate .015" through .024" rectangular or round dual-in-line leads
- Wire wrap posts held to true position of .015" providing a true position of .020" on boards for efficient automatic wire wrapping


WIRE WRAP
IDENTIFICATION FOR PIN NO. 1
Y
X
W
TOL. NON-CUMULATIVE
.100 TYP
.100 TYP.
COVER: TYPICAL LOCKING TECHNIQUES USED
V
PRELOADED CONTACT C. E.
COVER OPTIONAL D. H.
.020
.025 SQUARE
W
.250 MAX
.250 OPEN ENTRY ONLY
Z
.640 .690
X
SOLDER TAIL
IDENTIFICATION FOR PIN NO. 1
Y
SOLDER STANDOFFS
X
W
TOL. NON-CUMULATIVE
.100 TYP
.100 TYP
COVER: TYPICAL LOCKING TECHNIQUES USED
V
COVER OPTIONAL D. H.
.025
W
.200 MAX
.020
.250 OPEN ENTRY ONLY
Z
.125 .144
.007
X

MATERIAL:

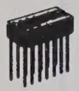
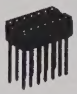
- A. Body-glass filled nylon (GFN)
- B. Contact-phosphor bronze per QQ-B-750 (C-81) copper nickel alloy (C-91)
- C. Finish-see part number schedule

NOTES:

- A. Sockets meet requirements of Texas Instruments test specification TS-0003 and test report TR-0001
- B. Contacts are replaceable
- C. Contacts have redundant spring elements
- D. Cover is removeable
- E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
- F. Operating temperature –65°C to +150°C
- G. Sockets are designed to achieve maximum density on boards and may be mounted .400" row to row centers
- H. Closed entry cover is provided to facilitate automatic insertion and protect IC leads against damage
- I. Accommodates standard IC leads up to .024" square, rectangular or .024" dia.
- J. Contact retention — 7 lbs. min.
- K. Sockets are capable of being automatically or semiautomatically wire wrapped

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	24 Pin	28 Pin	36 Pin	40 Pin
Dimension V ±0.10	.465	.765	.865	.965	1.065	1.280	1.480	1.845	2.045
Dimension W (max)	.400	.400	.400	.400	.400	.700	.700	.700	.700
Dimension X ±.005	.300	.300	.300	.300	.300	.600	.600	.600	.600
Dimension Y ±0.10	NA	.400	.400	.400	.400	.500	.500	.800	1.000
Dimension Z ±.005	.280	.280	.280	.280	.280	.280	.280	.325	.325

WIRE WRAP

		OPEN ENTRY	CLOSED ENTRY
PART NUMBER SCHEDULE			
Contact Finish	Pins	Black Body	Black Cover
Series **C-81** 200-400 microinch min tin per MIL-T-10727	8	C810854	C810804
	14	C811454	C811404
	16	C811654	C811604
	18	C811854	C811804
	20	C812054	C812004
	24	C812454	C812404
	28	C812854	C812804
	36		C813604
	40		C814004
Series **C-91** 50 microinch min gold stripe inlay	8	C910850	C910800
	14	C911450	C911400
	16	C911650	C911600
	18	C911450	C911400
	20	C912050	C911800
	24	C912450	C912000
	28	C912850	C912800
	36		C913600
	40		C914000

SOLDER TAIL

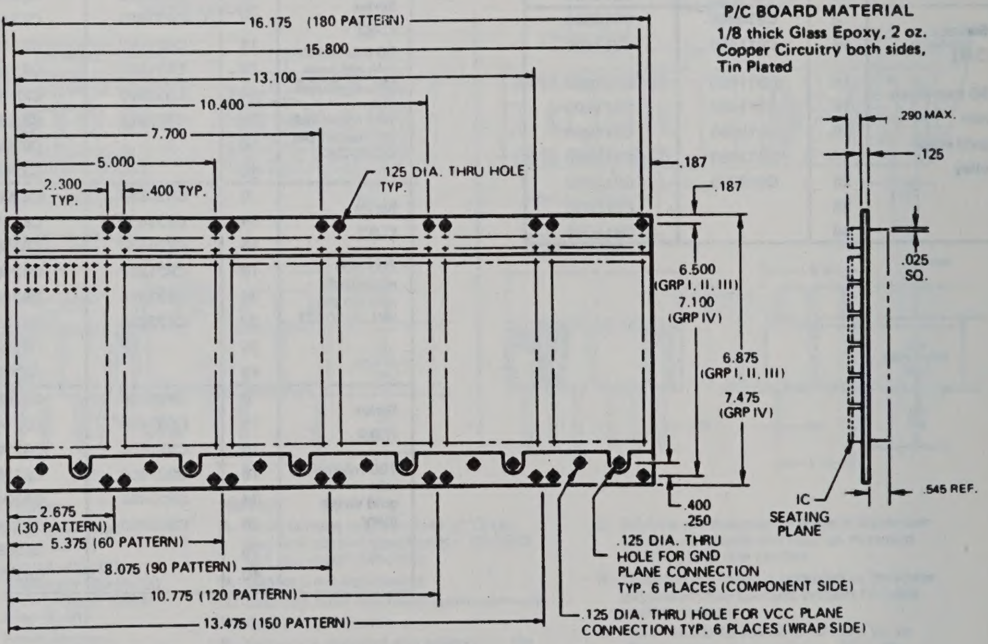
		OPEN ENTRY	CLOSED ENTRY
PART NUMBER SCHEDULE			
Contact Finish	Pins	Black Body	Black Cover
Series **C-82** 30 microinch min gold per MIL-G-45204 over 50 microinch min nickel per QQ-N-290	8	C820850	C820800
	14	C821450	C821400
	16	C821650	C821600
	18	C821850	C821800
	24	C822450	C822400
	28	C822850	C822800
	36		C823600
	40		C824000
Series **C-82** 50 microinch min gold per MIL-G-45204 over 100 microinch min nickel per QQ-N-290	8	C820852	C820802
	14	C821452	C821402
	16	C821652	C821602
	18	C821852	C821802
	24	C822452	C822402
	28	C822852	C822802
	36		C823602
	40		C824002
Series **C-82** 200-400 microinch min tin per MIL-T-10727	8	C820854	C820804
	14	C821454	C821404
	16	C821654	C821604
	18	C821854	C821604
	24	C822454	C822404
	28	C822854	C822804
	36		C823604
	40		C824004
Series **C-92** 100-microinch min gold stripe inlay	8	C920850	C920800
	14	C921450	C921400
	16	C921650	C921600
	18	C921850	C921800
	24	C922450	C922400
	28	C922850	C922800
	36		C923600
	40		C924000

SOCKET PANELS

STANDARD

D4 SERIES

- 180 position panel or multiples of 30 position with 14 or 16 position socket pattern
- I/O – 4 rows with 13 pins per row or 3 - 14 pin sockets
- Low cost standard hardware
- Available in 98 standard series
- Off-the-shelf availability


16.175 (180 PATTERN)
15.800
13.100
10.400
7.700
5.000
2.300 TYP.
.400 TYP.
.125 DIA. THRU HOLE TYP.
.187
.187
.290 MAX.
.125
.025 SQ.
6.500 (GRP I, II, III)
7.100 (GRP IV)
6.875 (GRP I, II, III)
7.475 (GRP IV)
.545 REF.
IC SEATING PLANE
.400
.250
2.675 (30 PATTERN)
5.375 (60 PATTERN)
8.075 (90 PATTERN)
10.775 (120 PATTERN)
13.475 (150 PATTERN)
.125 DIA. THRU HOLE FOR GND PLANE CONNECTION TYP. 6 PLACES (COMPONENT SIDE)
.125 DIA. THRU HOLE FOR VCC PLANE CONNECTION TYP. 6 PLACES (WRAP SIDE)

P/C BOARD MATERIAL
1/8 thick Glass Epoxy, 2 oz. Copper Circuitry both sides, Tin Plated

NOTE: Dimensions shown are nominal. Detail information and tolerances available on request (indicate series and group number).

STANDARD SOCKETS

C-81 or C-91 series, 14 pin or 16 pin, closed entry sockets as designated in the Part No. Schedule at right. See pages 7 and 8 for complete socket information.

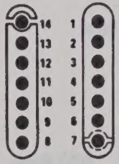
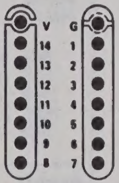
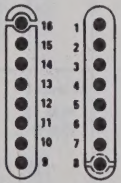
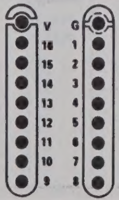
C-81 SERIES SOCKETS

Body......... Glass filled nylon
Contact .... Phosphor bronze per QQ-B-750
Finish .... 30 microinch min. gold per MIL-G-45204 *over* 50 microinch min. nickel per QQ-N-290

C-91 SERIES SOCKETS

Body......... Glass filled nylon
Contact .... Copper nickel alloy
Finish .... 50 microinch min. gold stripe inlay

STANDARD PANEL PART NO. SCHEDULE –D4 Series

Group No.	I/O Option	Sockets Per Panel	C-81 Sockets	C-91 Sockets
Group I **14 Pin** PIN 14 .... VCC PIN 7 ...... GRD 	SOCKETS 	30	D411211	D411231
		60	D411212	D411232
		90	D411213	D411233
		120	D411214	D411234
		150	D411215	D411235
		180	D411216	D411236
	FEED-THRU PINS 	30	D411411	D411431
		60	D411412	D411432
		90	D411413	D411433
		120	D411414	D411434
		150	D411415	D411435
		180	D411416	D411436
Group II **14 Pin** PIN V ...... VCC PIN G ...... GRD 	SOCKETS 	30	D434211	D434231
		60	D434212	D434232
		90	D434213	D434233
		120	D434214	D434234
		150	D434215	D434235
		180	D434216	D434236
	FEED-THRU PINS 	30	D434411	D434431
		60	D434412	D434432
		90	D434413	D434433
		120	D434414	D434434
		150	D434415	D434435
		180	D434416	D434436.
Group III **16 Pin** PIN 16 .... VCC PIN 8 ...... GRD 	SOCKETS 	30	D423211	D423231
		60	D423212	D423232
		90	D423213	D423233
		120	D423214	D423234
		150	D423215	D423235
		180	D423216	D423236
	FEED-THRU PINS 	30	D423411	D423431
		60	D423412	D423432
		90	D423413	D423433
		120	D423414	D423434
		150	D423415	D423435
		180	D423416	D423436
Group IV **16 Pin** PIN V ...... VCC PIN G ...... GRD 	SOCKETS 	30	D444211	D444231
		60	D444212	D444232
		90	D444213	D444233
		120	D444214	D444234
		150	D444215	D444235
		180	D444216	D444236
	FEED-THRU PINS 	30	D444411	D444431
		60	D444412	D444432
		90	D444413	D444433
		120	D444414	D444434
		150	D444415	D444435
		180	D444416	D444436

SOCKET CARDS

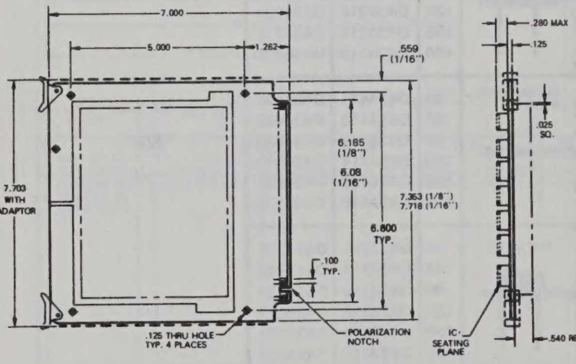
STANDARD

DO2 SERIES

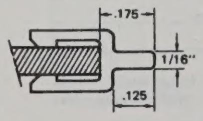
- Low Cost
- 14 - 16 pin socket pattern – 60 position
- Standard ground and power pin commitment
- 8 standard designs
- Mates with dual 60 position edge connector

P/C BOARD MATERIAL

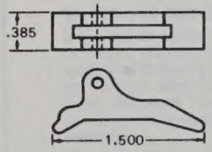
1/16 and 1/8 thick Glass Epoxy, 2 oz. Copper Circuitry both sides, Tin Plated


7.000
5.000
1.262
.559
(1/16")
.280 MAX
.125
.025
SQ.
6.185
(1/8")
6.08
(1/16")
7.703
WITH
ADAPTOR
7.363 (1/8")
7.718 (1/16")
6.800
TYP.
.100
TYP.
.125 THRU HOLE
TYP. 4 PLACES
POLARIZATION
NOTCH
IC
SEATING
PLANE
.540 REF.

NOTE: Dimensions shown are nominal. Detail information and tolerances available on request (indicate series and group number).



ADAPTER
Part no. Z501300



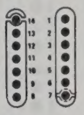
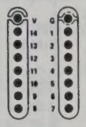
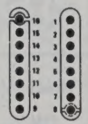
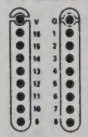
EJECTOR KEYS
Material: Nylon
Part no. Z501200 (1/8")
Z501201 (1/16")

DO Series
MULTIPURPOSE CARD PART NO. SCHEDULE

I/O

Board Thk.	Part No.
1/16"	Z012510
1/8"	Z011510

DO2 Series
STANDARD CARD PART NO. SCHEDULE

Group No.	Board Thk.	C-81 Sockets	C-91 Sockets
Group I 14 Pin PIN 14 ..... VCC PIN 7 ..... GRD  14 13 12 11 10 9 8 1 2 3 4 5 6 7	1/16"	D022110	D022130
	1/8"	D021110	D021130
Group II 14 Pin PIN V ..... VCC PIN G ..... GRD  V 14 13 12 11 10 9 8 G 1 2 3 4 5 6 7	1/16"	D022310	D022330
	1/8"	D021310	D021330
Group III 16 Pin PIN 16 ..... VCC PIN 8 ..... GRD  16 15 14 13 12 11 10 9 1 2 3 4 5 6 7 8	1/16"	D022210	D022230
	1/8"	D021210	D021230
Group IV 16 Pin PIN V ..... VCC PIN G ..... GRD  V 16 15 14 13 12 11 10 9 G 1 2 3 4 5 6 7 8	1/16"	D022410	D022430
	1/8"	D021410	D021430